19-3354; Rev 0; 8/04

MAXIM

SFP铜缆预加重驱动器

概述

MAX3982是工作于1Gbps到4.25Gbps的单通道铜缆预加重驱动器。它能够为4.25Gbps光纤通道等铜线连接提供补偿，允许跨距达15米的24AWG电缆连接。该电缆驱动器提供4种可选预加重级别。对于工作在4.25Gbps速率的FR4电路板，其输入补偿可达10英寸。

MAX3982还具有灵敏度可选的SFP兼容信号丢失检测功能和TX_DISABLE功能。输出摆幅可设置以够降低EMI和功耗。采用3mm x 3mm，16引脚薄型QFN封装，工作温度范围为0°C到+85°C。

应用

SFP有源铜缆装配

背板

1.0625Gbps，2.125Gbps和4.25Gbps光纤通道

1.25Gbps以太网

2.488Gbps STM16

InfiniBand

PCI Express

特性

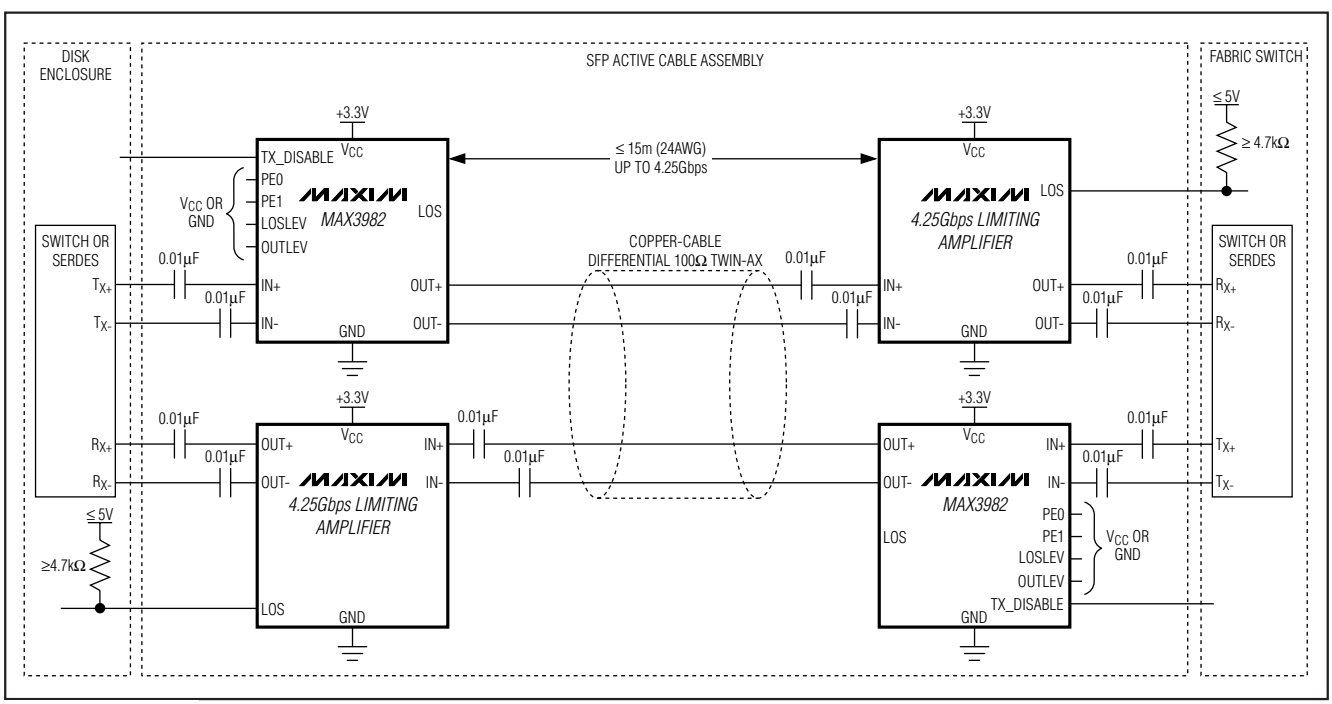
- 24AWG电缆传输距离达15米
- FR4电路板上传输距离达30英寸
- +3.3V供电总功耗为0.25W
- 可选1600mV$_{P-P}$或者1200mV$_{P-P}$差分输出摆幅
- 可选输出预加重
- 固定输入均衡
- 灵敏度可选的信号丢失检测
- 发送禁止功能

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3982UTE	0°C to +85°C	16 Thin QFN	T1633-4

引脚配置在数据手册末尾。

定购信息



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +6.0V
Continuous CML Output Current
at OUT+, OUT-.....-25mA to +25mA
Voltage at IN+, IN-, LOSLEV, LOS,
TX_DISABLE, PE0, PE1, OUTLEV .....-0.5V to (V_{CC} + 0.5V)
LOS Open Collector Supply Voltage
with ≥ 4.7kΩ Pullup Resistor.....-0.5V to +5.5V
Continuous Power Dissipation at +85°C
(derate 20.8mW/°C above +85°C).....1.35W
Operating Junction Temperature Range (T_J)....-55C° to +150°C
Storage Ambient Temperature Range (T_S) .....-55C° to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C and V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current		TX_DISABLE=low		75	97	mA
Inrush Current		Current beyond steady-state current			10	mA
Power-On-Reset Delay	t_{POR}		1		40	ms
OPERATING CONDITIONS						
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
Supply-Noise Tolerance		1MHz ≤ f < 2GHz		40		mV_{P-P}
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data (Note 1)	1.0		4.25	Gbps
CID		Consecutive identical digits (bits) (Note 1)			10	Bits
CONTROL INPUTS: TX_DISABLE, PE0, PE1, OUTLEV, LOSLEV						
Voltage, Logic High	V_{IH}		2.0			V
Voltage, Logic Low	V_{IL}				0.8	V
Current, Logic High	I_{IH}	V_{IH} = V_{CC} + 0.5V			-150	µA
Current, Logic Low	I_{IL}	V_{IL} = 0.8V			350	µA
STATUS OUTPUT: LOS						
LOS Open Collector Current Sink		LOS asserted	0		25	µA
		LOS unasserted, V_{OL} ≤ 0.4V with 4.7kΩ pullup resistor, pullup supply = 5.5V	1.0			mA
		V_{CC} = 0V, pullup supply = 5.5V, external pullup resistor ≥ 4.7kΩ	0		25	µA
LOS Assert Level		LOSLEV = high (Note 1)	100			mV_{P-P}
		LOSLEV = low (Note 1)	50			mV_{P-P}
LOS Deassert Level		LOSLEV = high (Note 1)			300	mV_{P-P}
		LOSLEV = low (Note 1)			120	mV_{P-P}
LOS Hysteresis		LOSLEV = high (Note 1)	20			mV_{P-P}
		LOSLEV = low (Note 1)		4		mV_{P-P}
LOS Response Time		Time from IN dropping below assert level, or rising above deassert level to 50% point of LOS			10	µs
LOS Transition Time		Rise-time or fall-time (10% to 90%), external pullup resistor = 4.7kΩ		250		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values are at T_A = +25°C and V_{CC} = +3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP	MAX	UNITS
EQUALIZER AND CABLE DRIVER SPECIFICATIONS									
Input Swing		Measured differentially at point A of Figure 2 (Note 1)				600		2000	mV_{P-P}
Input Resistance		Measured differentially				85	100	115	Ω
Input Return Loss		100MHz to 2GHz (Note 1)				10			dB
Differential Output Swing		Measured differentially at point B of Figure 2 (Notes 1, 2)	TX_DISABLE = low, OUTLEV = high			1450		1800	mV_{P-P}
			TX_DISABLE = low, OUTLEV = low			1000		1350	
			TX_DISABLE = high				40		
Common-Mode Output		(OUT+) + (OUT-), measured at point B of Figure 2; TX_DISABLE = low, OUTLEV = high (Notes 1, 2)						60	mV_{P-P}
Output Resistance		OUT+ or OUT- to V_{CC}, single ended				42	50	58	Ω
Output Return Loss		100MHz to 2GHz (Note 1)				10			dB
Output Transition Time	t_r, t_f	20% to 80% (Notes 1, 3)					50	80	ps
Random Jitter		(Notes 1, 3)						1.6	ps_{RMS}
Output Preemphasis		See Figure 1		PE1	PE0				dB
				0	0		2		
				0	1		4		
				1	0		8		
				1	1		14		
Residual Output Deterministic Jitter at 1.0625Gbps to 2.125Gbps (Notes 1, 4, 5)		Source to IN	OUT to Load	PE1	PE0				UI_{P-P}
		6 mil FR4 ≤ 10in	1m, 24AWG	0	0		0.10	0.15	
			5m, 24AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				
Residual Output Deterministic Jitter at 4.25Gbps (Notes 1, 4, 5)		Source to IN	OUT to Load	PE1	PE0				UI_{P-P}
		6 mil FR4 ≤ 10in	1m, 24AWG	0	0		0.15	0.20	
			5m, 24AWG	0	1				
			10m, 24AWG	1	0				
			15m, 24AWG	1	1				

Note 1: Guaranteed by design and characterization.

Note 2: PE1 = PE0 = 1 for maximum preemphasis, load is 50Ω ±1% at each side, and the pattern is 0000011111 at 1Gbps.

Note 3: Measured at point B in Figure 2 using 0000011111 at 1Gbps. PE1 = PE0 = 0 for minimum preemphasis. For transition time, the 0% reference level is the steady-state level after four zeros, just before the transition. The 100% reference level is the maximum voltage of the transition.

Note 4: Tested with CJTPAT, as well as this pattern: 19 zeros, 1, 10 zeros, 1010101010 (D21.5 character), 1100000101 (K28.5+ character), 19 ones, 0, 10 ones, 0101010101 (D10.2 character), 0011111010 (K28.5 character).

Note 5: Cables are unequalized, Amphenol Spectra-Strip 24AWG. Residual deterministic jitter is the difference between the source jitter at point A, and load jitter at point D in Figure 2. The deterministic jitter at the output of the transmission line must be from media-induced loss and not from clock-source modulation.

SFP铜缆预加重驱动器

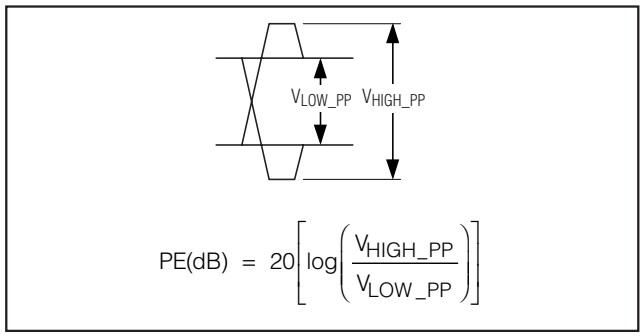


图 1. 用 dB 表示的 Tx 预加重

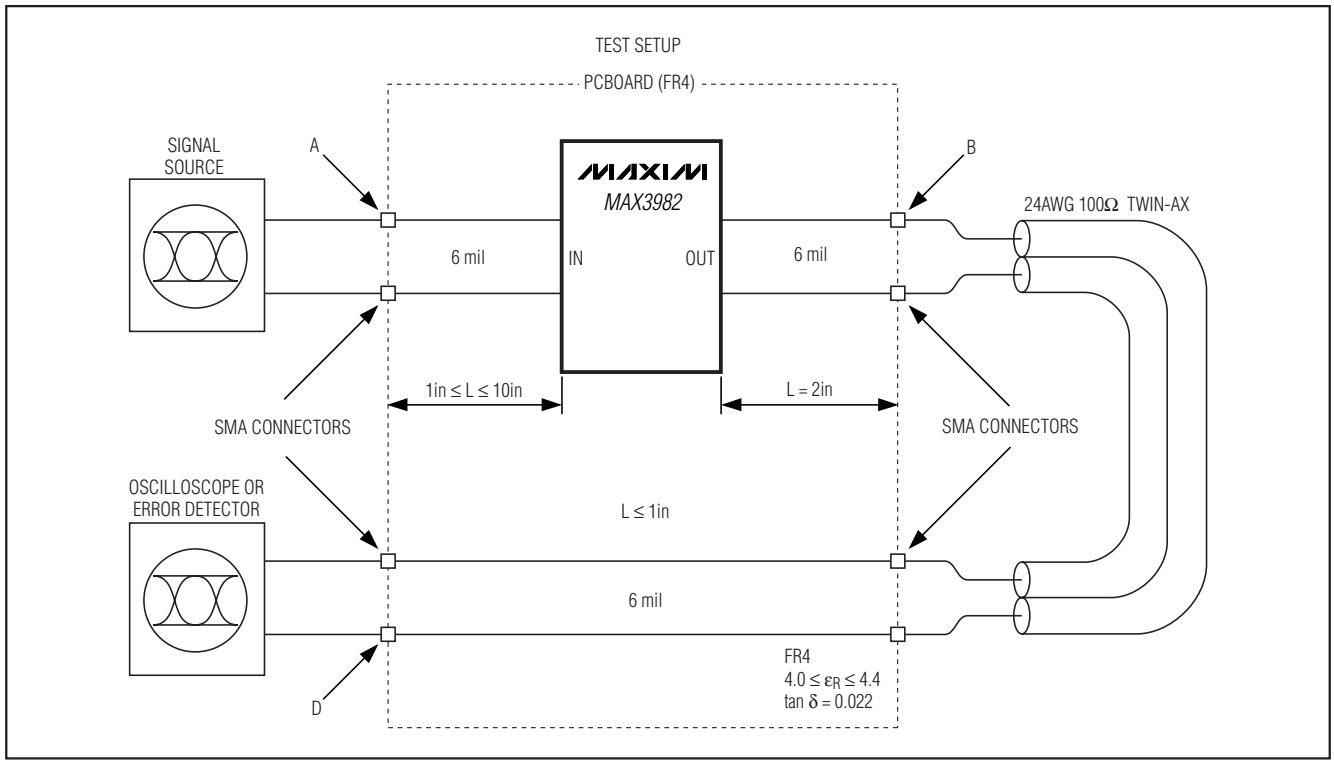


图 2. 测试设置。标注为 A，B，D 的点为 AC 参数测试条件的参考点。在 D 点进行确定性抖动和眼图测量。

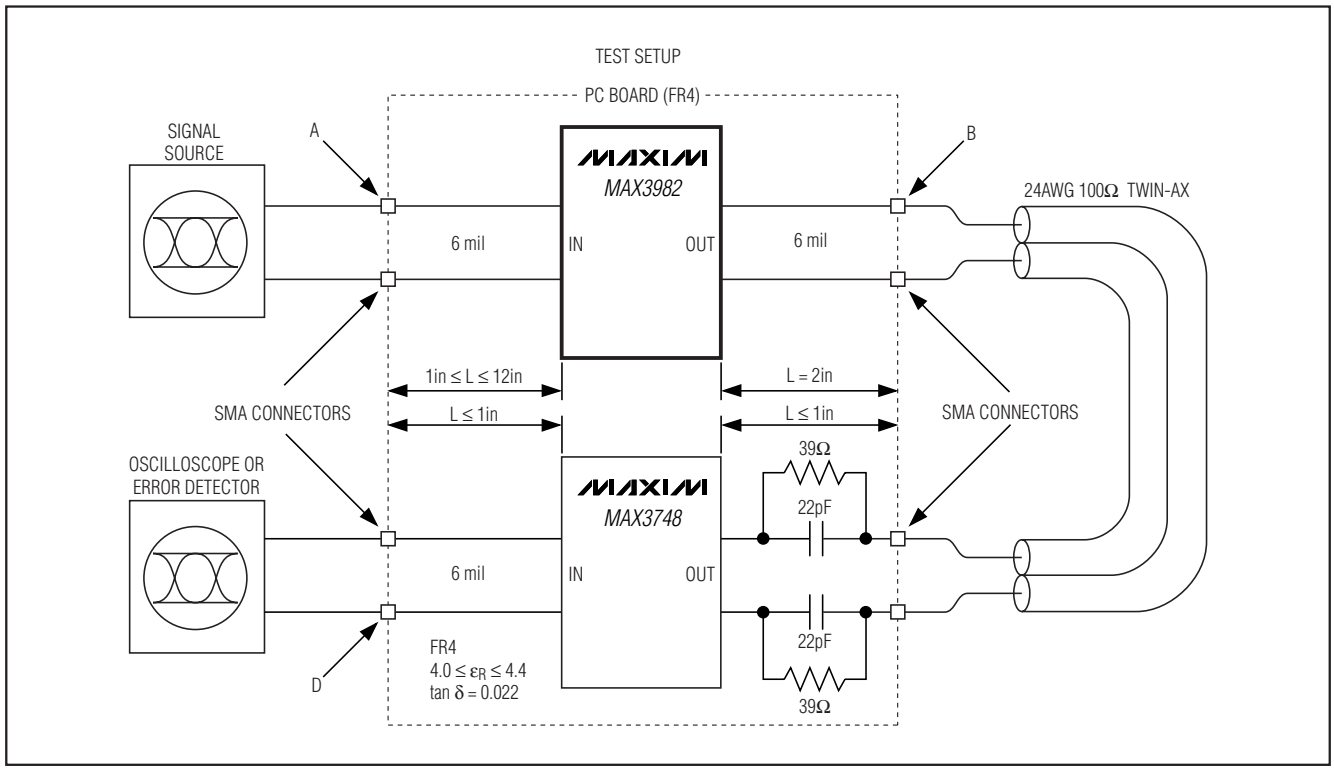
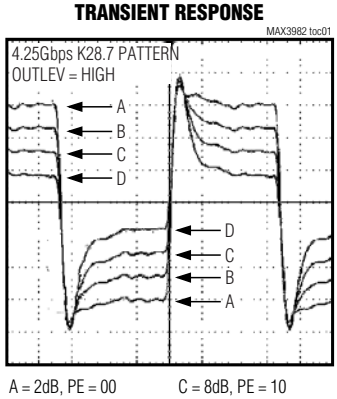


图 3. 端到端测试中采用 MAX3748 作为接收器。在 D 点进行确定性抖动和眼图测量。

典型工作特性

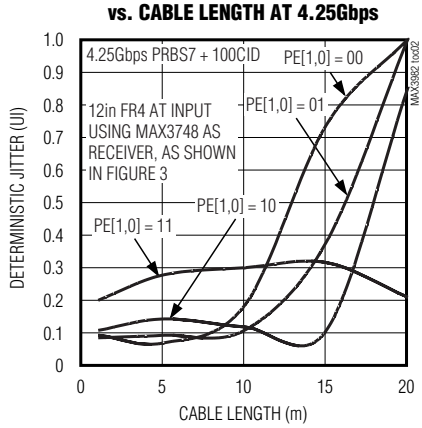
(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.)

TRANSIENT RESPONSE

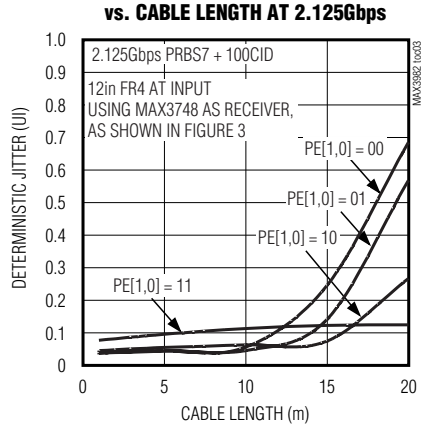


A = 2dB, PE = 00
B = 4dB, PE = 01
C = 8dB, PE = 10
D = 14dB, PE = 11

END-TO-END DETERMINISTIC JITTER vs. CABLE LENGTH AT 4.25Gbps



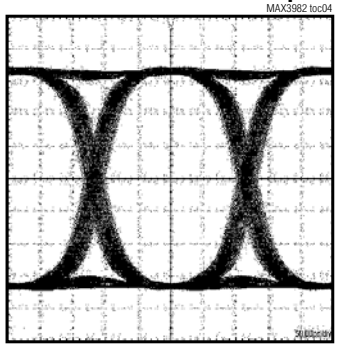
END-TO-END DETERMINISTIC JITTER vs. CABLE LENGTH AT 2.125Gbps



典型工作特性(续)

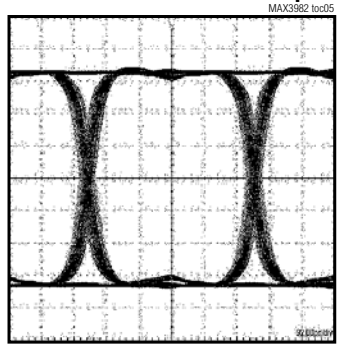
(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.)

END-TO-END EYE DIAGRAM, 20m 24AWG CABLE AT 4.25Gbps



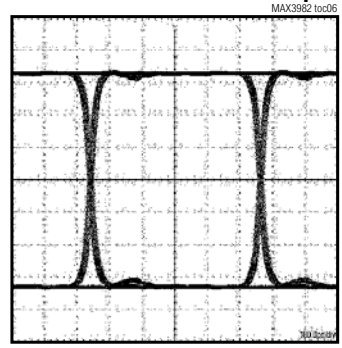
4.25Gbps PRBS7 + 100CID PATTERN, 0in FR4 AT INPUT, USING MAX3748 AS RECEIVER, AS SHOWN IN FIGURE 3

END-TO-END EYE DIAGRAM, 20m 24AWG CABLE AT 2.125Gbps



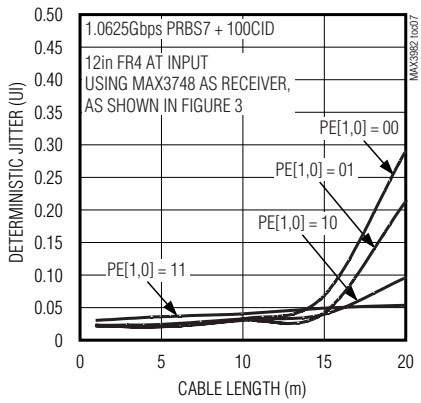
2.125Gbps PRBS7 + 100CID PATTERN, 0in FR4 AT INPUT, USING MAX3748 AS RECEIVER, AS SHOWN IN FIGURE 3

END-TO-END EYE DIAGRAM, 20m 24AWG CABLE AT 1.0625Gbps

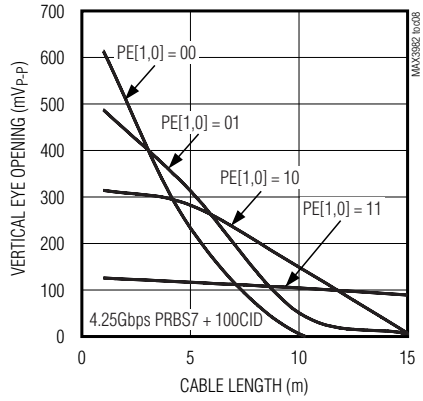


1.0625Gbps PRBS7 + 100CID PATTERN, 0in FR4 AT INPUT, USING MAX3748 AS RECEIVER, AS SHOWN IN FIGURE 3

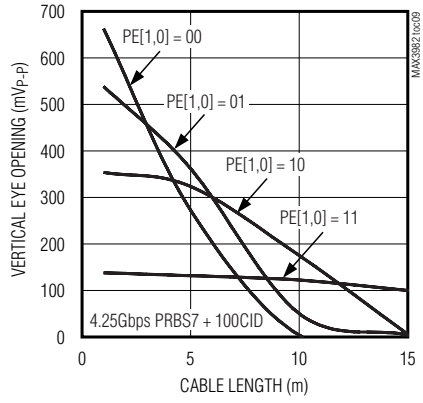
END-TO-END DETERMINISTIC JITTER vs. CABLE LENGTH AT 1.0625Gbps



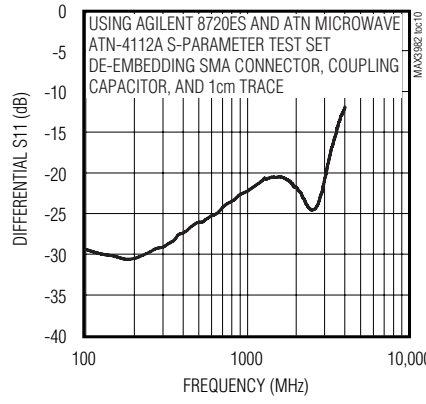
VERTICAL EYE OPENING vs. CABLE LENGTH WITH OUTLEV = LOW



VERTICAL EYE OPENING vs. CABLE LENGTH WITH OUTLEV = LOW



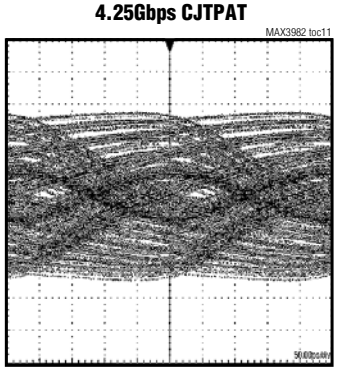
INPUT RETURN LOSS vs. FREQUENCY



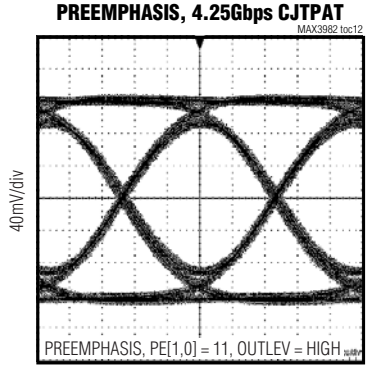
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.)

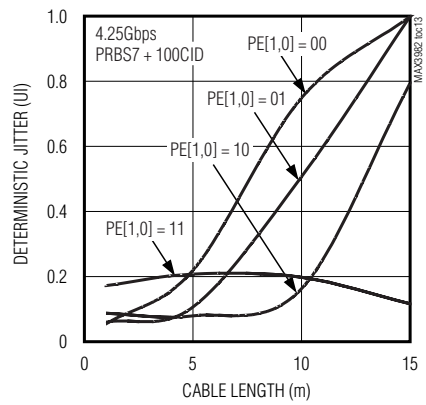
15m 24AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3982, 4.25Gbps CJTPAT



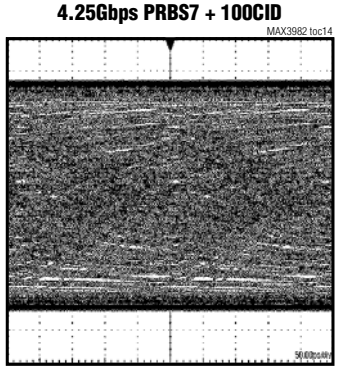
15m 24AWG CABLE ASSEMBLY OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps CJTPAT



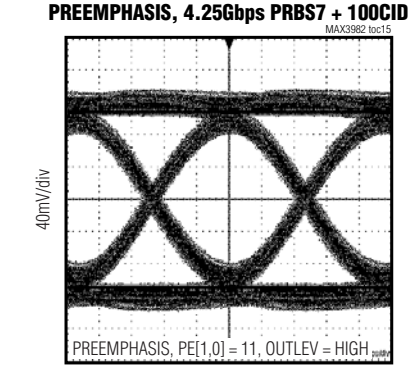
DETERMINISTIC JITTER vs. CABLE LENGTH



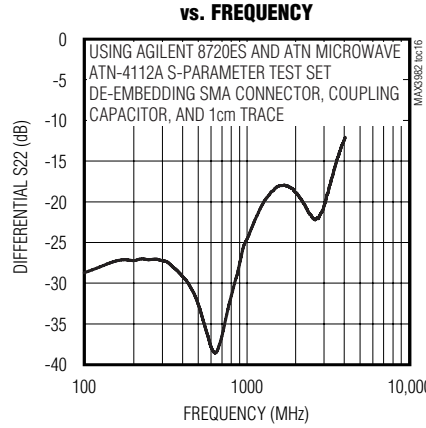
15m 24AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3982, 4.25Gbps PRBS7 + 100CID



15m 24AWG CABLE ASSEMBLY OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps PRBS7 + 100CID



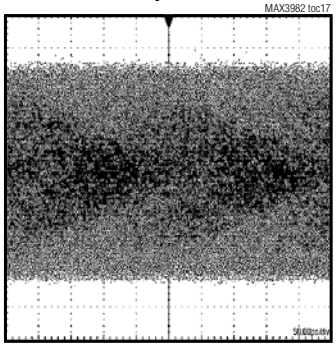
OUTPUT RETURN LOSS vs. FREQUENCY



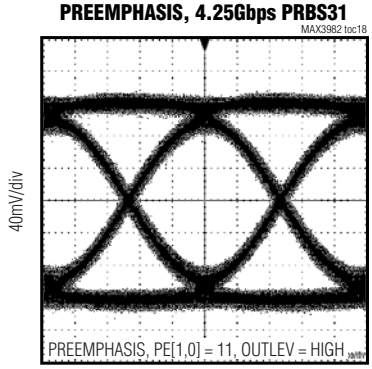
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.)

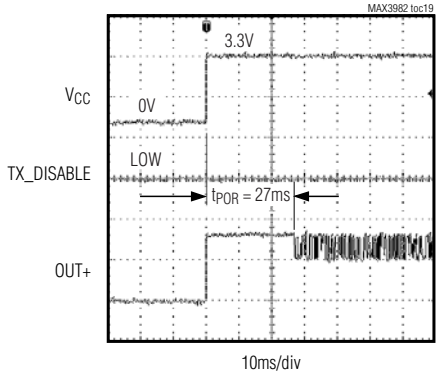
15m 24AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3982, 4.25Gbps PRBS31



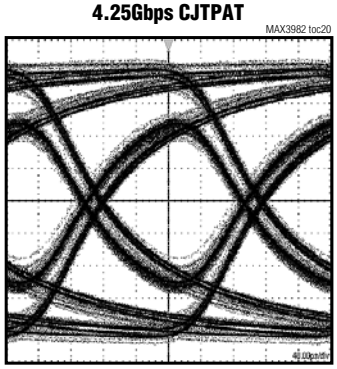
15m 24AWG CABLE ASSEMBLY OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps PRBS31



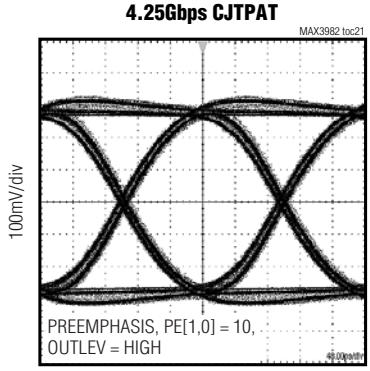
HOT-PLUG WITH TX_DISABLE LOW



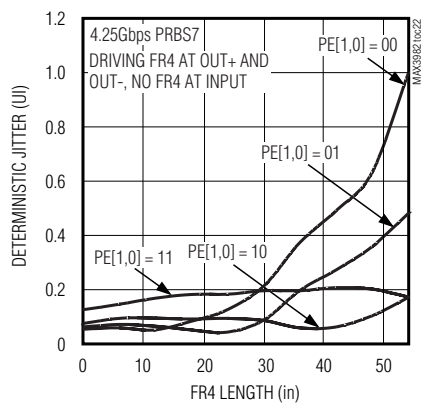
30in FR4 OUTPUT WITHOUT MAX3982, 4.25Gbps CJTPAT



30in FR4 OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps CJTPAT



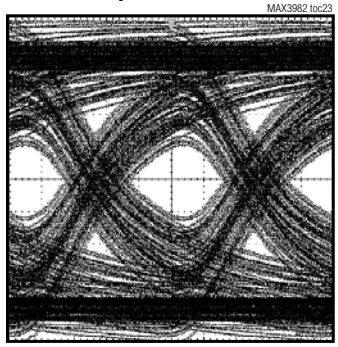
DETERMINISTIC JITTER vs. FR4 LENGTH



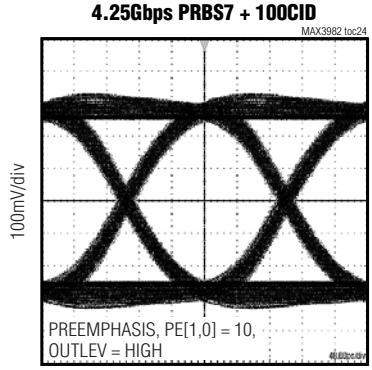
典型工作特性(续)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted. PRBS7 + 100CID pattern is PRBS 2^7, 100 zeros, 1010, PRBS 2^7, 100 ones, 0101.)

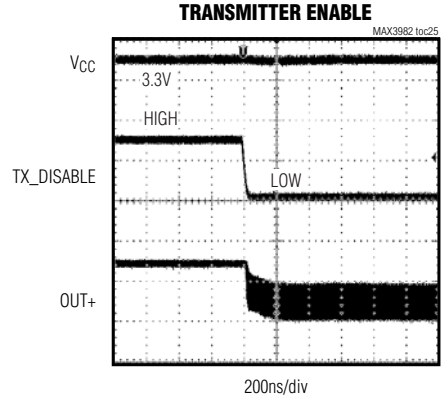
30in FR4 OUTPUT WITHOUT MAX3982 4.25Gbps PRBS7 + 100CID



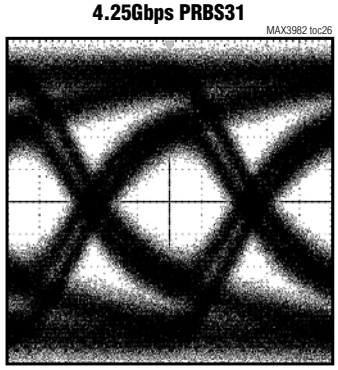
30in FR4 OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps PRBS7 + 100CID



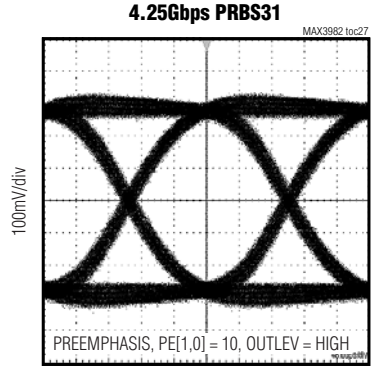
TRANSMITTER ENABLE



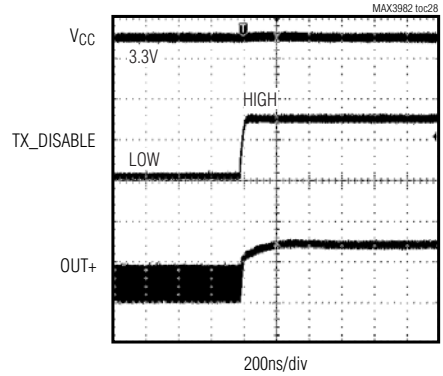
30in FR4 OUTPUT WITHOUT MAX3982, 4.25Gbps PRBS31



30in FR4 OUTPUT WITH MAX3982 PREEMPHASIS, 4.25Gbps PRBS31



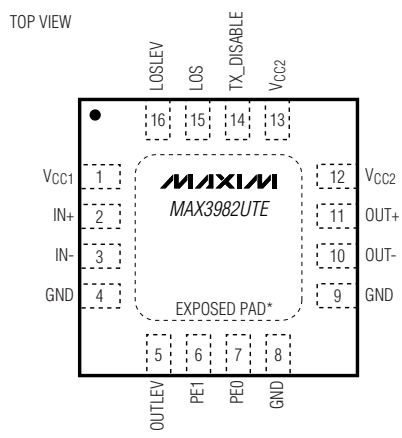
TRANSMITTER DISABLE



引脚说明

引脚	名称	功能
1	V_{CC1}	电源输入端，接+3.3V。
2	IN+	数据输入正端，CML。该输入在内部以50Ω端接到V_{CC1}。
3	IN-	数据输入负端，CML。该输入在内部以50Ω端接到V_{CC1}。
4, 8, 9	GND	电路地。
5	OUTLEV	输出摆幅控制输入，为带40kΩ内部上拉电阻的LVTTL，置为TTL高电平或开路为最大输出摆幅，置为TTL低电平降低输出摆幅。
6	PE1	输出预加重控制输入，为带10kΩ内部上拉电阻的LVTTL。该引脚为2位预加重控制位的高位。通过设为高电平或开路来置位。
7	PE0	输出预加重控制输入，为带10kΩ内部上拉电阻的LVTTL。该引脚为2位预加重控制位的低位。通过设为高电平或开路来置位。
10	OUT-	数据输出负端，CML。该输出以50Ω端接到V_{CC2}。
11	OUT+	数据输出正端，CML。该输出以50Ω端接到V_{CC2}。
12, 13	V_{CC2}	输出级的电源端，接+3.3V。
14	TX_DISABLE	发送禁止输入，为带10kΩ内部上拉电阻的LVTTL。置高或开路时，差分输出为40mV_{P-P}。正常操作时置低。
15	LOS	信号丢失检测，TTL输出。该输出为集电极开路的TTL输出，需要一个4.7kΩ至10kΩ的外部上拉电阻(最大5.5V)。当输入信号电平有效时，该输出将吸收电流。
16	LOSLEV	LOS灵敏度控制输入，为带40kΩ内部上拉电阻的LVTTL。置为TTL高电平或开路时为低灵敏度(高报警阈值)。置为TTL低电平时为高灵敏度(低报警阈值)。
EP	EXPOSED PAD	裸露焊盘。为获得最佳散热性能，该焊盘必须焊接在电路板的地上。

引脚配置



THIN QFN

*THE EXPOSED PAD OF THE QFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL OPERATION OF THE MAX3982.

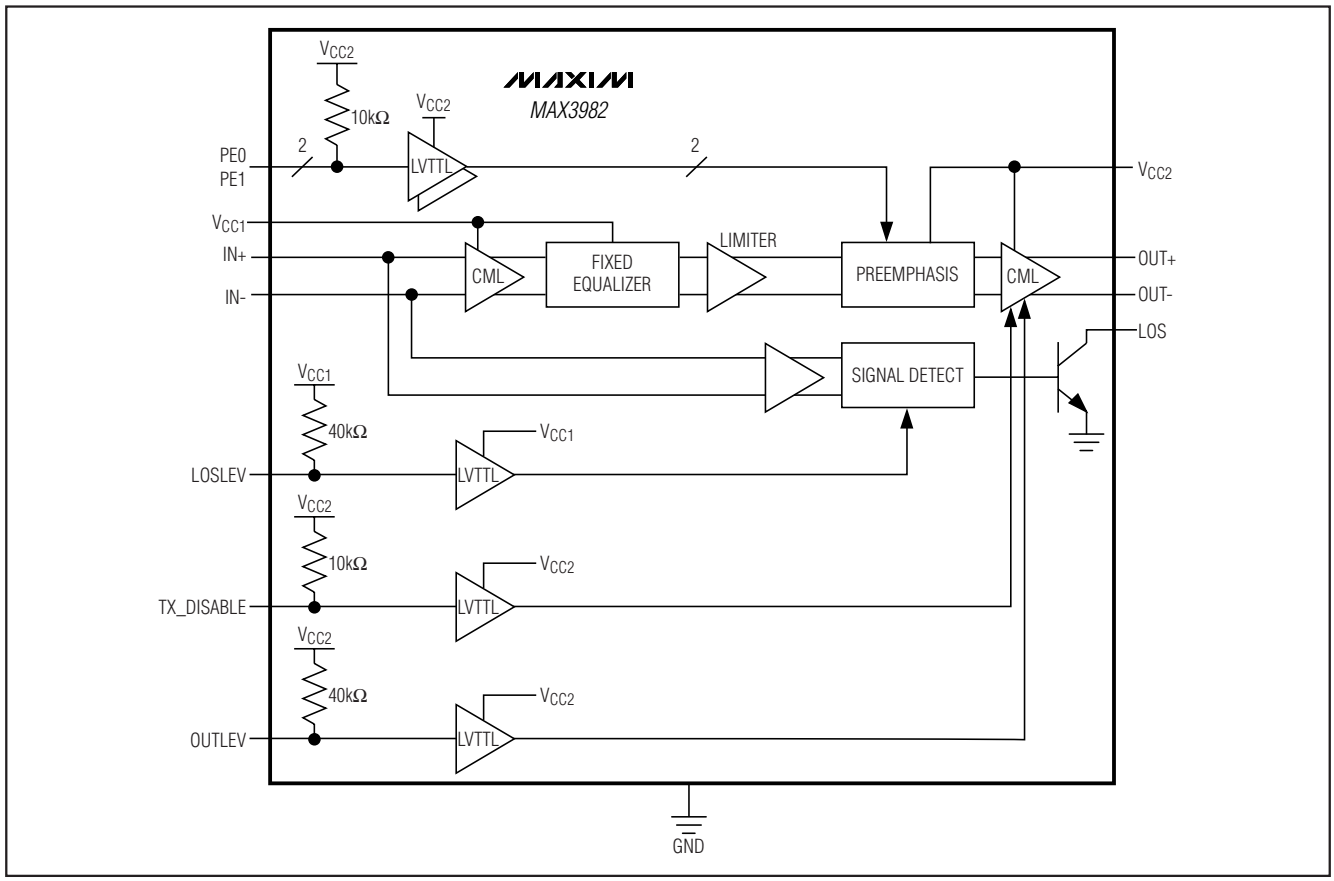


图 4. 功能框图

详细说明

MAX3982由一个PC板接收器，一个电缆驱动器和一个阈值可调的信号丢失检测器(图4)组成。接收器提供均衡功能。发送器提供可选预加重和可选输出幅度控制。MAX3982还提供禁止发送输出控制。

PC板接收器和电缆驱动器

数据通过CML输入级和固定均衡级馈入MAX3982。在4.25Gbps速率，接收器的固定均衡器可纠正10英寸的FR4 PC板损耗。

电缆驱动器含四级预加重，可补偿15米的24AWG，100Ω平衡电缆。表1是预加重表达式之间的简单转换。通过OUTLEV引脚选择输出幅度。当OUTLEV置低时，幅度为1200mV$_{P-P}$。当OUTLEV置高时，幅度为1600mV$_{P-P}$。MAX3982的剩余抖动独立于近0.20UI$_{P-P}$的源抖动。

信号丢失(LOS)输出

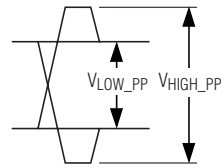
信号丢失检测根据输入数据提供。上拉电阻应将LOS接至+3.0V至+5.5V的电源。上电完成后，LOS输出才有效。典型LOS响应时间为100ns。

LOS报警和解除报警电平由LOSLEV引脚设置。当LOSLEV为LVTTL高电平或者开路时，LOS报警阈值为180mV$_{P-P}$。当LOSLEV为LVTTL低电平时，LOS报警阈值为85mV$_{P-P}$。

TX禁止

发送禁止在需要时关断输出。TX_DISABLE引脚可以连至LOS，当输入信号低于由LOSLEV设置的阈值时自动禁止输出(参见*自动检测*部分)。

表 1. 预加重转换

Ratio	α	10Gbase–CX4	IN dB	
$\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}$	$\frac{V_{HIGH\_PP} - V_{LOW\_PP}}{V_{HIGH\_PP} + V_{LOW\_PP}}$	$1 - \frac{V_{LOW\_PP}}{V_{HIGH\_PP}}$	$20\left[\log\left(\frac{V_{HIGH\_PP}}{V_{LOW\_PP}}\right)\right]$	
1.26	0.11	0.21	2	
1.58	0.23	0.37	4	
2.51	0.43	0.6	8	
5.01	0.67	0.8	14	

应用信息

自动检测

MAX3982可以自动检测输入信号并使能数据输出。自动检测功能可通过连接LOS引脚和TX_DISABLE实现。TX_DISABLE具有一个10kΩ内部上拉电阻。如果检测到信号丢失，TX_DISABLE引脚将被强制置位，并禁止输出。由于噪声可能被放大并出现不希望的输出信号，所以不推荐将MAX3982输入开路(例如，浮空)。推荐使用自动检测来消除噪声放大或可能的振荡。如果没有数据传输的时间远大于100ns，自动检测电路将禁止输出。

布线考虑

电路板布线和设计会显著影响MAX3982的性能。应尽量采用优良的高频设计技术，包括减小接地电感和对数据信号采用阻抗受控的传输线。电源去耦应尽可能地靠近V_{CC}引脚。以保证足够的电源滤波。所有V_{CC}引脚应连接到一个电源层上。注意隔离输入和输出信号以免发生串扰。

裸露焊盘封装

裸露焊盘的16引脚QFN封装为IC提供了一个热阻非常低的散热通道。MAX3982的裸露焊盘必须焊接在电路板上以获得良好的热性能。有关裸焊盘封装的更多信息，请参考Maxim应用笔记HFAN-08.1：*Thermal Considerations of QFN and Other Exposed-Paddle Packages*。

接口示意图

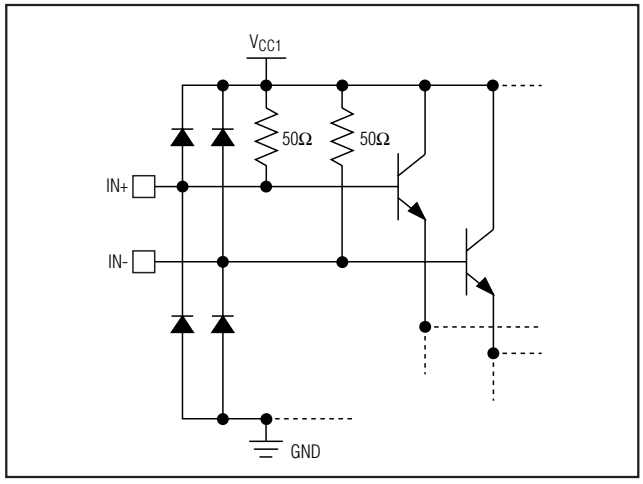


图 5. IN+/IN-等效输入结构

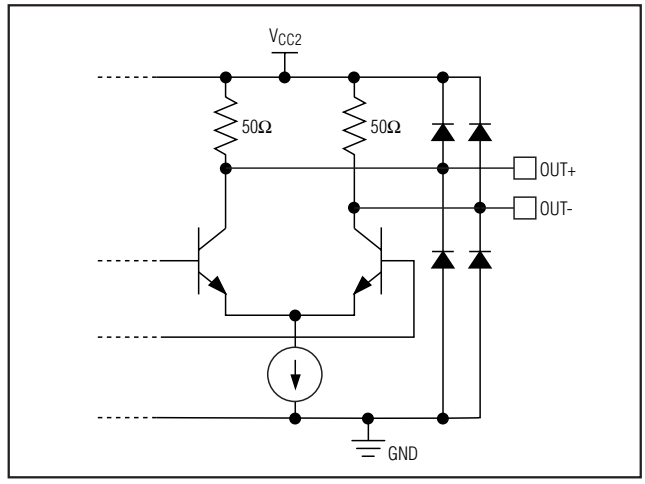
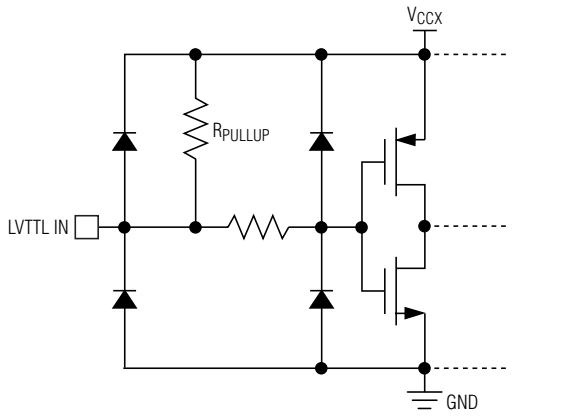


图 6. OUT+/OUT-等效输出结构



PIN NAME	V_{CCX}	R_{PULLUP} (kΩ)
LOSLEV	V_{CC1}	40
OUTLEV	V_{CC2}	40
TX_DISABLE, PE0, PE1	V_{CC2}	10

图 7. LVTTL 等效输入结构

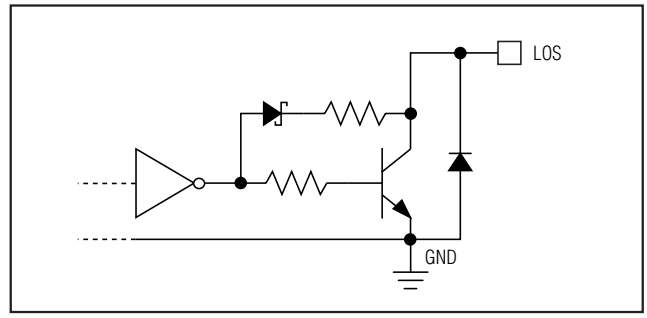


图 8. 信号丢失检测等效输出结构

芯片信息

TRANSISTOR COUNT: 2957

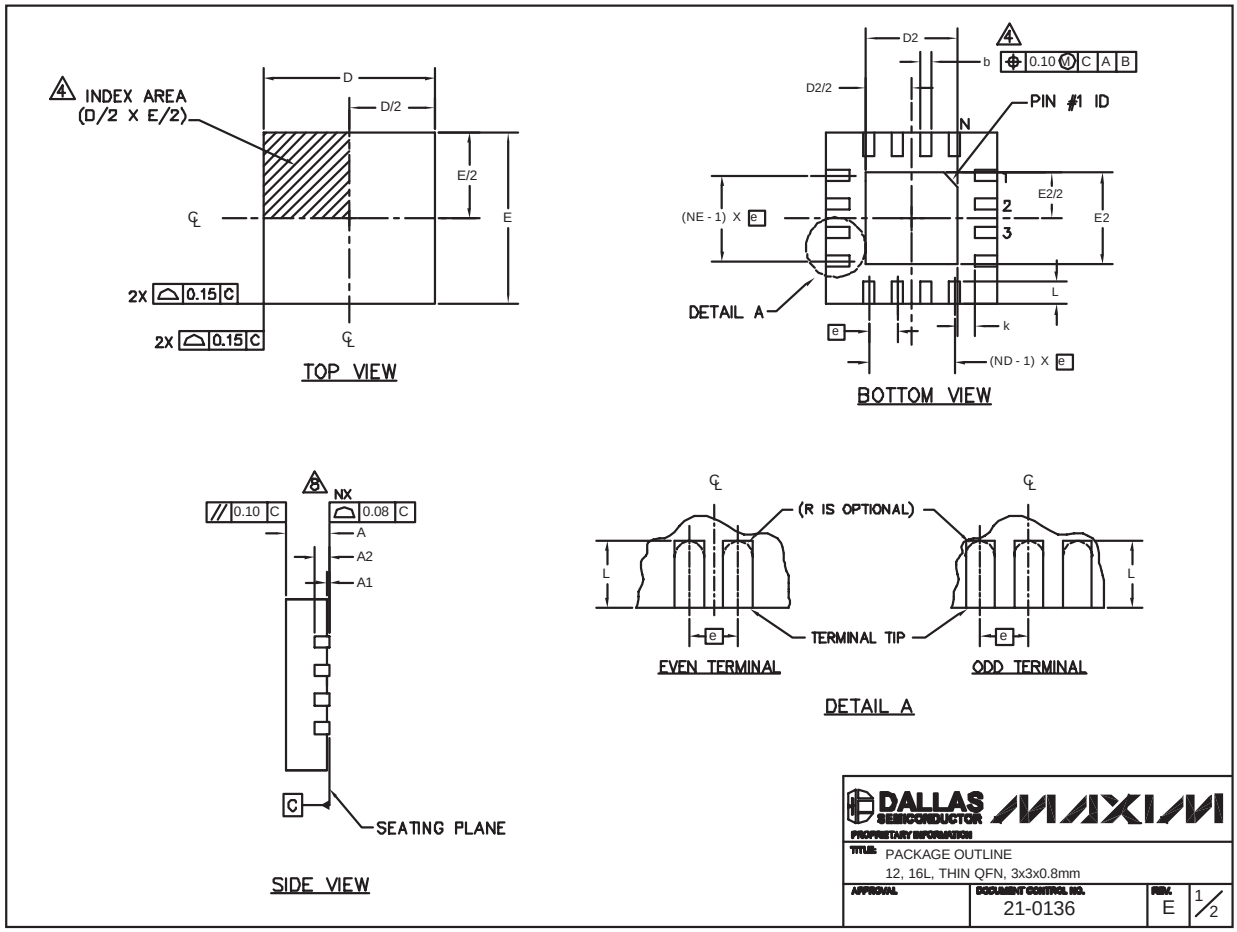
PROCESS: SiGe Bipolar

SFP铜缆预加重驱动器

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

12x16L QFN THIN.EPS



封装信息 (续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16L, THIN QFN, 3x3x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	E	2/2

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