19-2630; Rev 2; 5/04

MAXIM

6.25Gbps、1.8V PC板均衡器

概述

MAX3785为6.25Gbps均衡器，工作于1.8V单电源，用于补偿FR4传输线的传输介质损耗。MAX3785优化于线卡与开关卡之间的低电压、高密度、直流耦合连接，在保持传统的2.5Gbps至3.125Gbps速率的同时，为系统升级提供了途径。MAX3785尺寸仅相当于两个0603无源器件，提供了简单灵活的布局和布线。

MAX3785由均衡器、限幅放大器和输出驱动器组成。对于数据速率为3.2Gbps或更低的系统，MAX3785可以均衡信号，使FR4板上信号传输距离达40英寸。数据速率为6.25Gbps时，经过MAX3785补偿，信号在FR4板上可传输距离30英寸。MAX3785的工作与编码无关，对于8b/10b信号或扰码信号提供相同的性能。

MAX3785采用直流耦合电流模式逻辑 (CML)数据输入和输出，提供微型1.5mm x 1.5mm晶片级封装 (USCP™)和6引脚TDFN封装。

应用

≤ 6.4Gbps的HSBI

双IEEE 802.3ae XAUI

双STM-16/OC-48

UCSP是 Maxim Integrated Products, Inc.的商标。

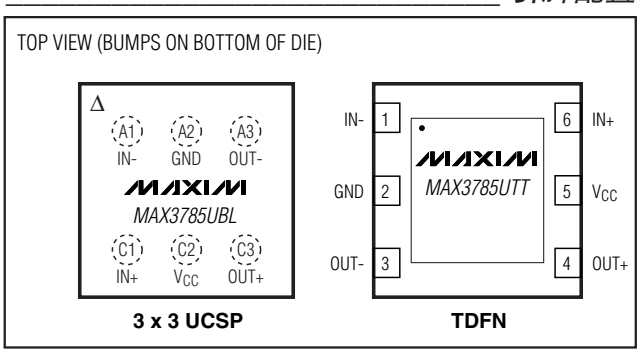
特性

- ♦ 1.8V单电源工作。
- ♦ 60mW超低功耗。
- ♦ 6.25Gbps速率下，FR4板上传输距离达30英寸。
- ♦ 工作于1.0Gbps至6.4Gbps。
- ♦ 不受编码影响，适合8b/10b或扰码信号。
- ♦ 直流耦合CML输入和输出。
- ♦ 微小的1.5mm x 1.5mm芯片面积。

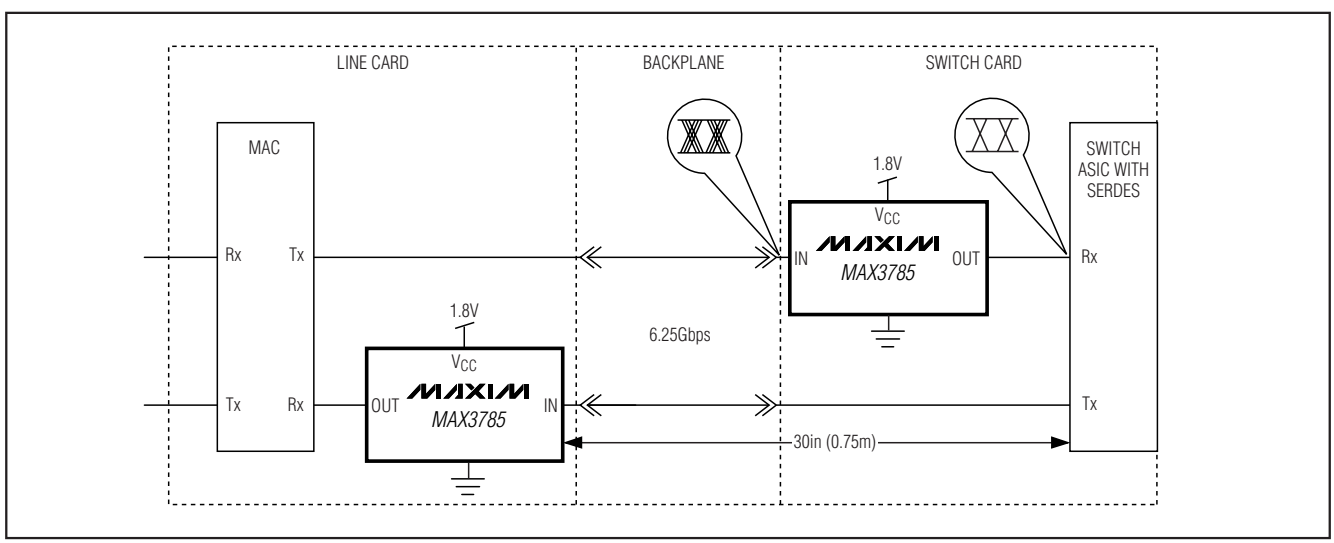
定购信息

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3785UBL	0°C to +85°C	6 UCSP (3 × 3)	—
MAX3785UTT	0°C to +85°C	6 TDFN	T633-1
MAX3785ITT	-20°C to +85°C	6 TDFN	T633-1

引脚配置



典型应用电路



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索取免费样品和最新版的数据资料，请访问 Maxim的主页：www.maxim-ic.com.cn。

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to GND.....-0.5V to +6.0V
Continuous Output Current (OUT+, OUT-).....-25mA to +25mA
Input Voltage (IN+, IN-).....-0.5V to (V_{CC} + 0.5V)
Operating Ambient Temperature Range
(UBL, UTB)..... 0°C to +85°C
Operating Ambient Temperature Range (ITT).....-20°C to +85°C
Storage Ambient Temperature Range.....-55°C to +150°C
Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 24.4mW above +70°C).....1.95W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Typical values measured at V_{CC} = 1.8V and T_A= +25°C. Specifications guaranteed over specified operating conditions.) (See *Operating Conditions* table.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			35	55	mA
Input Swing (IN)	Measured differentially at data source before encountering loss (Point A in Figure 1) (Note 1)	400		1600	mV_{P-P}
Input Common-Mode Voltage Range	(Note 1)	V_{CC} - (IN_{MAX}/4)		V_{CC} - (IN_{MIN}/4)	V
Input Return Loss	100MHz to 3.2GHz, power off		15		dB
Differential Input Resistance	IN+ and IN-	85	100	115	Ω
Output Swing	Measured differentially at OUT+ and OUT- with 50Ω ±1% load at each side	450		800	mV_{P-P}
Output Resistance	OUT+ or OUT-	42	50	58	Ω
Output Return Loss	100MHz to 3.2GHz, IN+ = high		14		dB
Output Transition Time (t_r, t_f)	20% to 80% (Note 2)	30	40	55	ps
Residual Deterministic Jitter (Notes 1, 3, 4)	2.5Gbps, 3.2Gbps, 5.0Gbps; 0in to 30in FR4 $400mV_{P-P} \le IN \le 1600mV_{P-P}$		0.10	0.15	UI
	2.5Gbps, 3.2Gbps; 40in FR4 $400mV_{P-P} \le IN \le 1600mV_{P-P}$		0.15	0.20	
	6.25Gbps; 0in to 30in FR4 $600mV_{P-P} \le IN \le 1600mV_{P-P}$		0.15	0.25	
	6.25Gbps; 0in to 30in FR4 $IN = 400mV_{P-P}$		0.20	0.30	
Output Random Jitter	(Notes 1, 2)		0.75	1.0	ps_{RMS}
Low-Frequency Cutoff Frequency			50		kHz
Latency			200		ps
Maximum Bit Rate	(Note 1)	6.25	6.4		Gbps
Minimum Bit Rate	(Note 1)		1.0	2.5	Gbps

Note 1: Guaranteed by design and characterization.

Note 2: Using input pattern 0000011111 at 6.25Gbps.

Note 3: Difference in deterministic jitter between data source and equalizer output, evaluated at 2.5Gbps, 3.2Gbps, 5Gbps, and 6.25Gbps. Pattern used: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1.

Note 4: Signal is applied differentially at input to a 6-mil wide, loosely coupled stripline. Deterministic jitter at the output of the transmission line is from media-induced loss, not from clock source modulation (see Figure 1).

工作条件

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		1.71	1.8	1.89	V
Operating Ambient Temperature (UBL, UTT)		0	25	85	°C
Supply Noise Tolerance	10Hz ≤ f < 100Hz		100		mV_{P-P}
	100Hz ≤ f < 1MHz		40		
	1MHz ≤ f ≤ 1GHz		10		
Bit Rate	NRZ data	2.50		6.25	Gbps
Operating Ambient Temperature (ITT)		-20	25	85	°C

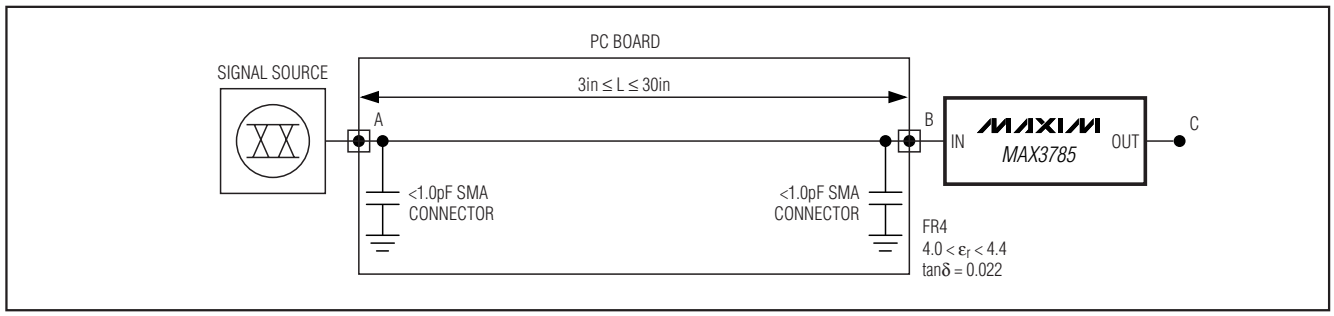
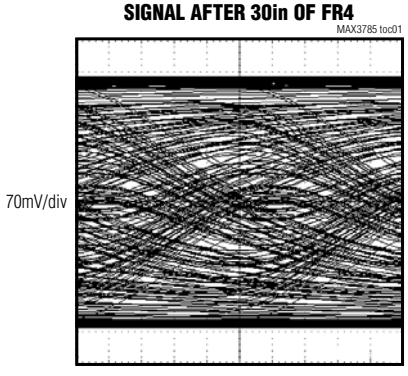


图 1. 测试条件

典型工作特性

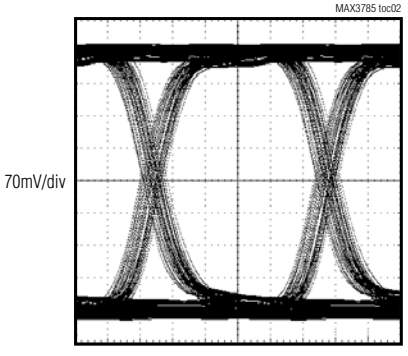
(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV_{P-P} at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan™. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

EYE DIAGRAM OF UNEQUALIZED SIGNAL AFTER 30in OF FR4



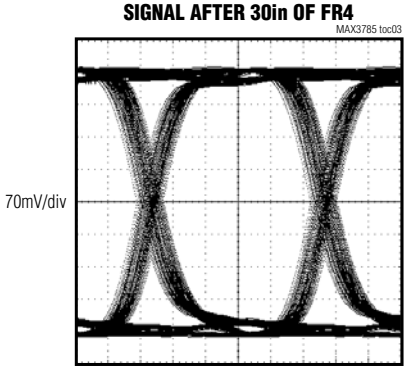
TEST PATTERN, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



TEST PATTERN, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



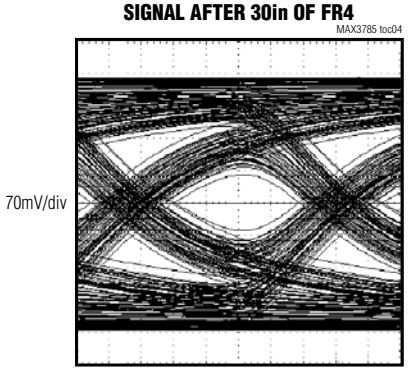
2^{10} - 1 PRBS, 6.25Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

FrameScan 是 Tektronix 的商标。

典型工作特性 (续)

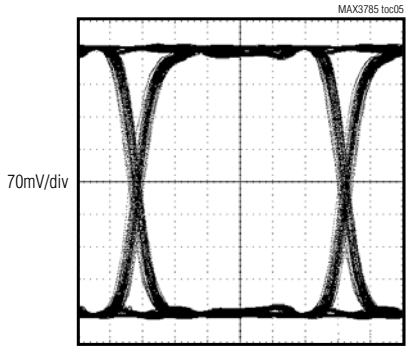
(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV$_{P-P}$ at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

EYE DIAGRAM OF UNEQUALIZED SIGNAL AFTER 30in OF FR4



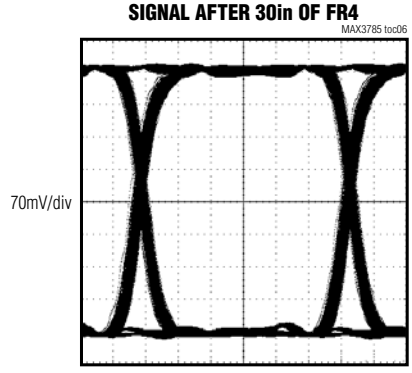
TEST PATTERN, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4



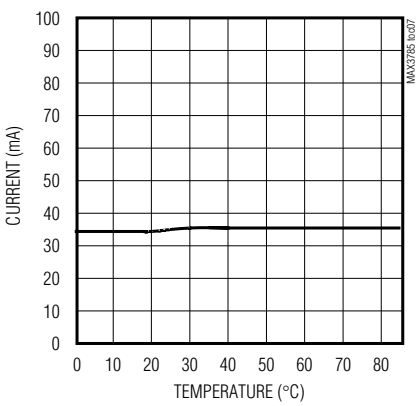
TEST PATTERN, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

EYE DIAGRAM OF EQUALIZED SIGNAL AFTER 30in OF FR4

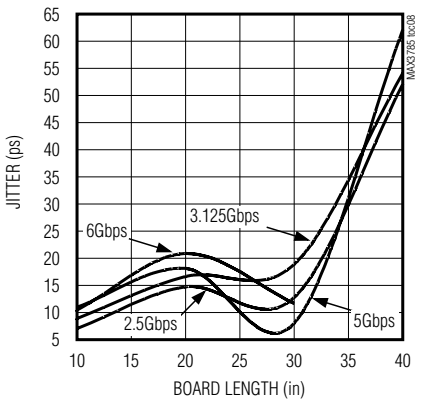


CRPAT, 3.125Gbps,
WITHOUT RANDOM JITTER,
INCLUDING 13ps SYSTEM JITTER

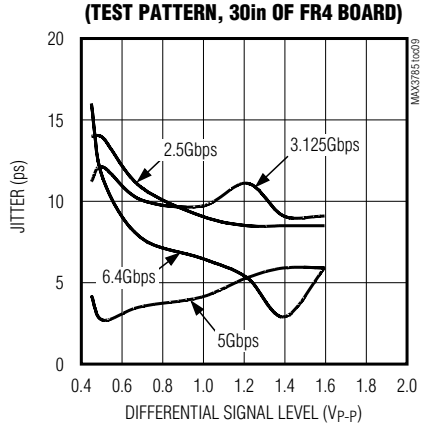
EQUALIZER OPERATING CURRENT vs. TEMPERATURE



DETERMINISTIC JITTER vs. BOARD LENGTH (FR4) (INPUT LEVEL OF 500mV$_{P-P}$, TEST PATTERN)



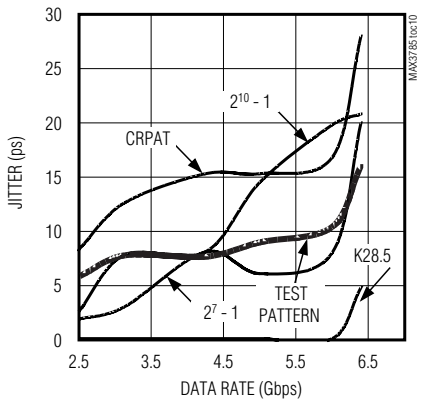
DETERMINISTIC JITTER vs. SIGNAL LEVEL (TEST PATTERN, 30in OF FR4 BOARD)



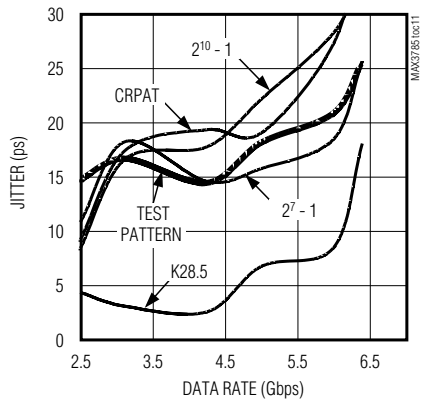
典型工作特性 (续)

(V_{CC} = +1.8V, T_A = +25°C, unless otherwise noted. Measurements done at 6.25Gbps, 500mV$_{P-P}$ at the source with a test pattern: PRBS (2^7), ninety-six 0s, 1, 0, 1, 0, PRBS (2^7), ninety-six 1s, 0, 1, 0, 1. Deterministic jitter of the MAX3785 and the board was measured using Tektronix's FrameScan. Deterministic jitter of the system was subtracted from the measured value. Eye diagrams were acquired by FrameScan, which includes system jitter but eliminates random jitter.)

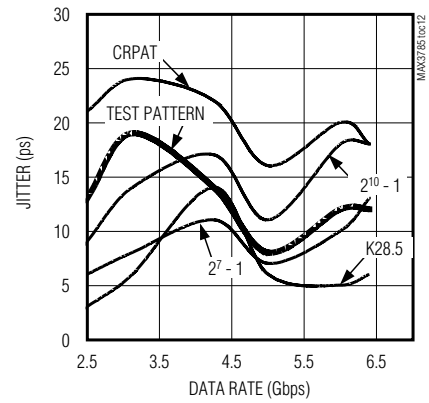
DETERMINISTIC JITTER vs. DATA RATE FOR 10in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



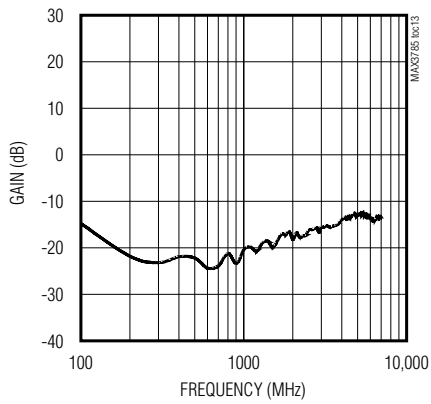
DETERMINISTIC JITTER vs. DATA RATE FOR 20in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



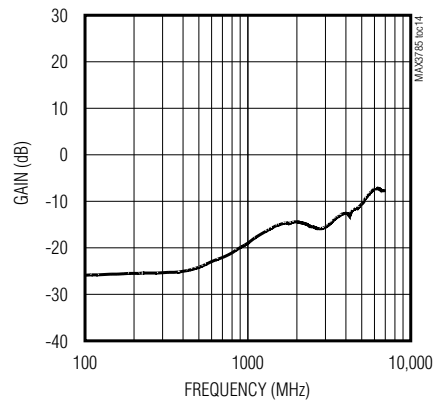
DETERMINISTIC JITTER vs. DATA RATE FOR 30in OF FR4 BOARD (INPUT LEVEL OF 500mV$_{P-P}$)



EQUALIZER INPUT RETURN GAIN (SDD11) (INPUT SIGNAL LEVEL = -40dBm, POWER OFF)



EQUALIZER INPUT RETURN GAIN (SDD22) (INPUT SIGNAL LEVEL = -40dBm, IN+ HIGH)



MAX3785UBL引脚说明

引脚	名称	功能 (MAX3785UBL)
A1	IN-	数据输入负端，CML。
A2	GND	电源地
A3	OUT-	数据输出负端，CML。
C1	IN+	数据输入正端，CML。
C2	V_{CC}	电源电压
C3	OUT+	数据输出正端，CML。

功能说明

MAX3785 6.25Gbps PC板均衡器由均衡器、限幅放大器、补偿驱动器和消偏差电路 (见图2)组成。均衡电路对PC板产生的衰减进行补偿。限幅放大器将均衡器输出转换成方波。消偏差电路对限幅放大器的内部失调进行校准，使脉宽失真最小。这将引入低频截止。数据在不到100µs内必须达到50%的符号/间隔比。为避免自激振荡，必须保持规定的最小差分输入。

输入、输出结构

等效直流输入电路如图3所示，等效直流差分输入阻抗为100Ω。输出缓冲器采用电流模式逻辑 (CML)，如图4所示。

封装说明

晶片级封装具有0.5mm (19.7mil)的焊球间隔及0.3mm (12mil)的焊球直径。焊盘布局间隔为0.5mm (19.7mil)，焊盘尺寸为 0.25mm (10mil)，掩膜开口0.33mm (13mil)。允许采用圆形或方形焊盘。有关UCSP布局及处理的详细信息，请登录Maxim网站www.maxim-ic.com.cn查询。封装说明在资料发布时是准确的。对于MAX3785，图中B行所示的所有焊球没有安装在芯片上 (空缺)。要获取最新的封装信息，请访问Maxim网站。

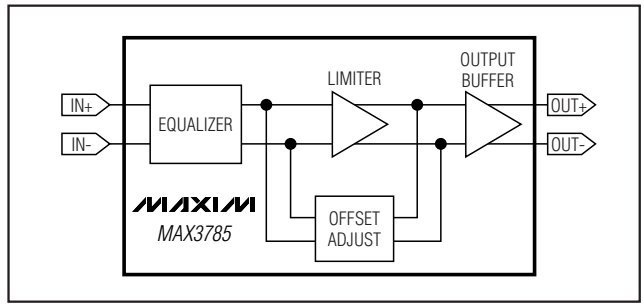


图 2. MAX3785的功能框图

MAX3785UTT引脚说明

引脚	名称	功能 (MAX3785UTT)
1	IN-	数据输入负端 (CML)
2	GND	电源地
3	OUT-	数据输出负端 (CML)
4	OUT+	数据输出正端 (CML)
5	V_{CC}	电源电压
6	IN+	数据输出正端 (CML)

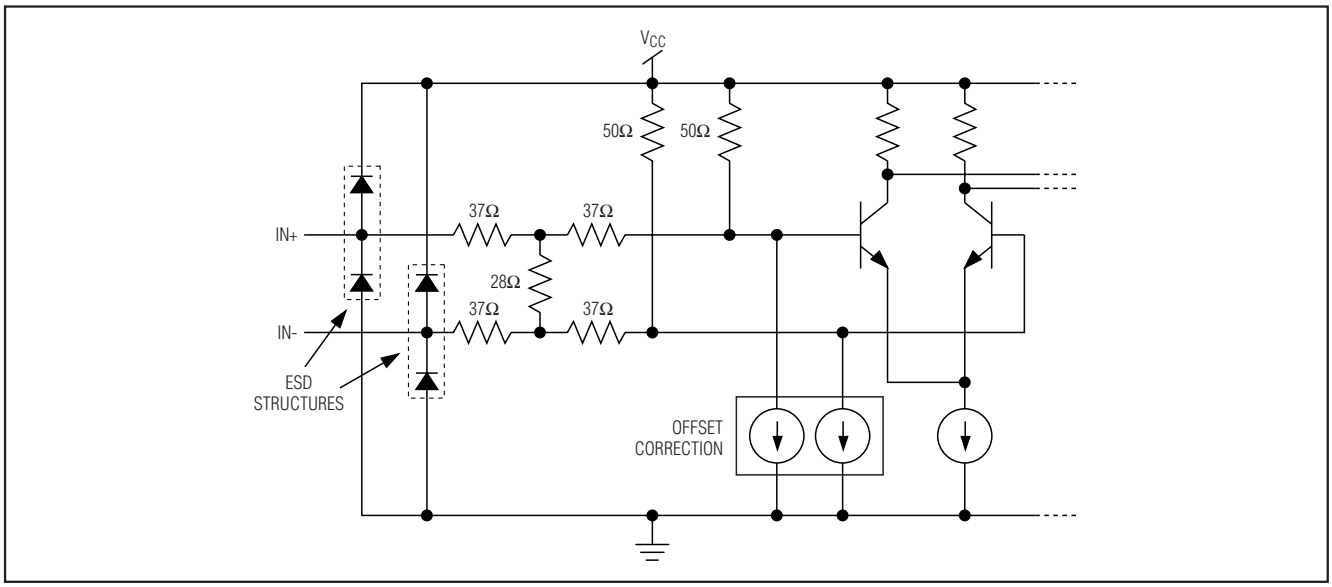


图 3. 均衡器输入直流等效电路

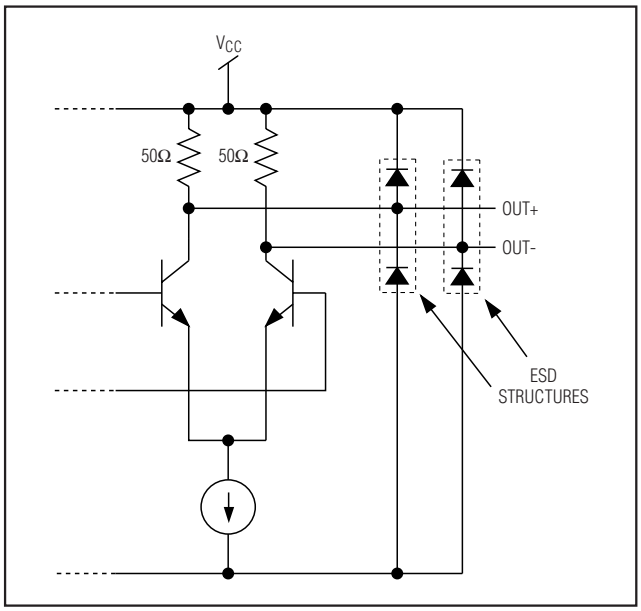
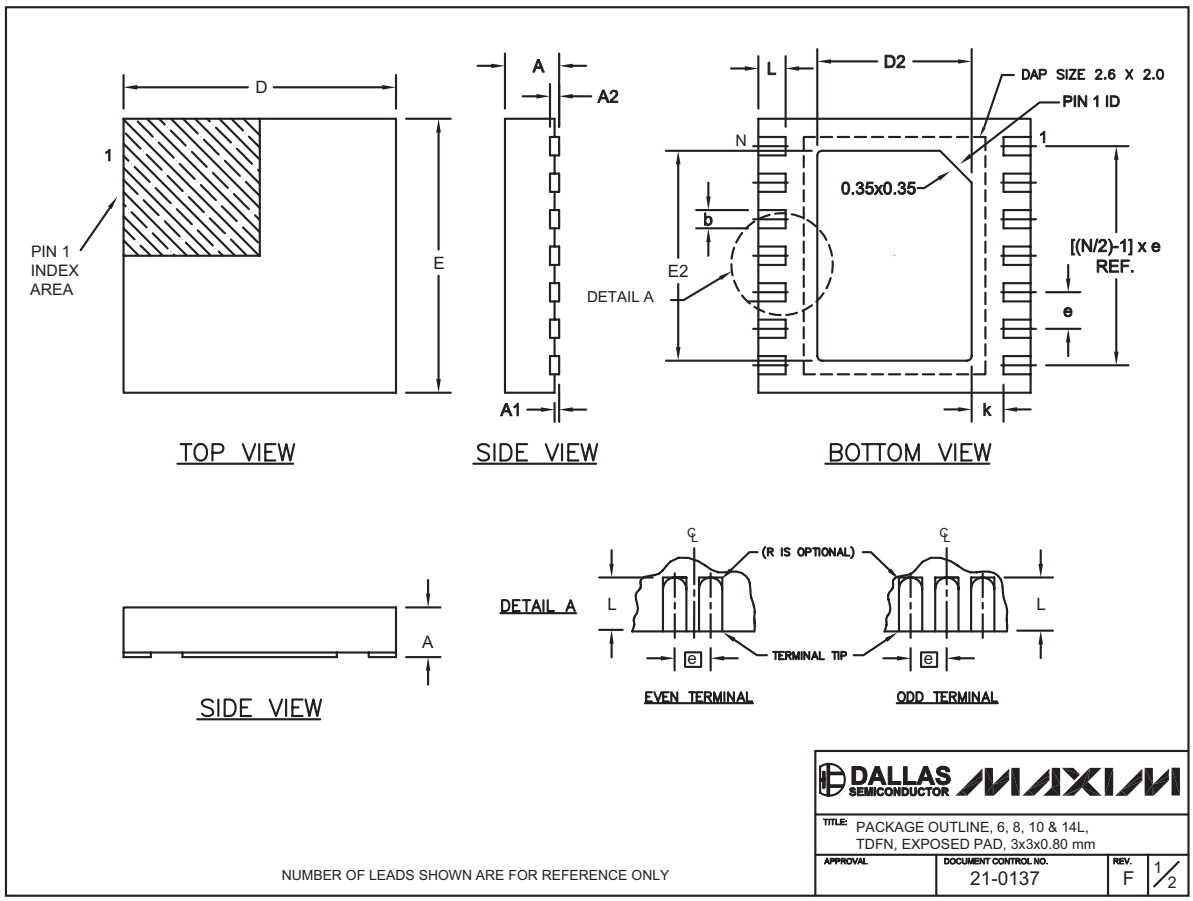


图 4. CML输出等效电路

6.25Gbps、1.8V PC板均衡器

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)



封装信息 (续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.03	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.03	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.

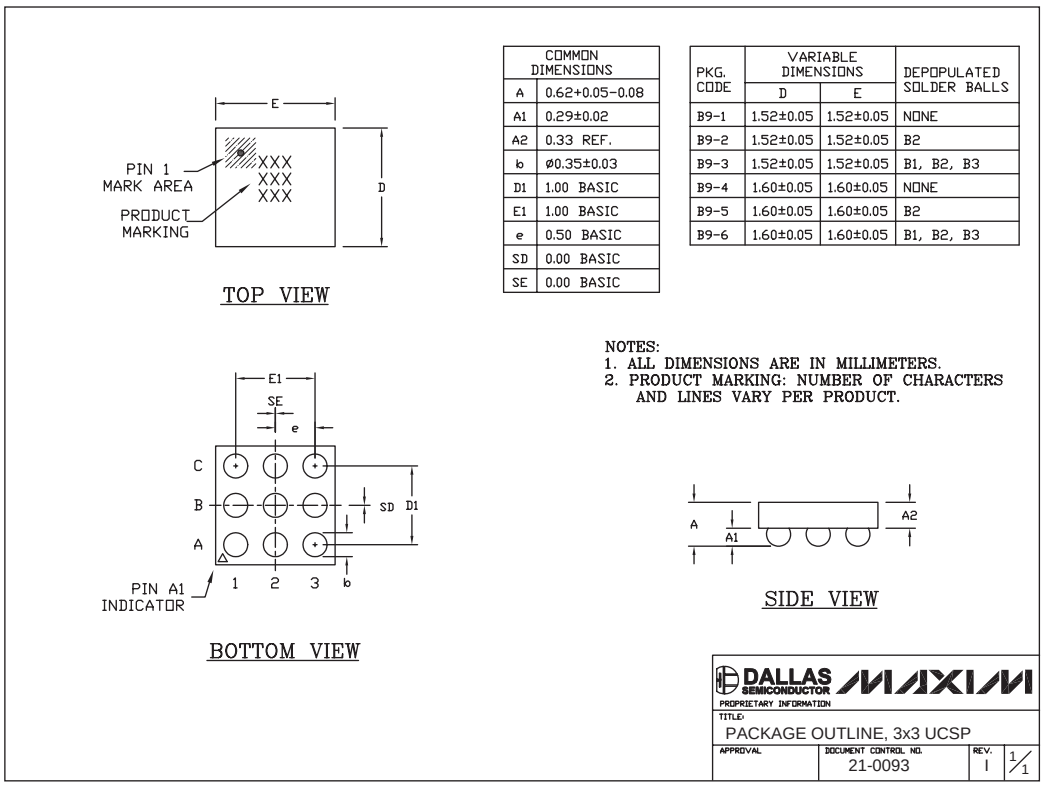
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	F	2/2

封装信息 (续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)



COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3

注：对于MAX3785，没有安装图中位于B行的全部焊球。

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