电流反馈运算放大器的直流性能（V_{OS}、CHR等）要比精密电压反馈运算放大器差，但是电流反馈放大器的交流性能要比电压反馈放大器好。例如，电流反馈放大器的频带要比电压反馈放大器高，尤其是0.1dB的信号频率平坦度及相位变化，电流反馈放大器要比电压反馈放大器好得多，甚至不是同一数量级的比较。

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2、电流反馈运算放大器应用中应注意的几个问题

电流反馈运算放大器和电压反馈运算放大的使用方法基本相同，但由于放大器内部结构的差异，因此，使用时要注意这种差别，正确选择放大器的类型。以下介绍使用中应注意的几个问题。

2.1 同相放大器的应用

不论是电压反馈运算放大器还是电流反馈运算放大器，都适用于同相放大器。

在应用电压反馈运算放大器时，闭环带宽不仅决定于反馈电阻 R_F，而且还决定于增益电阻 R_G。对于电流反馈运算放大器，闭环带宽仅决定于反馈电阻 R_F，改变增益电阻 R_G 时，不改变电路的闭环带宽。闭环带宽的的一阶响应是随着反馈电阻 R_F 的变化而变化。

2.2 反相放大器的应用

当运算放大器用于反相放大器时，由于内部结构的不同，选用时是有区别，尤其是多输入端电压反馈放大器的传递函数会有明显的变化，如图3所示。

2.3 电压跟随器的应用

电压跟随器是同相输入放大器的一个特例。电压跟随器的增益为1。放大器内部结构决定了由电流反馈放大器组成电压跟随器时，放大器的输出端不能直接与反相输入端短接，而必须通过一个电阻才能连接，见图4电路。

这是由于输出端与反相输入端直接连接时，相当于输出短路，会使电流反馈运算放大

表1　电压反馈运算放大器和电流反馈运算放大器几项主要参数比较

		单位	电压反馈运算放大器			电流反馈运算放大器			
			AD854	AD847	AD817	AD811	AD846	AD9618	ADEL2020
输入失调电压		mV	0.25	0.5	0.5	0.5	25μV	0.5	1.5
输入失调电流			25pA	50mA	50nA	2μA			
输入阻抗	输入阻抗	Ω	10^{11}	3×10^{5}	3×10^{4}				
	输入电容	pF	4.0	1.5	1.5				
	同相输入	Ω				15×10^{5}	10^{4}	75×10^{3}	10^{7}
	反相输入	Ω				14	50	75×10	40
输入偏置电流	同相(典型值)	nA	0.75	3300	3300	200	3000	5000	1000
	反相(典型值)	nA	0.75	3300	3300	200	150	0	500
小信号单位增益带宽		MHz	16	50	50	140	80	160	90
0.1dB信号平坦度		MHz				35			25
转换速率		V/μs	20	300	300	2500	450	1800	500
电压噪声		nV/$\sqrt{Hz}$	80	15	15	1.9	20	1.2	2.9
互阻抗		MΩ				1.5	200		3.5
共模抑制		dB		95	95	66			64
共模抑制比		dB					125	52	

●应用经验

电流反馈运算放大器与电压反馈运算放大器的区别与应用

西安英世模拟器件有限责任公司 张强

摘要：本文介绍了电流反馈运算放大器与电压反馈运算放大器的区别及其有关的增益表达式，并且列举了几个应用实例，说明如何选用运算放大器。

关键词：电流反馈 电反馈 频率平坦度

运算放大器是应用最广的集成电路。根据运算放大器不同的特性，它能满足高精度、高频率的要求，并且应用方便。但是如何正确选择与使用运算放大器，这是设计电路时十分关注的问题。

运算放大器按照反馈信号类型进行分类，可以分为电压反馈运算放大器和电流反馈运算放大器两大类。本文对它们之间的区别及如何正确使用电流反馈运算放大器进行简单介绍，供广大读者参考。

1、电流反馈运算放大器和电压反馈运算放大器的区别

电流反馈运算放大器和电压反馈运算放大器是二种不同反馈信号的运算放大器，基本区别如下：

1.1 输入极结构不同

电压反馈运算放大器的同相输入端与反相输入端不仅结构基本相同，而且输入阻抗基本相同。在差动输入模式和共模形式下。输入阻抗一般都在10Ω以上。而电流反馈运算放大器的输入端是一个连接同相输入端与反相输入段的单位增益缓冲器。同相输入端与反相输入端输入阻抗相差极大。同相输入端的输入阻抗一般在10Ω以上，反相输入端的输入阻抗在理想状态下为0，实际上有几十欧输入阻抗。因此对于输入阻抗的表达方式也是不同的。

进行交流分析时，原理框图如图1所示。

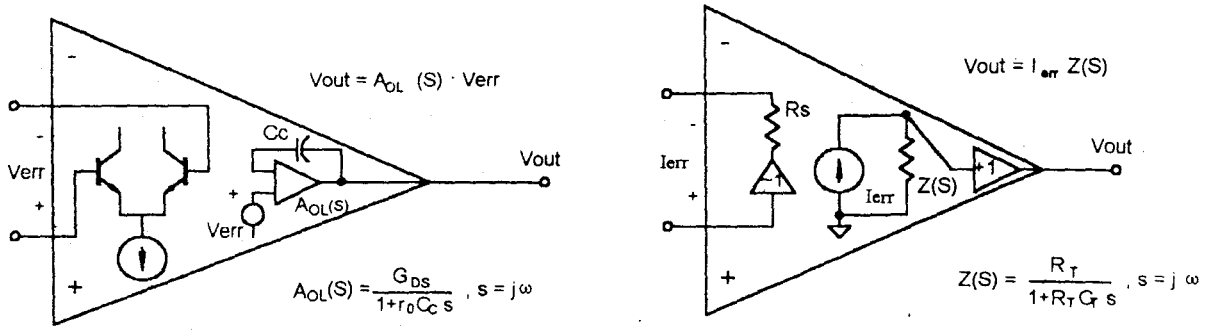
1.2 影响运算放大器带宽因素不同

电压反馈运算放大器开环时，输出电压等于开环增益A_{OL}与输入的偏差电压$Verr$的积

$$Vout = A_{OL(S)}\,Verr \qquad (1)$$

式中 $$A_{OL}(S)=\frac{G_{DC}}{1+\gamma_O C_{CS}} \quad S=j\omega \qquad (2)$$

G_{DC}：直流开环增益



a 电压反馈运算放大器交流分析框图　　b 电流反馈运算放大器交流分析框图

图1 运算放大器交流分析框图

γ_O：开环方程中的有效阻抗

C_C：补偿电容。

补偿电容不仅影响放大器的稳定性，而且决定了放大器的转换速率。

当接成同相输入的闭环电路时，电压反馈运算放大闭环增益为：

$$V_O = (V_{in+} - V_{in-}) A_{OL}(S) \quad (3)$$

$$V_{in} = \frac{R_G}{R_G + R_F} V_O \quad (4)$$

运算后，化简得到：

$$\frac{V_O}{V_{in}} = \left[1 + \frac{R_F}{R_G}\right] \frac{1}{1 + \frac{1}{L_G}} \quad (5)$$

$$L_G = \frac{A_{OL}(S)}{1 + \frac{R_F}{R_G}} \quad (6)$$

L_G：闭环状态下的环路增益

因此，影响电压反馈运算放大器的闭环增益，不仅是开环增益 AOL(S)，而且还有反馈电阻 R_F 和增益电阻 R_G。

在低频时，由于开环增益非常大，可以忽略开环增益的影响。当频率增高时，$A_{OL(S)}$ 开始以 20dB/10 倍频速率下降，最终会成为影响电路增益的主要因素。

电流反馈运算放大器，在开环时，它的输出电压等于开环阻抗 Z(S) [Transimpedance] 和输入误差电流 $Ierr$ 乘积。

$$V_{out} = Ierr\ Z(S) \quad (7)$$

$$Z(S) = \frac{R_T}{1 + R_T C_T S} \quad S = j\omega \quad (8)$$

R_T：直流开环互阻抗

C_T：镜像电流源控制转换速率的补偿电容

电流反馈放大器的转换速率，由 C_T 和放大器的内部残余电流决定。

当连接成同相的闭环形式时，电流反馈放大器的闭环增益表达式：

$$\frac{V_O - V_{in-}}{R_T} + \frac{-V_{in}}{R_G} + Ierr = 0 \quad (9)$$

$$Ierr = V_O / Z(S) \quad (10)$$

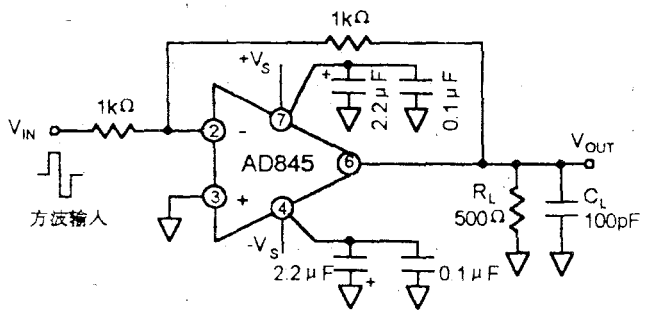
将式(10)代入式(9)，化简后得到：

$$\frac{V_O}{V_{in+}} = \left[1 + \frac{R_F}{R_G}\right] \frac{1}{1 + \frac{1}{L_G}} \quad (11)$$

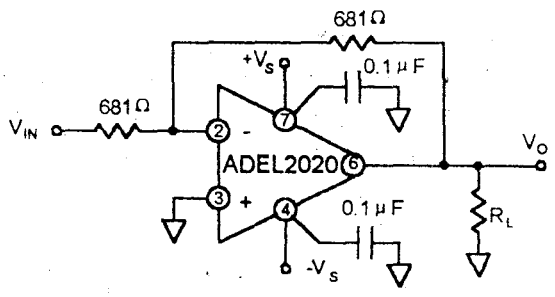
$$L_G = \frac{Z(S)}{R_F} \quad (12)$$

在闭环电路中，电流反馈运算放大器的传递函数表达式(11)和电压反馈运算放大器的传递函数表达式(5)是相同的，但是电流反馈运算放大器的闭环增益表达式(12)与电压反馈运算放大器的闭环增益表达式(6)是不同的。影响电流反馈运算放大器的闭环增益除了放大器本身的互阻抗 Z(S)外，只有反馈电阻 R_F 一个因素。因此对于电流反馈运算放大器，当反馈电阻 R_F 确定之后，改变增益电阻 R_G，不影响电路的闭环频带，而对于电压反馈运算放大器不改变反馈电阻 R_F，只改变增益电阻时，也影响电路的闭环频带。

1.3 交直流性能不同



a. 电压反馈放大器的同相增益电路



b. 电流反馈放大器的同相增益

图 2 运算放大器同相输入时增益电路图

电流反馈运算放大器的直流性能（V_{OS}、CHR等）要比精密电压反馈运算放大器差，但是电流反馈放大器的交流性能要比电压反馈放大器好。例如，电流反馈放大器的频带要比电压反馈放大器高，尤其是0.1dB的信号频率平坦度及相位变化，电流反馈放大器要比电压反馈放大器好得多，甚至不是同一数量级的比较。

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2.3 电压跟随器的应用

电压跟随器是同相输入放大器的一个特例。电压跟随器的增益为1。放大器内部结构决定了由电流反馈放大器组成电压跟随器时，放大器的输出端不能直接与反相输入端短接，而必须通过一个电阻才能连接，见图4电路。

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输入失调电流			25pA	50mA	50nA	2μA			
输入阻抗	输入阻抗	Ω	10^{11}	3×10^{5}	3×10^{4}				
	输入电容	pF	4.0	1.5	1.5				
	同相输入	Ω				15×10^{5}	10^{4}	75×10^{3}	10^{7}
	反相输入	Ω				14	50	75×10	40
输入偏置电流	同相(典型值)	nA	0.75	3300	3300	200	3000	5000	1000
	反相(典型值)	nA	0.75	3300	3300	200	150	0	500
小信号单位增益带宽		MHz	16	50	50	140	80	160	90
0.1dB信号平坦度		MHz				35			25
转换速率		V/μs	20	300	300	2500	450	1800	500
电压噪声		nV/$\sqrt{Hz}$	80	15	15	1.9	20	1.2	2.9
互阻抗		MΩ				1.5	200		3.5
共模抑制		dB		95	95	66			64
共模抑制比		dB					125	52	

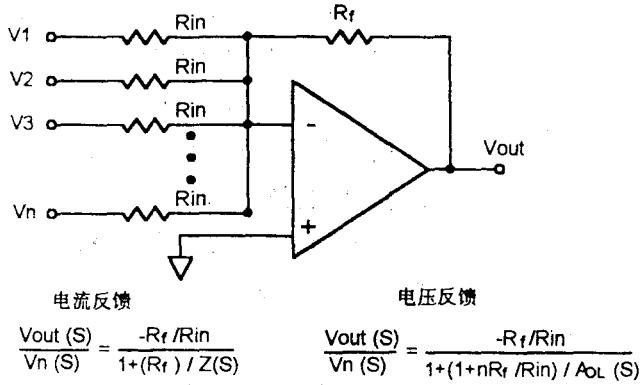


图 3 多输入端放大器原理图

器内部产生过热和过流保护，器件无输出电压。所以必须串入一个电阻，该电阻的典型值为 1kΩ 以上。

值得指出的是，在电压跟随器情况下，输出端与反相输出端之间接入一个电阻并非是电流反馈放大器独有的特点，输入阻抗很低的高频电压反馈放大器也应串入一个电阻才能正常使用。

2.4 利用反接光敏二极管构成互阻放大器

在电路图 5 中，当改变反馈电阻 R_F 时，就改变了电路增益。当采用电压反馈放大器时，在高频时改变 R_F 通常不影响电路的带宽。这是由于闭环增益主要由输入电容和反馈电容决定，使闭环增益与开环增益可能在预定点相交。如果采用电流反馈放大器，当改变 R_F 时，就会改变电路的带宽，使得电路的带宽随增益的变化而改变。另一方面，电流反馈放大器的反相输入端电流噪声要比电

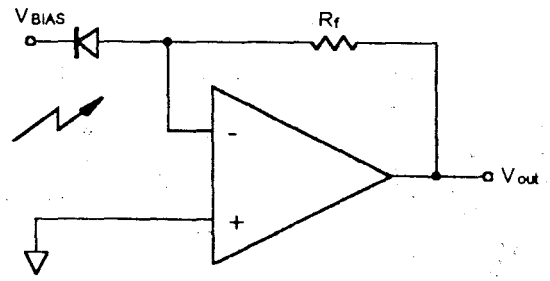


图 5 利用光敏二极管构成的互阻放大器

压反馈放大器大。因此，在图 5 中，应该采用电压反馈放大器。

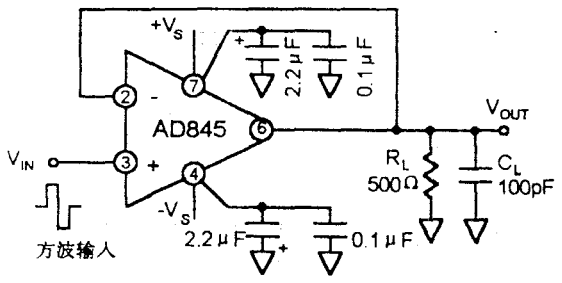
2.5 多功能滤波器

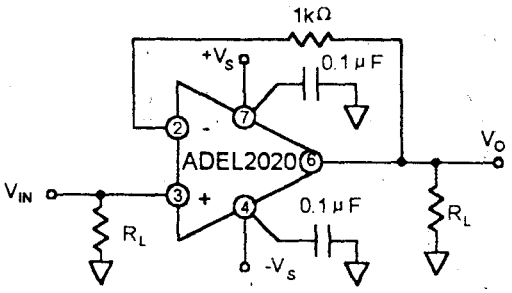
利用 4 个运算放大器和辅助元件，可构成一个有高通、低通和带通的多功能滤波器，原理图如图 6 所示。

在电路中，A2 和 A3 是积分器，应选用精密电压反馈运算放大器，如果选用电流反馈运算放大器的话，在反馈回路中，单独的电容元件(无任何串联电阻)将使电路工作不稳定。R1 和 R6 分别调节 A1 和 A4 的增益。调节增益时，既不能影响频带，又要保证能够独立调整，因此，选用电流反馈运算放大器最合适。这样使电路具有更高的频带，这一点对于 A1 来讲是很关键的。

3、结论

应用时，应该根据实际电路很好地选用运算放大器，使电路的各项性能指标得到充分的体现。如果要求电路有比较高的闭环增





a. 电压反馈运算放大器的电压跟随器原理图　　b. 电流反馈运算放大器的电压跟随器的原理图

图 4 不同类型运算放大器组成的电压跟随器原理图

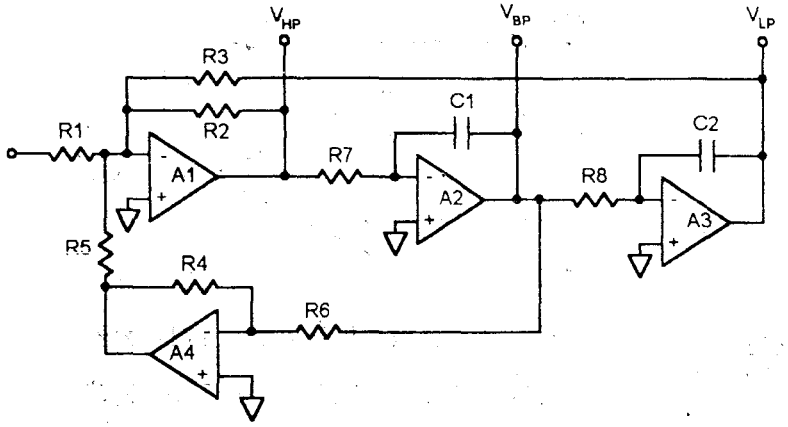


图6 具有高通,低通和带通输出二阶状态可变滤波器

益，则选用电流反馈运算放大器。如果即要求电路在高频状态有高的闭环增益，很好的频率平坦度，又要保证调整闭环增益不影响电路频带，则选用AD811、AD8011、AD812等视频电流反馈运算放大器比较好。电流反馈放大器在闭环宽频带范围内有较低的增益偏差。电压反馈运算放大器在闭环低增益情况下，性能比较好，在高增益情况时，会降低精度和带宽指标。在差动输入电路中，一般选用电压反馈运算放大器，这是由于电压反馈运算放大器的共模抑制比要比电流反馈运算放大器高。

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咨询编号：970301

编者注：本文由英世集团特约刊登，关于AD公司运算放大器的咨询请直接与该公司联系，具体地址参见中插广告。

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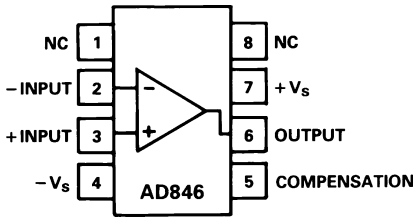
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/√Hz

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Plastic SOIC (A) Package
- MIL-STD-883B Part Available

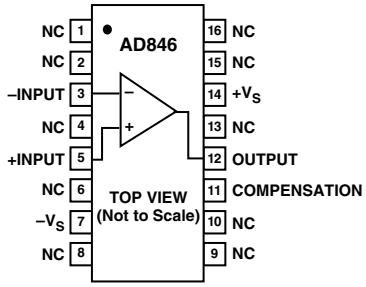
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



NC = NO CONNECT
TOP VIEW

SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from –1 to gains greater than –100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of –40°C to +85°C. The AD846S is rated over the full military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

The AD846 is available in two types of 8-lead packages: plastic mini-DIP and hermetic cerdip. The AD846AR-16 is available in the 16-lead SOIC package. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of –1 to –10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of –1 to –100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
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AD846–SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**200**		25	**75**		25	**200**	µV
T_{MIN}–T_{MAX}			50	350		50	**125**		100	**350**	µV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	µV/°C
vs. Supply (PSRR)	5 V–18 V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{MIN}–T_{MAX}		110	120		**116**	120		**94**	116		dB
vs. Common Mode (CMRR)	V_{CM} = ±10 V										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{MIN}–T_{MAX}		110	120		**116**	120		**94**	116		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	**450**		100	**250**		150	**450**	nA
T_{MIN}–T_{MAX}			450	1200		400	**750**		1000	**1500**	nA
vs. Temperature			6	20		6	**17**		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	**15**		9	**10**		9	**15**	nA/V
T_{MIN}–T_{MAX}			11	20		11	**15**		11	**25**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{MIN}–T_{MAX}			5	15		3	**7**		5	**20**	nA/V
+Input Bias Current											
Initial			3	**15**		3	**5**		3	**15**	µA
T_{MIN}–T_{MAX}			4	20		4	**7**		5	**20**	µA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	**15**		5	**10**		5	**15**	nA/V
T_{MIN}–T_{MAX}			5	20		5	**15**		5	**20**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{MIN}–T_{MAX}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/$\sqrt{\text{Hz}}$
Input Current Noise											
–Input	1 kHz		20			20			20		pA/$\sqrt{\text{Hz}}$
+Input	1 kHz		6			6			6		pA/$\sqrt{\text{Hz}}$
OPEN LOOP											
TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	**100**	200		**150**	200		**100**	200		MΩ
	T_{MIN}–T_{MAX}	50			**75**			**50**			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**±10**			**±10**			**±10**			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = –1 R_F = 1k		80			80			80		MHz
(–3 dB)	A_V = –10 R_F = 875 Ω		31			31			31		MHz
	A_V = –30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p-p										
	R_L = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = –1		110			10			10		ns
Overshoot	A_V = –1		20			20			20		%
Slew Rate	A_V = –1		450			450			450		V/µs
Settling Time											
10 V Step, A_V = –1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degrees
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	±5		**±18**	**±5**		**±18**	V
Quiescent Current	T_{MIN}–T_{MAX}		5	**6.5**		5	**6.5**		5	7	mA
TRANSISTOR COUNT			72			72			72		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = 15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.5 W
  Cerdip Package . . . . . 1.3 W
Common-Mode Input Voltage, Max Safe . . . . . $|V_S|$ – 3 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±1 V
Continuous Input Current
  Inverting or Noninverting . . . . . 2.0 mA
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Storage Temperature Range (N) . . . . . –65°C to +125°C
Storage Temperature Range (R) . . . . . –65°C to +125°C
Operating Temperature Range
  AD846A/B . . . . . –40°C to +85°C
  AD846S . . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
ESD Rating . . . . . 3500 V

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C, derate cerdip (Q) package at 8.7 mW/°C and plastic (N) package at 10 mW/°C.
Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/W.
Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/W.
SOIC Package: θ_{JA} = 100°C/Watt, θ_{JC} = 33°C/W.

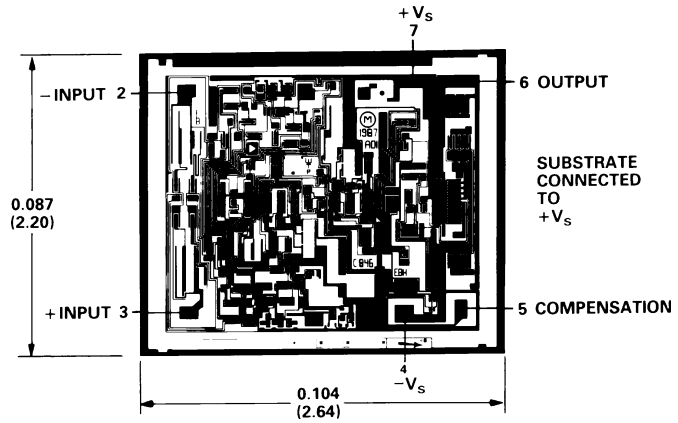
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD846AN	–40°C to +85°C	N-8
AD846BN	–40°C to +85°C	N-8
AD846AQ	–40°C to +85°C	Q-8
AD846BQ	–40°C to +85°C	Q-8
AD846SQ	–55°C to +125°C	Q-8
AD846SQ/883B	–55°C to +125°C	Q-8
5962-8964601PA	–55°C to +125°C	Q-8
AD846AR-16	–40°C to +85°C	R-16
AD846AR-16-REEL	–40°C to +85°C	R-16

NOTES
[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP Package; Q = Cerdip Package, R = SOIC Package

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



AD846 – Typical Characteristics

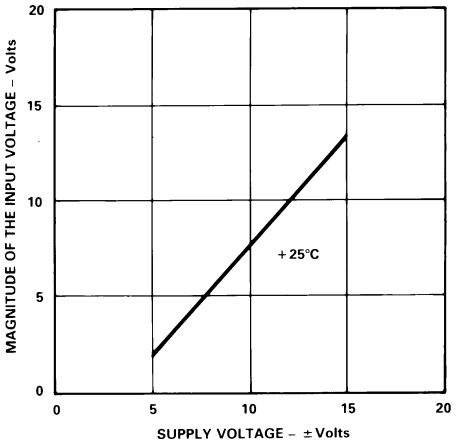


Figure 1. Input Voltage Swing vs. Supply

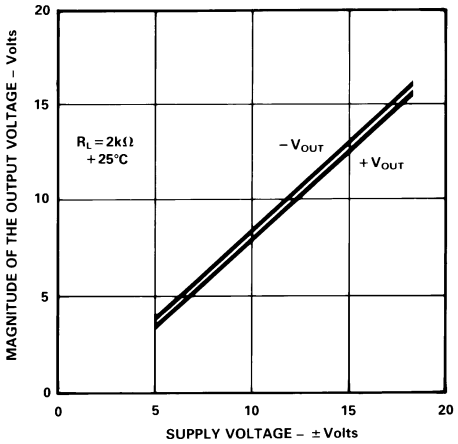


Figure 2. Output Voltage Swing vs. Supply

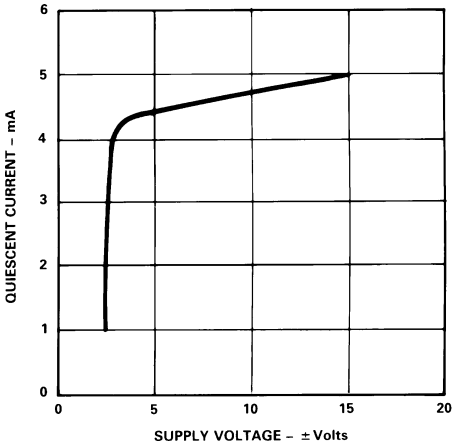


Figure 3. Quiescent Current vs. Supply Voltage

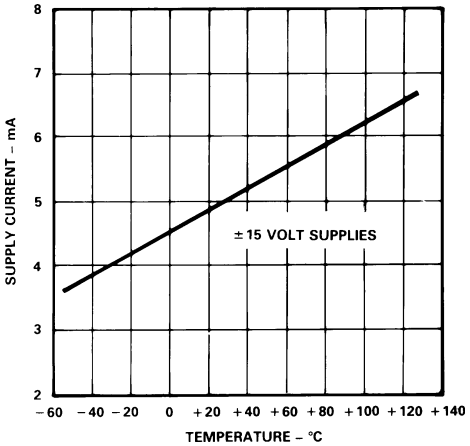


Figure 4. Quiescent Supply Current vs. Temperature

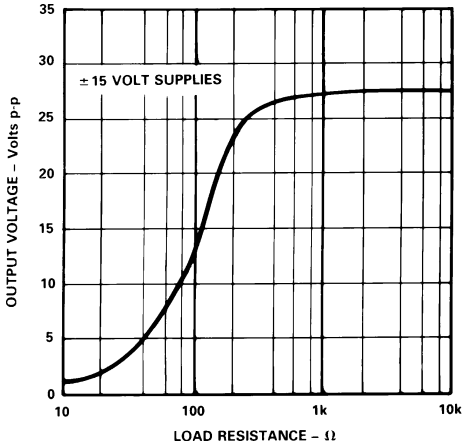


Figure 5. Output Voltage Swing vs. Resistive Load

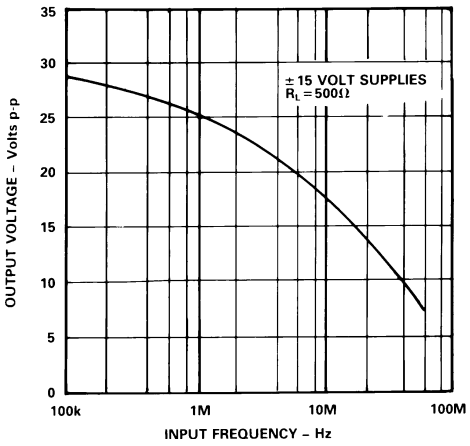


Figure 6. Large Signal Frequency Response

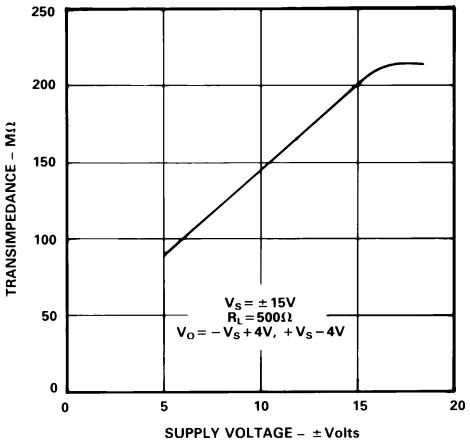


Figure 7. Open-Loop Transimpedance vs. Supply

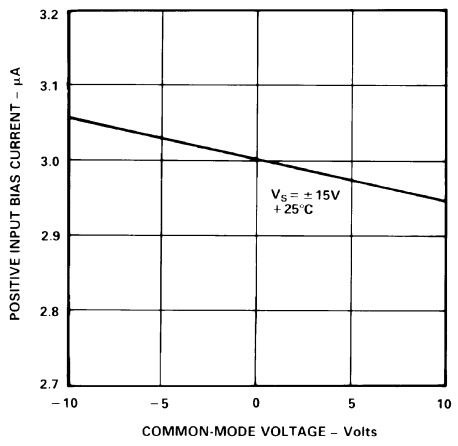


Figure 8. Positive Input Bias Current vs. Common-Mode Voltage

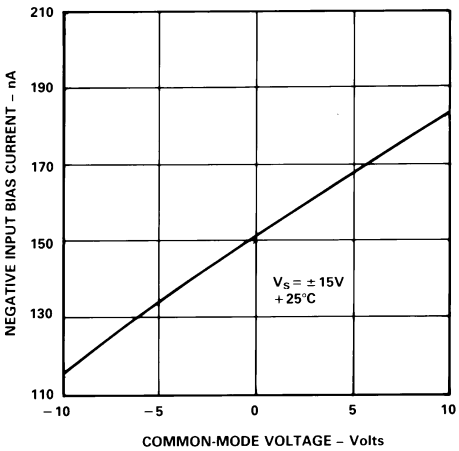


Figure 9. Negative Input Bias Current vs. Common-Mode Voltage

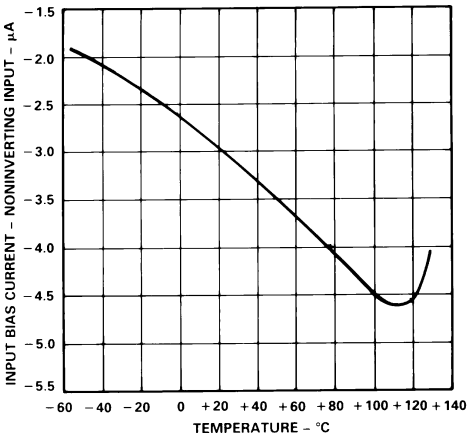


Figure 10. Positive Input Bias Current vs. Temperature

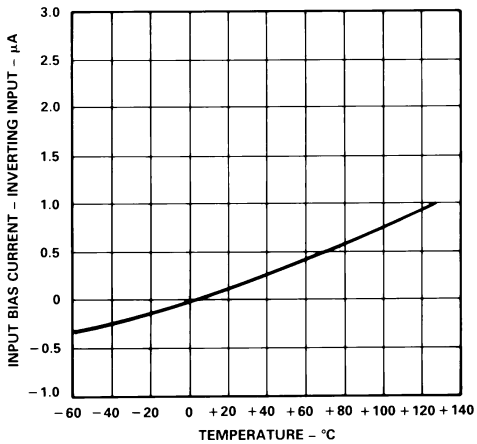


Figure 11. Negative Input Bias Current vs. Temperature

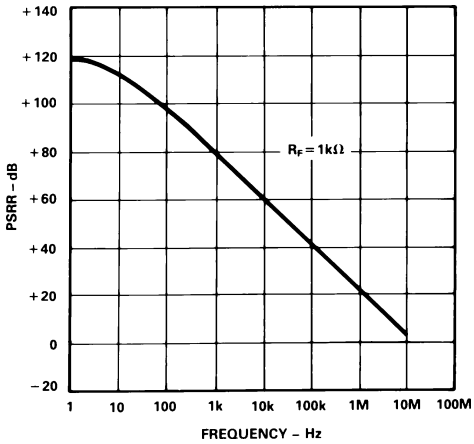


Figure 12. Power Supply Rejection vs. Frequency

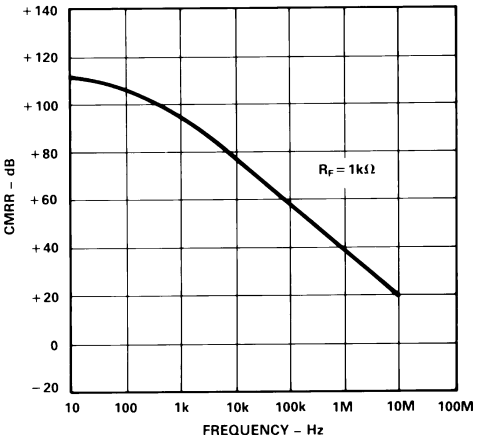


Figure 13. Common-Mode Rejection vs. Frequency

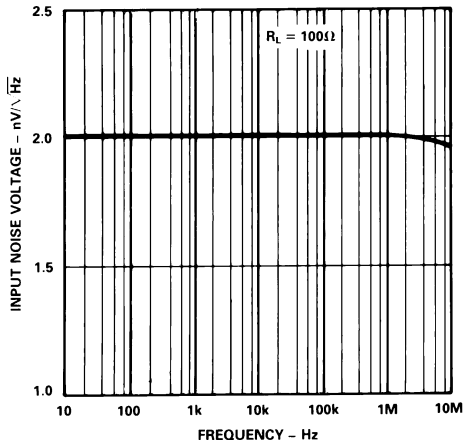


Figure 14. Input Noise Voltage Spectral Density

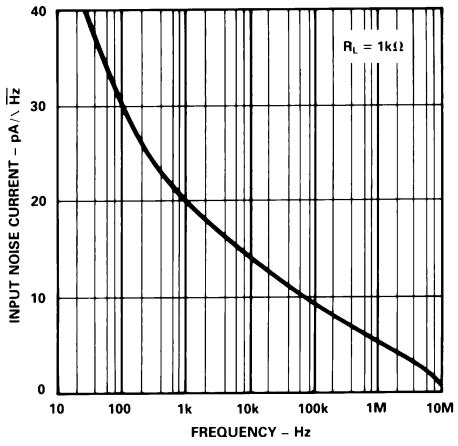


Figure 15. Inverting Input Noise Current Spectral Density

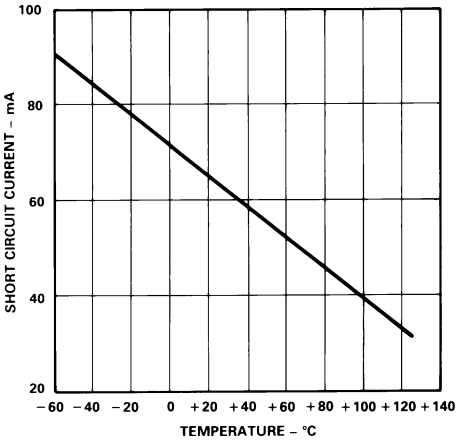


Figure 16. Short Circuit Current Limit vs. Temperature

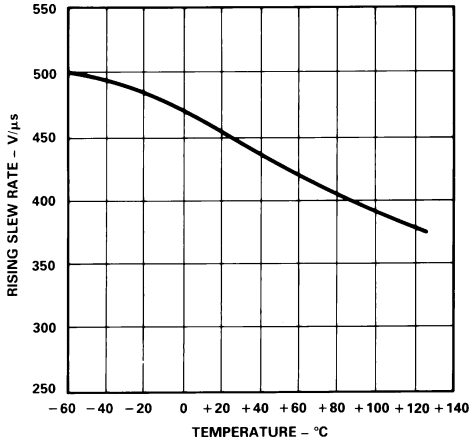


Figure 17. Slew Rate vs. Temperature

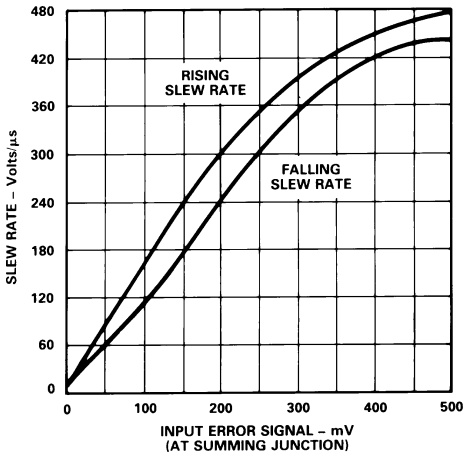


Figure 18. Slew Rate vs. Input Error Signal

AD846 – Typical Characteristics, Inverting Gain of 1

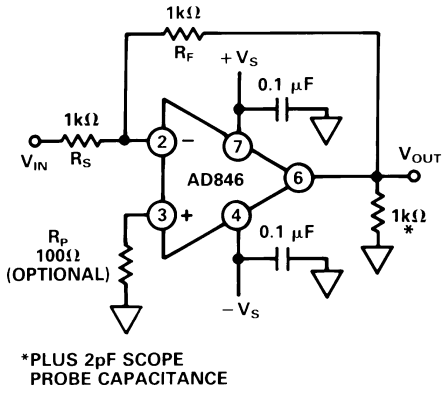


Figure 19a. Inverting Amplifier, Gain of 1

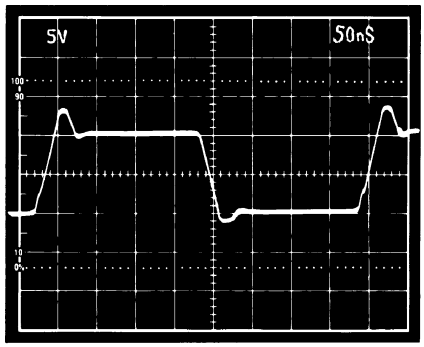


Figure 19b. Large Signal Pulse Response, Gain of –1

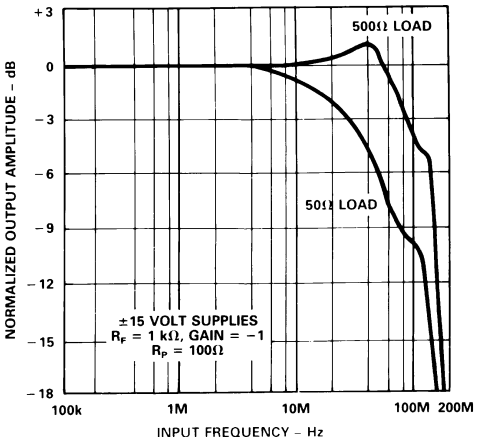


Figure 20. Normalized Output Amplitude vs. Frequency vs. Load

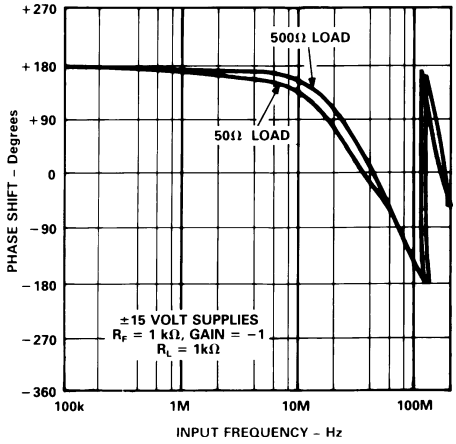


Figure 21. Phase Shift vs. Frequency

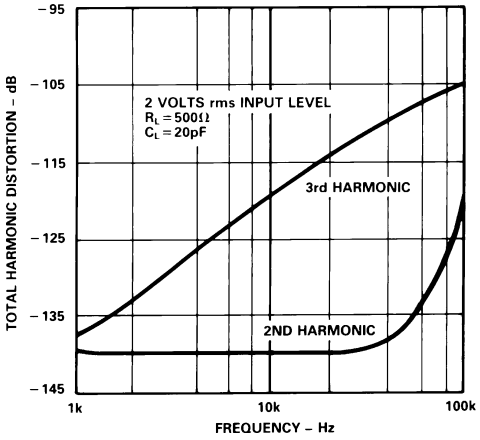


Figure 22. Total Harmonic Distortion vs. Frequency

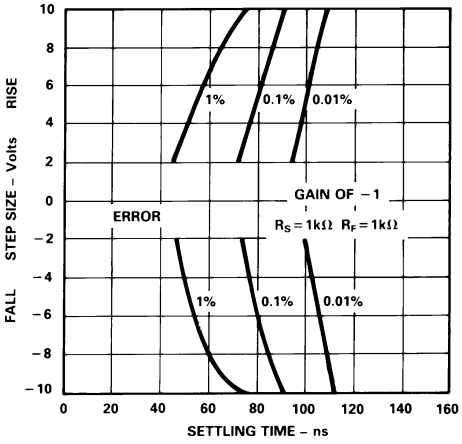


Figure 23. Settling Time vs. Step Size

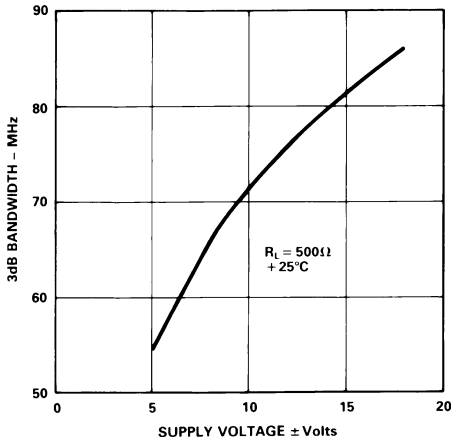


Figure 24. 3 dB Bandwidth vs. Supply Voltage

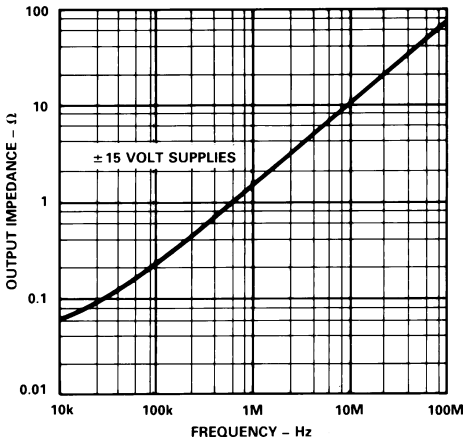


Figure 25. Output Impedance vs. Frequency

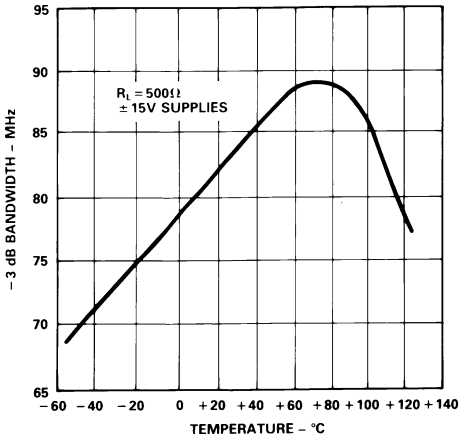


Figure 26. –3 dB Bandwidth vs. Temperature

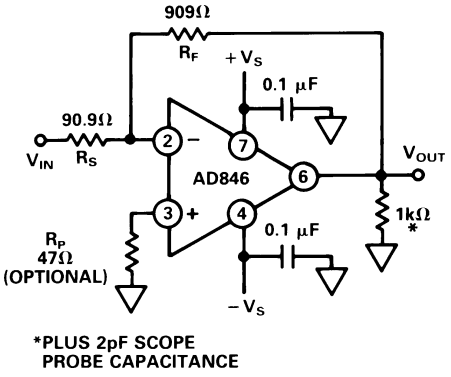


Figure 27a. Inverting Amplifier, Gain of 10

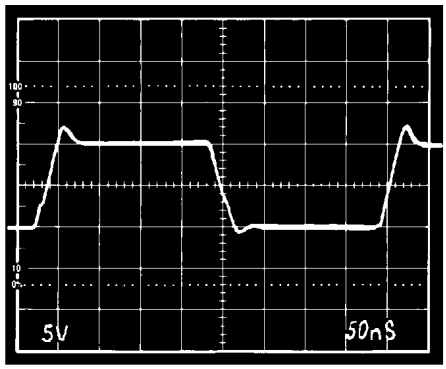


Figure 27b. Large Signal Pulse Response, Gain of 10

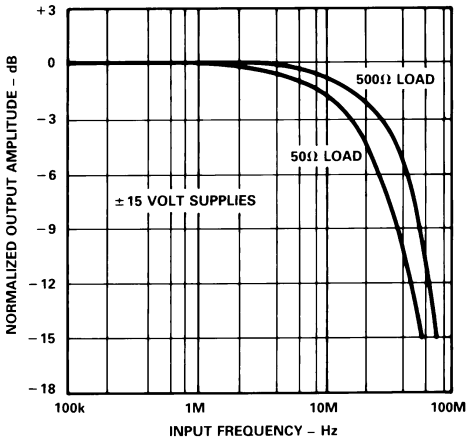


Figure 28. Normalized Output Amplitude vs. Frequency vs. Load

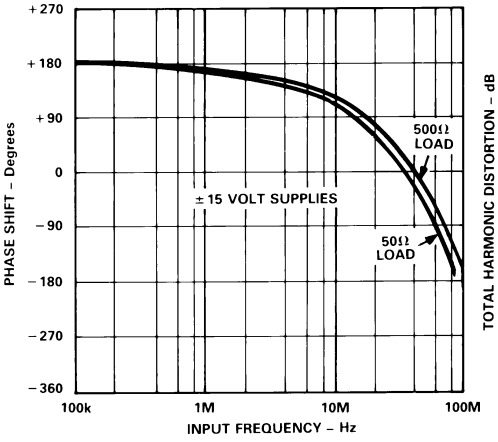


Figure 29. Phase vs. Frequency vs. Load

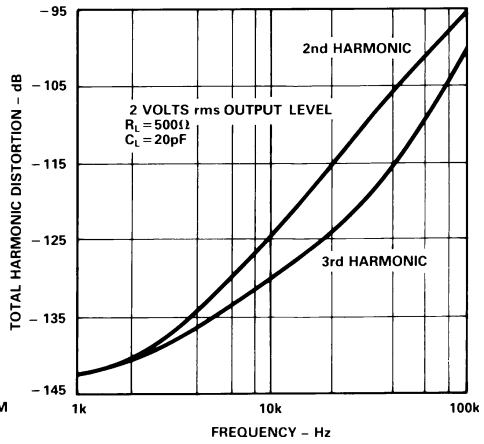


Figure 30. Harmonic Distortion vs. Frequency

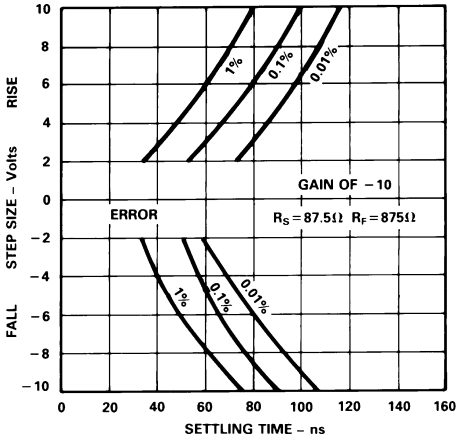


Figure 31. Settling Time vs. Step Size

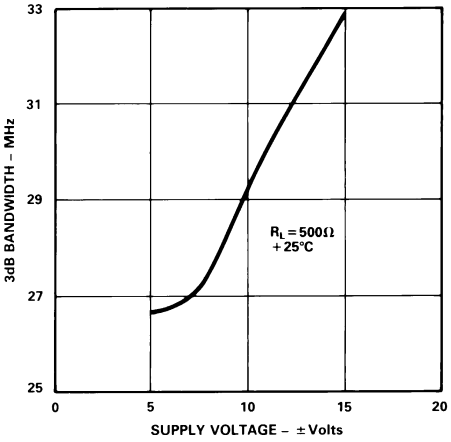


Figure 32. 3 dB Bandwidth vs. Supply Voltage

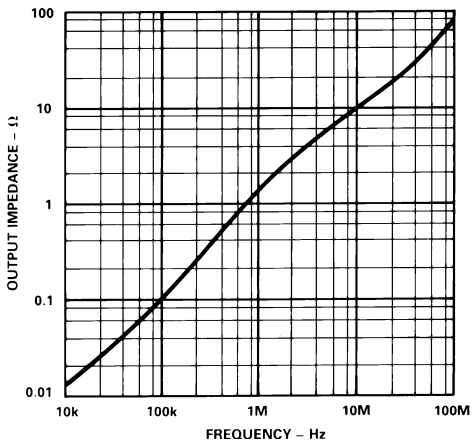


Figure 33. Output Impedance vs. Frequency

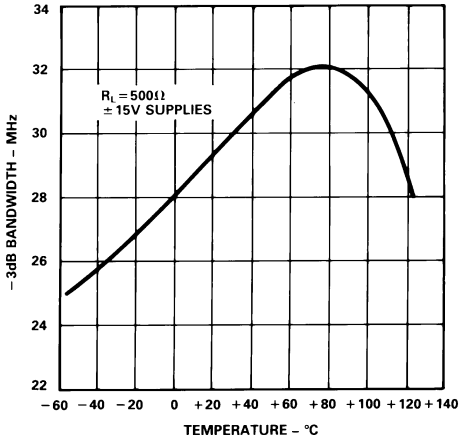


Figure 34. –3 dB Bandwidth vs. Temperature

POWER SUPPLY CONSIDERATIONS

The power supply connections to the AD846 must maintain a low impedance to ground over a bandwidth of 40 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 µF ceramic and a 2.2 µF electrolytic capacitor as shown in Figure 35 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 µF should be used for any application.

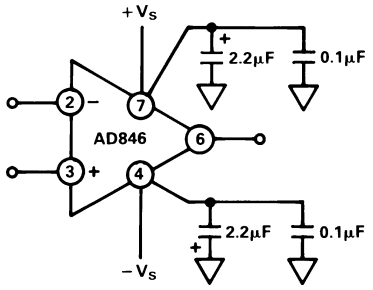


Figure 35. Recommended Power Supply Bypassing

THEORY OF OPERATION

The AD846 differs from conventional operational amplifiers in that it is a transimpedance device rather than a conventional voltage amplifier. Figure 36 is a simplified schematic of the AD846. The input stage consists of a pair of transistors, Q1 and Q2, which are biased by two diode-connected transistors, Q3 and Q4. Transistors Q1 and Q2 have their emitters connected together, and this common point functions as the inverting input of the amplifier. Correspondingly, the common connection of the two biasing diodes acts as the noninverting input.

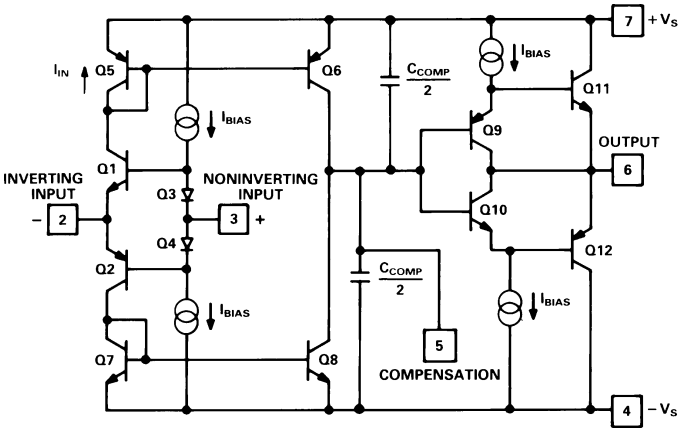


Figure 36. AD846 Simplified Schematic

When operated as a closed-loop amplifier, feedback error current, I_{IN}: flows into the inverting input terminal and is conveyed via current mirrors (transistors Q5, Q6, Q7, and Q8) to the compensation capacitor, C_{COMP}. The voltage developed across C_{COMP} is buffered by the output stage, consisting of transistors Q9–Q12.

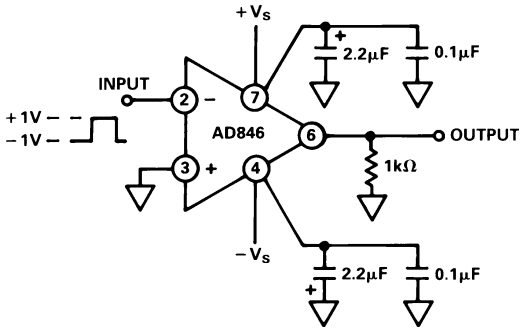


Figure 37. Overload Recovery Test Circuit

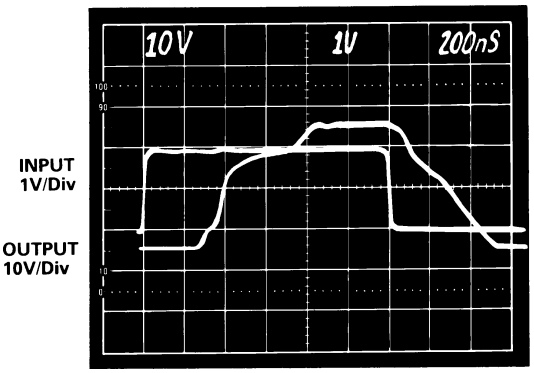


Figure 38. Overload Recovery Time Photo

Because the input error signal developed is in the form of a current, not a voltage, the AD846 differs from conventional operational amplifiers. This also means that, unlike most operational amplifiers which rely on negative feedback to produce a "virtual ground" at the inverting input terminal, this terminal explicitly has a low impedance.

A unique circuit approach allows the AD846 to realize an open-loop transimpedance of close to 200 MΩ. This is nearly three orders of magnitude greater than that of any other operational transimpedance amplifier and results in extremely high levels of dc precision.

As an example, the output voltage gain error is approximately equal to the value of the feedback resistor divided by the value of the open-loop transimpedance of the amplifier. That is, when using a 1 kΩ feedback resistor, this error is one part in 200,000. For a transimpedance amplifier with 1 MΩ transimpedance, this error is only one part in 1000; such an amplifier would barely be able to achieve 10-bit precision.

Figure 39 is a simplified three-terminal model for the AD846. Figure 40 is a simplified three-terminal model for a conventional voltage op amp. The action of current feedback serves to modify the behavior of the amplifier under closed-loop conditions. The feedback resistor, R_F, is somewhat analogous to the input stage transconductance of a conventional voltage amplifier; and therefore, if the value of R_F is held constant, the closed-loop bandwidth also remains virtually constant, independent of closed-loop voltage gain.

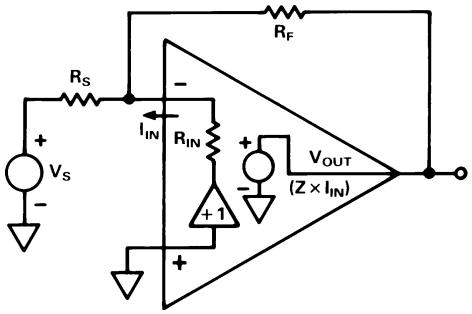


Figure 39. AD846 Three-Terminal Model

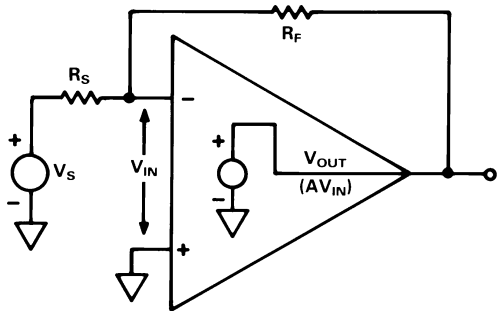


Figure 40. Op Amp Three-Terminal Model

A more detailed examination of the closed-loop transfer function of the AD846 results in the following equation:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + C_{COMP}\left[R_F + \left(1 + \frac{R_F}{R_S}\right)R_{IN}\right]s\right)}$$

Compare this to the equation for a conventional op amp:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + \frac{C_{COMP}}{g_M}\left(1 + \frac{R_F}{R_S}\right)s\right)}$$

where: C_{COMP} is the internal compensation capacitor of the amplifier; g_M is the input stage transconductance of the amplifier.

In the case of the voltage amplifier, the closed-loop bandwidth decreases directly with increasing values of $(1 + R_F/R_S)$, the closed-loop gain. However, for the transimpedance amplifier, the situation is different. At low gains, where $(1 + R_F/R_S)\ R_{IN}$ is small compared to R_F, the closed-loop bandwidth is controlled by the internal compensation capacitance of 7 pF and the value of R_F, and not by the closed-loop gain. At higher gains, where $(1 + R_F/R_S)\ R_{IN}$ is much larger than R_F, the behavior is that of a conventional operational amplifier in which the input stage transconductance is equal to the inverting terminal input impedance of the transimpedance amplifier (R_{IN} = 50 Ω).

A simple equation can, therefore, be used to determine the bandwidth of an amplifier employing the AD846 in the inverting configuration.

$$3\ dB\ Bandwidth = \frac{23}{R_F + 0.05\left(1 + G\right)}$$

where: The *3 dB bandwidth* is in MHz

G is the closed-loop inverting gain of the AD846

R_F is the feedback resistance in kΩ.

NOTE: This equation applies only for values of R_F between 10 kΩ and 100 kΩ, and for R_{LOAD} greater than 500 Ω. For R_F = 1 kΩ the bandwidth should be estimated from Figure 41.

Figure 41 illustrates the closed-loop voltage gain vs. frequency of the AD846 for various values of feedback resistor. For comparison purposes, the characteristic of a conventional amplifier having an 80 MHz unity gain bandwidth is also shown.

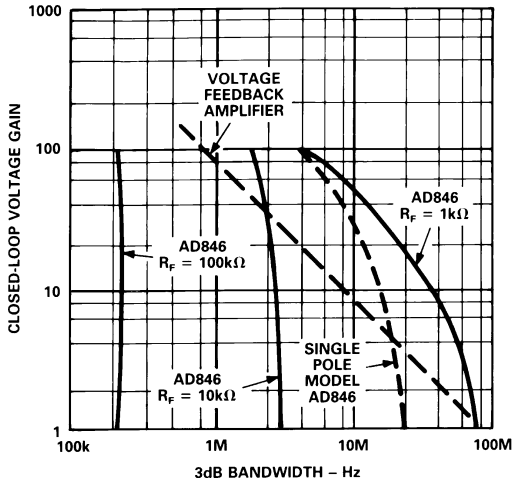


Figure 41. Closed-Loop Voltage Gain vs. Bandwidth for Various Values of R_F

For the case where R_F = 1 kΩ and R_S = 100 Ω (closed-loop gain of –10), the closed-loop bandwidth is approximately 28 MHz. It should also be noted that the use of a capacitor to shunt R_F, a normal practice for stabilizing conventional op amps, will cause this amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

A similar approach can be taken to calculate the noise performance of the amplifier. A simplified noise model is shown in Figure 42.

The equivalent mean-square output noise voltage spectral density will equal:

$$V_{ON}^{\ 2} = \left(R_F\ I_{NN}\right)^2 + \left(1 + \frac{R_F}{R_S}\right)^2 \left[V_N^{\ 2} + \left(R_P\ I_{NP}\right)^2 + 4\ kT\ R_P\right]$$

$$+ 4\ kT\ R_F\left(\frac{R_F}{R_S} + 1\right)$$

Where:

R_P is the external resistance placed in series with the noninverting input
R_F is the feedback resistor
R_S is the source resistor
I_{NN} is the noise current in the inverting input
I_{NP} is the noise current in the noninverting input
V_N is the input noise voltage.

Typical values for these parameters (@ 1 kHz) in pA/$\sqrt{\text{Hz}}$ are: I_{NN} = 20, I_{PN} = 6, V_N = 2.

Or, referring to the signal input, the equivalent mean-square input voltage noise is:

$$V_{IN}{}^2 = \left(R_F\, I_{NN}\right)^2 + \left(1+\frac{R_S}{R_F}\right)^2\left[V_N{}^2 + \left(R_P\, I_{NP}\right)^2 + 4\,kT\,R_P\right]$$

$$+ 4\,kT\,R_S\left(1+\frac{R_S}{R_F}\right)$$

Resistor R_P is required for both inverting and noninverting (follower) operation, to insure stable operation. The amplifier's noninverting input current (flowing through R_P of 100 Ω) will typically add less than 300 µV to the AD846's input offset voltage. This can be trimmed-out using the optional network shown in Figure 44. The following table gives recommended values for R_P.

Supply Voltage	Gain (R_F/R_S)	Recommended Value for R_F
6 V to 15 V	1–10	100 Ω
6 V to 15 V	10–20	47 Ω
6 V to 15 V	20–200	0 Ω
5 V	1–10	47 Ω
5 V	10–200	0 Ω

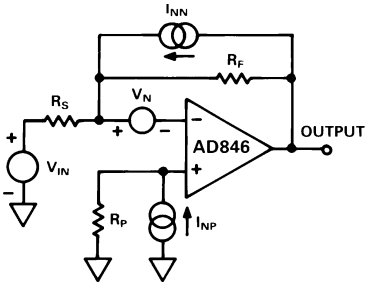


Figure 42. Op Amp Simplified Noise Model

NONINVERTING GAIN OPERATION

The AD846 can be used as a noninverting amplifier or voltage follower, operating at gains between 1 and 200. A minimum value of R_F equal to 1 kΩ should be employed. For low gains (1 to 2), the input signal should be applied to the AD846's noninverting input through a 100 Ω series resistor; this will help reduce peaking. The best transient response will occur when the amplifier's output level is below 5 V peak to peak.

At closed-loop gains of 3 or more, the input resistor is not required unless peak signals greater than 3 V will be applied. The amplifier's bandwidth can be determined by using the inverting amplifier's bandwidth equation or from Figure 41. For example, at a gain of + 10 (R_F = 1 kΩ, R_S = 100 Ω) the bandwidth of the AD846 will be approximately 33 MHz; at a gain of +100, (R_F = 1 kΩ, R_S = 10 Ω) it will be 4 MHz. At gains of 3 or greater, a small capacitor (2 pF–5 pF) connected across the feedback resistor will help reduce overshoot; but when operating at noninverting gains below 3, this same capacitance will cause instability.

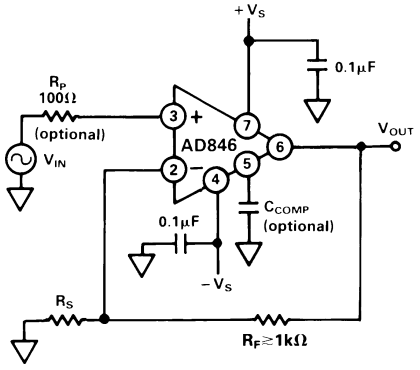


Figure 43. AD846 Noninverting Amplifier Configuration

USING THE COMPENSATION PIN OF THE AD846

Additional compensation may be provided for the AD846 by applying an external capacitance between Pin 5 and analog ground (Figure 44). The nominal value of the AD846's internal compensation capacitor is 7 pF. For a given value of feedback resistance (R_F), any added external capacitance reduces the amplifier's slew rate and bandwidth proportionally.

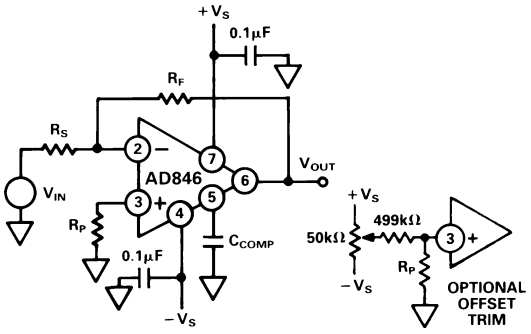


Figure 44. AD846 Inverting Amplifier Showing External Compensation Connection, R_P and Optional V_{OS} Trim

In addition to providing for external compensation, Pin 5 may be used to clamp the output of the amplifier, as shown in Figure 45. The output can be clamped anywhere within the output range (approximately ±10 V) of the amplifier. The input should also be clamped as a precaution against damaging the amplifier's input transistors.

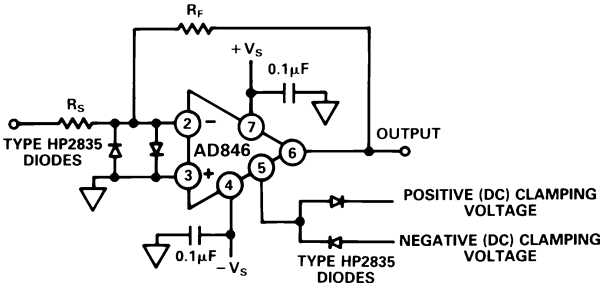


Figure 45. AD846 Used as a Clamped Amplifier

This compensation node may also be used as an additional output terminal as in the precision transconductance amplifier application of Figure 46.

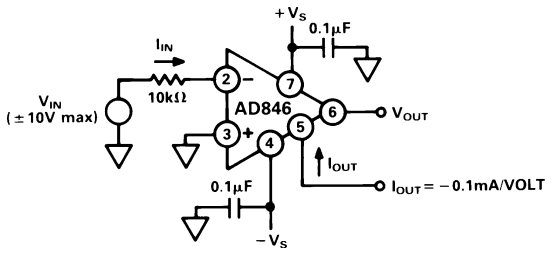


Figure 46. A Precision Transconductance Amplifier

The AD846 can be used in either the inverting transconductance mode as shown in Figure 46, or in a noninverting mode with R_S grounded and V_{IN} applied to the noninverting terminal. The current output is essentially constant over a compliance range of ±10 V at the compensation node. The output current (from Pin 5) is limited to about ±1 mA due to internal saturation. Under these circumstances the normal output pin provides a buffered version of the compensation node output voltage. Output load impedance of 500 Ω or greater will not affect the accuracy of the transconductance conversion.

THE AD846 IN A 2 MHz, 12-BIT SUBRANGING A/D CONVERTER CIRCUIT

The combination of fast settling times at high gains and low dc errors make the AD846 ideal for use as an error amplifier in high speed, 12-bit subranging A-D applications. In the circuit of Figure 47, an AD842 serves as an input amplifier. First pass conversion is accomplished, in a straightforward manner, determining the top 7 bits. The latch then holds these top 7 bits which are applied to a 7 bit, 12-bit accurate DAC and also to the highest 7 bits of the adder (note that a sample-and-hold should be used ahead of this converter to minimize errors due to its 500 ns acquisition time). In the second pass, the input switches S1 and S2 and S3 are set to state 2. The DAC output is then subtracted from the input signal and the resulting difference is then amplified by an AD846 gain of 32 follower. This gain, together with a 1/64th scale offset, insures a unipolar residue which can be converted by the flash A-D. Conversion is accomplished via switches S1, S2 and S3 in state 1. Switch S1 connects the input signal of the AD846 residue amplifier to ground which minimized overload recovery time.

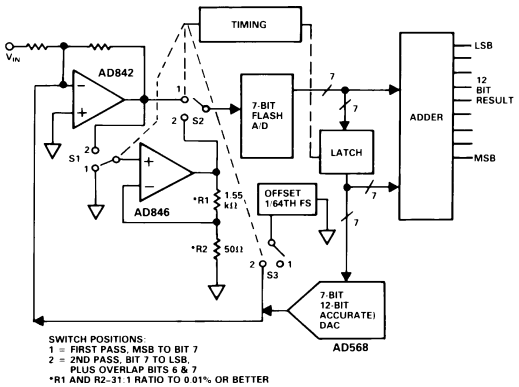


Figure 47. Block Diagram of a 2 MHz, 12-Bit Subranging A/D Converter

THE AD846 AS AN OPEN-LOOP LEVEL SHIFTER

The AD846 can also be used for open-loop level shifting. As shown in Figure 48, resistor R_S is used to develop an input current which is proportional to the input voltage, V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (R_C is equal in value to resistor R_S) which, rather than being grounded, has one end tied to reference voltage V2. The voltage appearing at Pin 5 is, therefore, voltage V_{IN} plus voltage V2 and will directly follow changes in V_{IN}. By scaling resistor R_C, a level shift with voltage gain can be produced.

In addition, the normal voltage output at Pin 6 is approximately equal to the voltage at Pin 5 thus providing a low impedance, buffered output for the level shifter.

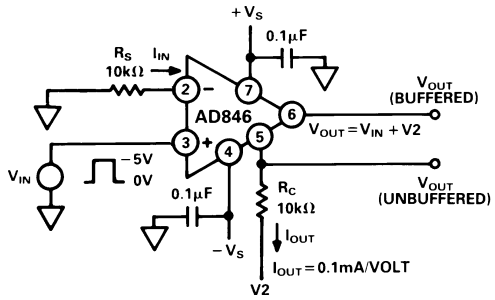


Figure 48. AD846 Connected as a Level Shift Amplifier

THE AD846 AS A HIGH SPEED DAC BUFFER

The AD846 will enable the AD568 12-bit DAC to develop a 10 V output step which settles to within 0.025 percent of itsfinal value in about 100 ns. This AD846/AD568 combination is shown in the circuit of Figure 49. Correct power supply decoupling is essential: a 2.2 μF tantalum capacitor connected in parallel with a 0.1 μF to 0.01 μF ceramic disc capacitor is usually sufficient. These should be placed as close to the power supply pins as possible. Also, a ground plane should be employed; this ensure that there is a low impedance signal path to ground which allows the fastest possible output settling. In 12-bit systems with the AD846 operating at gains of 10 or less, inadequate supply decoupling can cause the output settling to degrade from 100 ns to as much as 300 ns, with a 10 V output step applied.

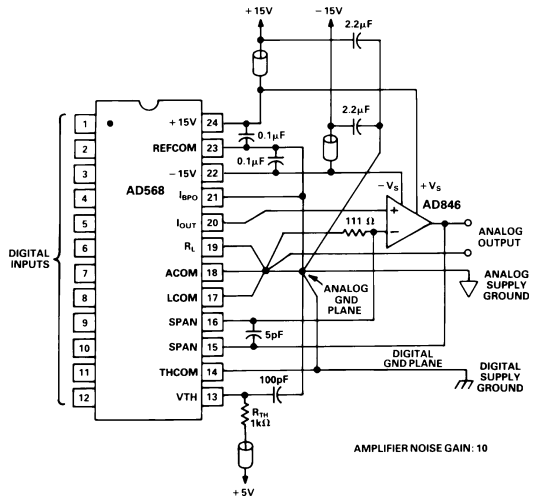
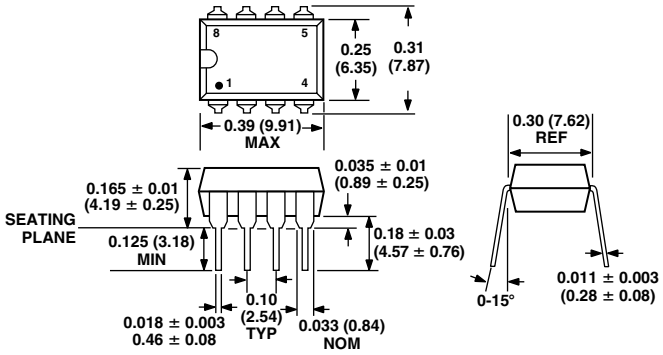


Figure 49. The AD846 Serving as a DAC Buffer

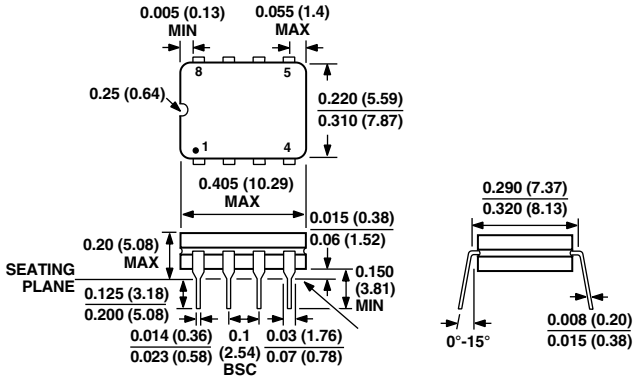
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

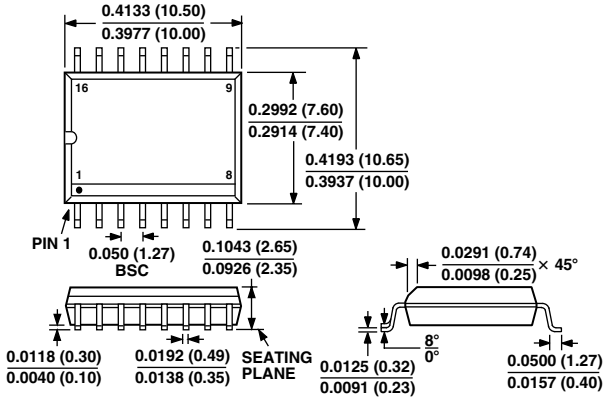
Plastic Mini-DIP (N) Package



Cerdip (Q) Package



R-16 Package



C1155–0–5/00 (rev. C) 00898

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AD846　高速, 高精度, 電流帰還型

ANALOG DEVICES

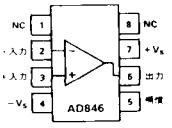
●スルーレート:450V/μs
●優れたDC特性
●DG:0.01%, DP:0.028°
●消費電流:5mA
●Av=-1～-100で真の12ビット精度を確保

セカンド・ソース			類似品
/			/

■ピン接続図

プラスチック・ミニDIP(N)パッケージ
および
サーディップ(Q)パッケージ

上面図



NC=接続なし

●電気的特性	●最大定格	AD846A		AD846B		単位
Vs=±15V	電源電圧	±18		±18		V
RL=150	入力電圧	|Vs|-3		|Vs|-3		V
Ta=25℃	差動入力電圧	±1		±1		V
	動作温度	-40～+85		-40～+85		℃
	許容損失	/		/		mW

規格	記号	条件	標準値	最悪値	標準値	最悪値	単位
入力オフセット電圧	Vos		0.025	0.2	0.025	0.075	mV
Voの温度ドリフト	TC/Vos		0.8	5	0.8	3.5	μV/℃
Voの長期安定性	Vos/time		/	/	/	/	μV/月
入力バイアス電流	Ib	①	3000	15000	3000	5000	nA
入力オフセット電流	Ios		/	/	/	/	nA
入力雑音電圧	Vn		/	/	/	/	μVp-p
入力雑音電圧密度	en	②	2	/	2	/	nV/√Hz
入力雑音電流密度	in	③	20	/	20	/	pA/√Hz
差動入力抵抗	Rin		0.01	/	0.01	/	MΩ
同相入力抵抗	RinCM		/	/	/	/	GΩ
同相入力電圧範囲	VCM		±10	/	±10	/	V
同相信号除去比	CMRR	④	125	110	125	120	dB
電源変動除去比	PSRR	⑤	125	110	125	120	dB
大信号電圧利得	Avo		/	/	/	/	V/mV
出力電圧振幅	Vo	⑥	±10	/	±10	/	V
出力インピーダンス	Zo	⑦	16	/	16	/	Ω
出力電流	Io	⑧	65	/	65	/	mA
電源電流	Is	⑨	5	6.5	5	6.5	mA
スルーレート	SR	⑩	450	/	450	/	V/μs
利得帯域幅積	GBW		/	/	/	/	MHz
帯域幅	fT	⑪	80	/	80	/	MHz
ライズ・タイム	tr	⑫	10	/	10	/	ns
セトリング・タイム	ts	⑬	110	/	110	/	ns
オーバシュート	OS	⑭	20	/	20	/	%
微分利得	DG	⑮	0.01	/	0.01	/	%
群遅延特性	GD		0.028	/	0.028	/	degree
高調波ひずみ率	THD		/	/	/	/	%
チャネル・セパレーション	CS		/	/	/	/	dB

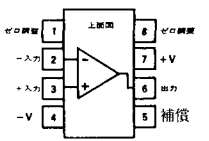
条件
① 非反転入力
② f0=1kHz
③ f0=1kHz
④ VCM=±10V
⑤ Vs=±5～±18V
⑥ RL=500
⑦ 開ループ
⑧ 出力短絡時
⑨ 全温度範囲
⑩ Av=-1
⑪ Av=-1, RF=1k
⑫ Av=-1
⑬ 10V±0.01%, Av=-1
⑭ Av=-1
⑮ f=4.4MHz, RL=100

AD844A/B/S, AD846A/B/S, AD9617JN/JR, AD9618JN/JR, AD810 電流帰還型OPアンプ

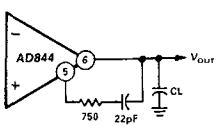
型　　名	AD844A/B/S	AD846A/B/S	AD9617JN/JR	AD9618JN/JR	AD810
動作電源電圧	±4.5～±18V（±18$V_{(max)}$）	←	±5V（±7$V_{(max)}$）	←	±5～±15V（±18$V_{(max)}$）
消費電流$_{(typ)}$	6.5mA（無負荷）	5mA（無負荷）	±34mA（無負荷）	±34mA（無負荷）	8m$A_{(max)}$
消費電力$_{(typ)}$	×	×	×	×	×
帯域幅$_{(typ)}$	60MHz（A_v=−1） 33MHz（A_v=−10） （V_S=±15V, −3dB, R_f=R_2=1kΩ）	46MHz（A_v=−1, R_F=1k） 31MHz（A_v=−10, R_F=875Ω） 〔V_S=±15V, −3dB〕	190MHz（V_S≦2V_{PP}） 150MHz（V_O=4V_{PP}） （V_S=±5V, −3dB, A_v=3, R_F=400Ω, R_L=100Ω）	160MHz（V_O≦2V_{PP}） 150MHz（V_O≦5V_{PP}） （V_S=±5V, −3dB, A_v=10, R_F=1kΩ, R_L=100Ω）	−3 dB：80MHz（A_v=+1） ：75MHz（A_v=+2） −0.1dB：30MHz（A_v=+2） 〔V_S=±15V, R_L=150Ω〕
スルーレート$_{(typ)}$	2000V/μs（V_S=±15V, オーバドライブ入力）	450V/μs（V_S=±15V, A_v=−1）	1400V/μs（V_S=±5V, A_v=3, R_L=100Ω, V_O=4V）	1800V/μs（V_S=±5V, A_v=10, R_L=100Ω, V_O=4V）	350V/μs〔A_v=−10, V_S=−5 V, R_L=150Ω〕 1000V/μs〔A_v=−10, V_S=±15V, R_L=400Ω〕
$CMRR_{(typ)}$	×	×	60dB	60dB	64dB（V_S=±15V）
$PSRR_{(typ)}$	×	×	60dB（⊿V_S=±5%）	60dB（←）	72dB（V_S=±4.5～±18V）
セトリング時間$_{(typ)}$	100ns（A_v=−1, −10, 0.1%, R_L=500Ω, 10Vステップ）	80ns（A_v=−1, 0.1%, 10Vステップ）	10ns（A_v=3, R_L=100Ω, 0.1%, 2Vステップ）	9ns（A_v=10, R_L=100Ω, 0.1%, 2Vステップ）	×
出力電流$_{(typ)}$	±50mA（R_L=50Ω）	出力電圧±10$V_{(min)}$（R_L=500Ω）	60m$A_{(min)}$（R_L=50Ω, A_v=3, V_S=±5V）	60m$A_{(min)}$（R_L=50Ω, A_v=10, V_S=±5V）	60m$A_{(min)}$（V_S=±15V, R_L=150Ω）
微分位相$_{(typ)}$	±0.1°（3.58MHz）	0.1°（F=3.58MHz）	0.02°	0.02°	0.04°（F=3.58MHz, V_S=±15V, R_L=150Ω）
微分利得$_{(typ)}$	±0.1%	0.1%（F=3.58MHz）	0.01%	0.01%	0.02%（F=3.58MHz, V_S=±15V, R_L=150Ω）
帰還抵抗$_{(typ)}$	R_1=R_2=500Ω（A_v=−1）	1kΩ	400Ω	1kΩ	×
動作利得範囲$_{(typ)}$	±1～	±1～	±1～±40	+5/−1～±100	×
歪率$_{(typ)}$	0.005%（F=100kHz, 2V_{rms}, R_L=500Ω）	0.0005%（F=100kHz, V_S=±15V）	HD_2:−86dBc（2V_{PP}, 4.3MHz, A_v=3, R_L=100Ω） HD_3:−83dBc	HD_2:−83dBc（2V_{PP}, 4.3MHz, A_v=10, R_L=100Ω） HD_3:−85dBc	−61dBc〔F=10MHz, V_S=±15V, R_L=400Ω, V_O=2 V_{p-p}, A_v=+2〕
入力インピーダンス$_{(typ)}$	10MΩ（+R_{IN}, 50Ω（−R_{IN}）	10kΩ（+R_{IN}）, 67Ω（−R_{IN}）	60kΩ	75kΩ	−R_{IN}=10MΩ/2 pF（V_S=±15V）
出力インピーダンス$_{(typ)}$	15Ω（オープン・ループ）	16Ω（オープン・ループ）	0.07Ω（at DC）	0.08Ω（at DC）	15Ω（オープン・ループ, 5 MHz, V_S=±15V）
温度範囲（℃）	A, B：−40～+85 S　：−55～+125	←	JN, JR：0～+70	←	A：−40℃～+85℃ S：−55℃～+125℃
パッケージ	N：8P-DIP Ⓐ Q：8P-サーディップ	H：TO-99 Ⓑ N：8P-DIP Q：8P-サーディップ	JN：8P-DIP Ⓒ JR：8P-SOP	← Ⓒ	N：8P-DIP Ⓓ R：8P-SOIC Q：8P-サーディップ
機能	●20MHzフルパワー帯域 ：20V_{PP}, R_L=500Ω ●低オフセット電圧 150μ$V_{(max)}$（Bグレード）	●DC性能良好 ●入力オフセット電圧 ：75μ$V_{(max)}$（Bグレード） ●入力オフセット・ドリフト ：3.5μV/℃$_{(max)}$（Bグレード） ●入力電圧ノイズ ：2nV/$\sqrt{\text{Hz}}$	●低歪，高精度 ●入力オフセット電圧 ：±0.5mV ●入力オフセット電圧T_C ：+3μV/℃ （A_v=3, V_S=±5V, R_L=100Ω）	●低歪，高精度 ●←：+0.5mV ●←：+3μV/℃ （A_v=10, V_S=±5V, R_L=100Ω）	●出力ディセーブル機能 ●低消費電力

AD844A/B/S, AD846A/B/S, AD9617JN/JR, AD9618JN/JR, AD810 電流帰還型OPアンプ(つづき)

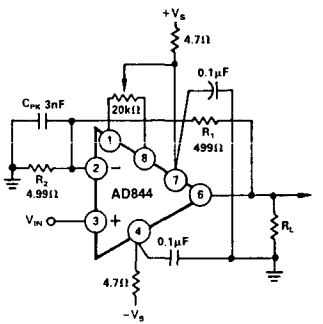
Ⓐ ■端子接続図



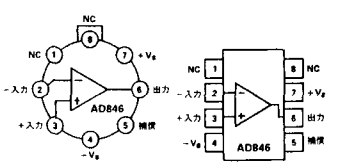
●大容量性負荷のための位相補償回路例



●オフセット付き ×100 非反転アンプ回路例



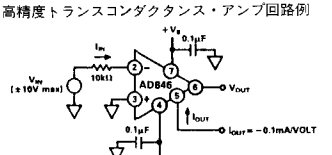
Ⓑ ■端子接続図



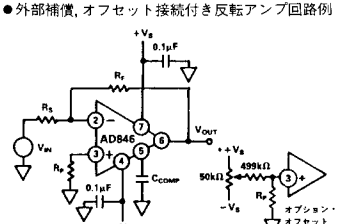
注意：キャンはV+に接続
NC＝接続なし
NC＝接続なし

電源電圧	ゲイン（R_F/R_S）	R_Fの推奨値
6～15V	1～10	100Ω
6～15V	10～20	47Ω
6～15V	20～200	0Ω
5V	1～10	47Ω
5V	10～200	0Ω

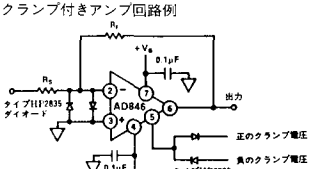
●高精度トランスコンダクタンス・アンプ回路例



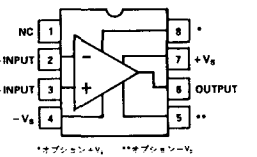
●外部補償，オフセット接続付き反転アンプ回路例



●クランプ付きアンプ回路例

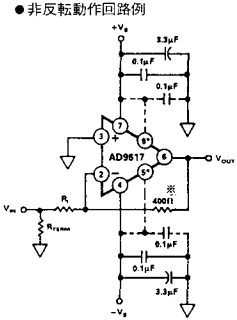


Ⓒ ■端子接続図

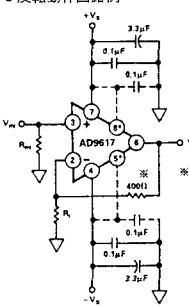


注：最良のセトリング時間と歪み特性を得るために、オプションの電源端子をご使用ください。仕様に示す特性はこの端子を使用することを前提にしています。

●非反転動作回路例

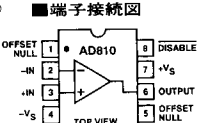


●反転動作回路例

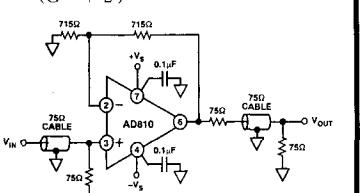


※ AD9618では1000Ω

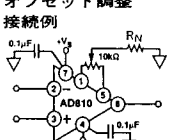
Ⓓ ■端子接続図



●ビデオ・ライン・ドライバ回路図
（G＝＋2）



●オフセット調整接続例



	V_S＝＋5 V	V_S＝±15V
R_S	50kΩ	150kΩ