●新特器件应用

单电源低功耗运算放大器 AD820/AD822/AD824的特点与应用

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摘要：文章介绍了AD820、AD822和AD824运算放大器的主要性能指标及其特点，列举了几个应用例子，并且讨论了应用中几个有关问题。

关键词：单电源供电　场效应晶体管输入级　差积分器

AD820/AD822/AD824三种运算放大器都是美国模拟器件公司生产的单电源、低功耗、精密场效应输入的运算放大器。采用双电源工作时，它的输出电压能够达到电源的正负电源电压。这三种运算放大器是属于同一个系列产品，它们的电气性能指标基本相同，所不同的是AD820的芯片内只有一个运算放大器，AD822的芯片内含有二个性能匹配的运算放大器，AD824的芯片内含有四个性能匹配的运算放大器。本文对AD820、AD822、AD824三种运算放大器的主要性能指标及其应用中的一些问题进行讨论，供广大读者参考。

1、AD820/AD822/AD824运算放大器主要特点及主要性能指标

AD820/AD822/AD824三种运算放大器主要特点如下：

它们都是同种类型的运算放大器。运算放大器有二种工作电压模式：单电源工作和双电源工作。单电源工作时，额定工作电压由+3V到+36V，双电源工作时，额定工作电压由±1.5V到±18V。它们的输出电压摆幅仅比电源电压小10mV。当采用正负电源电压供电时，输出电压即达到电源电压的正负限((Rail-to-Rail)。当采用单电源供电时，输入信号允许负电压，这样能够获得最大的动态范围。

这些运算放大器都是低失调电压、低失调电压漂移、低噪声的N沟通结型场效应晶体管输入的运算放大器，因此运算放大器都具有很高的输入阻抗，无论是共模状态还是差动状态，典型值都在$10^{13}\Omega$以上，输入电容很小，共模状态典型值只0.5pf，差动状态的输入电容是2.8pF。

AD820、AD822和AD824三种运算放大器都有短路保护功能。当输出错误地与地或者电源输入端短接时，保护器件不受损坏。但是，运算放大器没有过热保护，当器件结温短时间超过最大值时，只要结温下降，仍能恢复正常工作。如果结温长时间超过最大值时，就要永久损坏器件。

正常工作时，输入电流极小，均在皮安级。

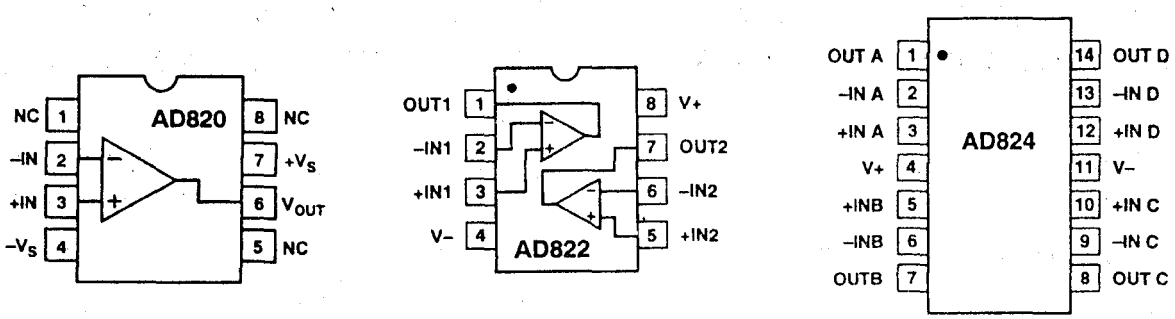
三种运算放大器不仅都是真正的单电源工作，而且在+3V低电压条件时能保持电气性能，因此它们都是电池供电路的首选器件。

三种运算放大器都有三种封装形式，分别为塑料双列直插封装、密封陶瓷双列直插封装和表面安装封装。

AD820、AD822、AD824三种运算放大器的管脚排列不同，各运算放大器的管脚排列如图(1)所示。

2、AD820、AD822和AD824运算放大器的应用

由于AD820、AD822和AD824三种运



a. AD820 管脚排列　　b. AD820 管脚排列　　c. AD824 管脚排列

图 1　AD820、AD822 和 AD824 三运算放大器的管脚排列图

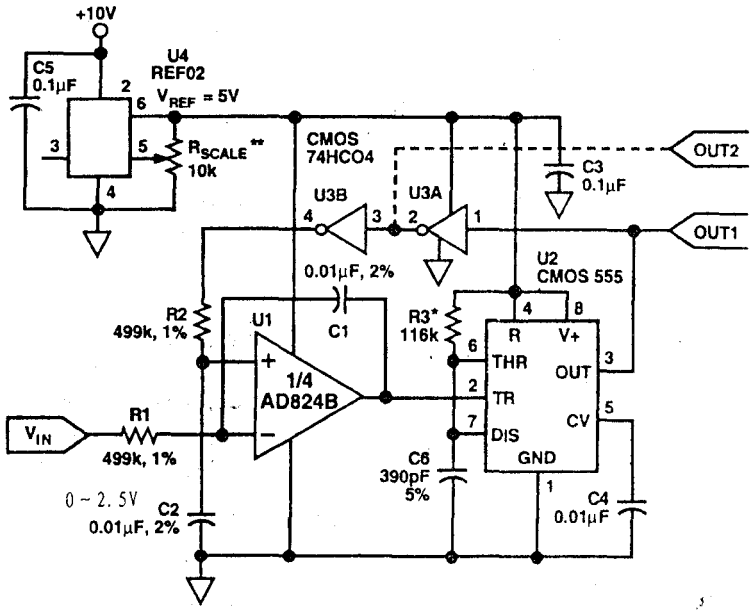


图 2　单电源电压—频率转换器原理图

算放大器的电器性能及电路结构形式相同，因此它们的应用领域是完全相同的。在电池供电的精密仪器、医疗仪器、低功耗参考源和稳压器、有源滤波器、12 位到 14 位的数据采集系统以及光敏二极管的前置放大器等各个方面都得到广泛的应用。

为了能更好地发挥 AD820、AD822 和 AD824 的优势，使用时应该注意以下几个问题。

1.1 输入信号有可能出现大于 $+V_S$ 时，运算放大器的同相输入端串联一个电阻，典型值为 1kΩ，就能防止输入信号的相位反相，但将产生附加的输入电压噪声。

1.2 由于运算放大器 AD820、AD822、AD824 运算放大器输入级采用 N 沟道的场效应晶体管，在正常工作时，输入电流是负的，电流从输入端流出。如果输入端电压大于 $+V_S-0.4V$ 时，则使器件内部结点变成正向偏置，输入电流方向相反。为了防止产生这种现象，使用时要求在输入端串联一个电阻（典型值在 1kΩ～10kΩ）。同时，该电阻还能起限流作用，防止输入电压大于 $+V_S+0.3V$ 或者在 $\pm V_S=0$，输入端有输入电压时，使运算放大器的输入电流过大而损坏器件。

当输入电压是负电压时，运算放大器允许输入电压小于 $-V_S$ 极限状态，允许输入电压比 $-V_S$ 还低 20V。因此采用单电源工作模式时，运算放大器的输入端也允许输入负电压信号，而不损坏器件。但是在任何状态，运算放大器的正电源电压值与负信号输入电压幅值的绝对值二者之和不大于 36V，就能保证器件正常工作，否则就要损坏器件。在正常工作状态时，输入端的输入电流是皮安级。

1.3 放大器开环增益特性会随负载状况而变化，当负载电阻超过 20kΩ，运算放大器的输出电压与输入电压之比实际上无变化。如果运算放大器的输出电压过高，因器件输

出电压在二个方向中的任何一个达到或大于饱和电压，那么就会在 2μs 内，输入端恢复到工作区域。

AD820、AD822 和 AD824 任何一种运算放大器都能与 555 定时器组合成一个高精度的电压频率转换器，具体电路如图 2 所示。

在图中运算放大器驱动 555 定时器，产生一个脉宽为 t_1 的稳定脉冲，正向的输出脉冲由 R2－C2 积分作为运算放大器的一个输入信号，另一个信号就是输入信号 V_{in}。这样运算放大器就成为差动积分器，该电路使用 5V 单电源供电时，供电电流小于 1mA，线性误差优于满量程的 0.01%。

利用 AD822 运算放大器和 AD620 仪表放大器能够很方便地组成一个低噪声的双极性电桥驱动器，它的原理图如图 3 所示。

在图中，AD822 运算放大器用来驱动 350Ω 的单臂惠登斯电桥（Wheatstone B ridge），AD822 的一个放大器为 1.235V 小功率基准源 AD589 的缓冲器，放大器输出 4.5V 电压作为 A/D 转换器的输入信号。AD822 中的另一个放大器构成一个单位增益放大器，它产生电桥的另一个输入信号－4.5V 电压。电阻 R1 和 R2 为电桥激励提供恒定电流。AD620 仪表

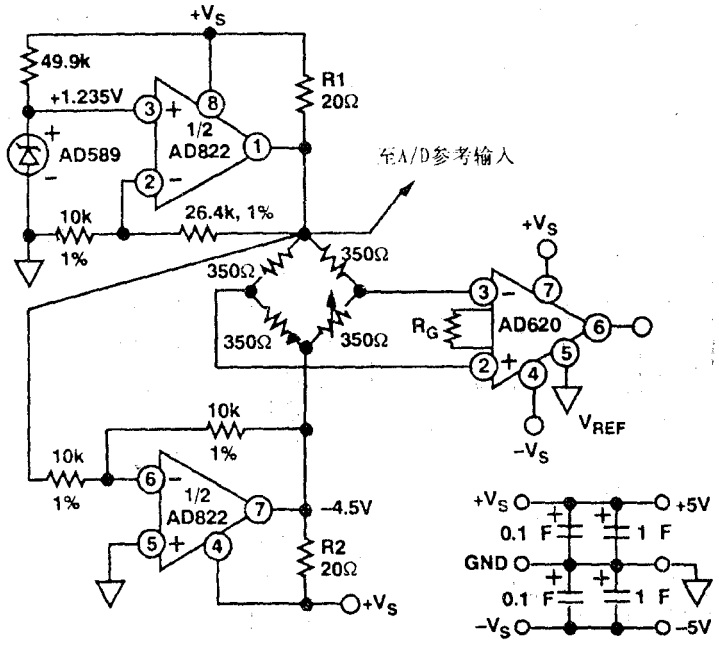


图 3　低噪声双极性电桥驱动器原理图

表　1：AD820，AD822 和 AD824 运算放大器主要性能指标

参数名称	AD820	AD822	AD824
失调电压	0.4mV	0.5mV	0.5mV
失调电压温度漂移	2μV/℃	2μV/℃	2μV/℃
输入电压器噪声	16mV/ $\sqrt{Hz}$	16mV/ $\sqrt{Hz}$	16mV/ $\sqrt{Hz}$
共模抑制比	80dB	80dB	80dB
差动输入阻抗	10^{13}/0.5pf	10^{13}/0.5pf	10^{13}/0.5pf
共模输入阻抗	10^{13}/2.8pf	10^{13}/2.8pf	10^{13}/2.8pf
共模电压范围	－15.2～14V	－15.2～14V	－15.2～14V
开环增益	2000V/mV	2000V/mV	
单线增益频率	1.9MHz	1.9MHz	2.0MHz
转换速率	3V/μs	3V/μs	3V/μs
建立时间达到(0.01%)	4.5μs	4.5μs	6μs
输入饱和电压 V_{OL} － V_{EE}	5mV	5mV	
电源电压(最大值)	±18V	±18V	±18V
输入电压(最大值)	$+V_S$+0.2V 到－(20V+V_S)	$+V_S$+0.2V 到－(20V+V_S)	－(V_S+0.2V)到 V_S
差动输入电压(最大值)	±30V	±30V	±30V

注：表 1 中的数据都是各运算放大器在±15V 电源电压条件下得出的典型值。

放大器用来决定电桥的差动输出电压。AD620 的增益决定于外接电阻 R_G。

由下式计算增益：

$$G=\frac{49.4K\Omega}{R_G}+1$$

由于 AD820、AD822 和 AD824 具有优异的电气性能，特别是在 3V 单电源供电时所具有的电流驱动特性，低总谐波失真和噪声的特性，利用一个 AD822 能够组成高保真的立体声耳机驱动电路。具体电路如图 4 所示。

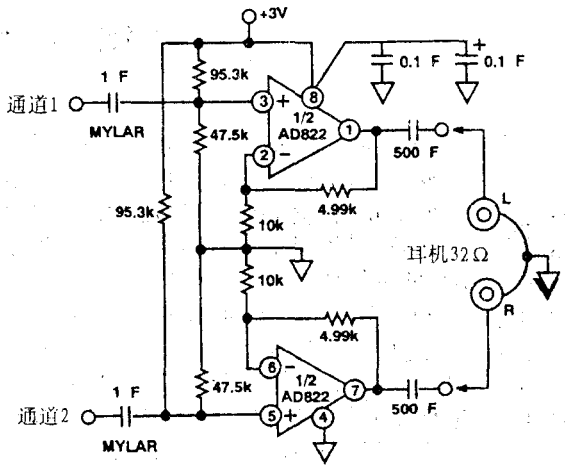


图 4 3V 单电源高保真立体声耳机驱动电路原理图

在电源中耦合电容器采用聚酯薄膜电容器，耦合电容 500μF，与耳机组成了一个截止频率 5Hz 的高通滤波器，它确保音频信号全部通过。在 1kHz，300mV$_{P-P}$输出信号时，该电路总谐波失真系数与噪声之和等于－62dB (0.079%)。

AD820、AD822、AD824 运算放大器能够广泛地应用于各个领域，尤其是在单电源供电的条件下，是设计人员和首选器件。

参考资料：

1、Analog Device Inc Single supply Rail－Io－Rail Low Power FET－Input Op Amp Data Sheet 1996

2、Analog Device Inc Design－in Reference Manual 1994。

编者注：

由于篇幅所限，有关的应用例子不再介绍，如需要进一步了解和购买，请与英赛尔器件集团所属各公司联系，联系地址见英赛器件集团的广告。

咨询编号：970710

Single Supply, Rail to Rail Low Power FET-Input Op Amp

AD820

FEATURES

TRUE SINGLE SUPPLY OPERATION
- Output Swings Rail to Rail
- Input Voltage Range Extends Below Ground
- Single Supply Capability from +3 V to +36 V
- Dual Supply Capability from ±1.5 V to ±18 V

EXCELLENT LOAD DRIVE
- Capacitive Load Drive Up to 350 pF
- Minimum Output Current of 15 mA

EXCELLENT AC PERFORMANCE FOR LOW POWER
- 800 μA Max Quiescent Current
- Unity Gain Bandwidth: 1.8 MHz
- Slew Rate of 3.0 V/μs

EXCELLENT DC PERFORMANCE
- 800 μV Max Input Offset Voltage
- 1 μV/°C Typ Offset Voltage Drift
- 25 pA Max Input Bias Current

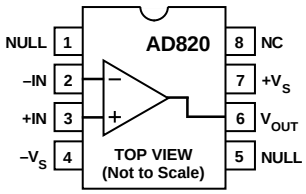
LOW NOISE
- 13 nV/$\sqrt{\text{Hz}}$ @ 10 kHz

APPLICATIONS

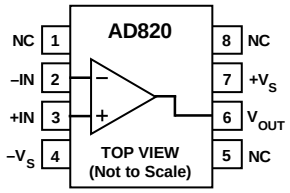
Battery Powered Precision Instrumentation
Photodiode Preamps
Active Filters
12- to 14-Bit Data Acquisition Systems
Medical Instrumentation
Low Power References and Regulators

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP



8-Pin SOIC



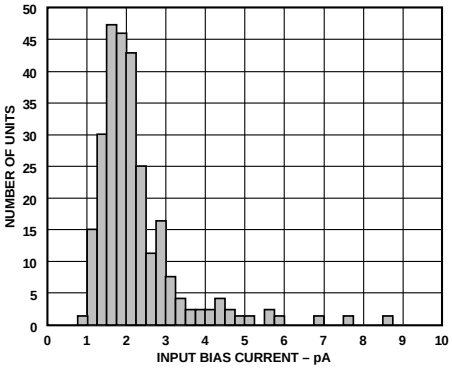
PRODUCT DESCRIPTION

The AD820 is a precision, low power FET input op amp that can operate from a single supply of +3.0 V to 36 V, or dual supplies of ±1.5 V to ±18 V. It has true single supply capability with an input voltage range extending below the negative rail, allowing the AD820 to accommodate input signals below ground in the single supply mode. Output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range.

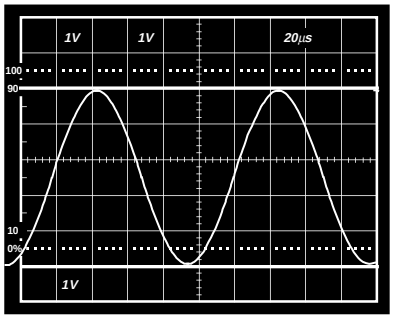
Offset voltage of 800 μV max, offset voltage drift of 1 μV/°C, typ input bias currents below 25 pA and low input voltage noise provide dc precision with source impedances up to a Gigaohm. 1.8 MHz unity gain bandwidth, –93 dB THD at 10 kHz and 3 V/μs slew rate are provided for a low supply current of 800 μA. The AD820 drives up to 350 pF of direct capacitive load and provides a minimum output current of 15 mA. This allows the amplifier to handle a wide range of load conditions. This combination of ac and dc performance, plus the outstanding load drive capability, results in an exceptionally versatile amplifier for the single supply user.

The AD820 is available in three performance grades. The A and B grades are rated over the industrial temperature range of –40°C to +85°C. There is 3 volt grade—the AD820A-3V, rated over the industrial temperature range.

The AD820 is offered in two varieties of 8-pin package: plastic DIP, and surface mount (SOIC).



Input Voltage Noise vs. Frequency



Gain of +2 Amplifier; V_S = +5, 0, V_{IN} = 2.5 V Sine Centered at 1.25 Volts

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD820—SPECIFICATIONS (V_S = 0, 5 volts (@ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.1	0.4	mV
Max Offset over Temperature			0.5	1.2		0.5	0.9	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_O = 0 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 4 V							
	R_L = 100k	400	1000		500	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	15	30		15	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		$nV/\sqrt{Hz}$
f = 100 Hz			21			21		$nV/\sqrt{Hz}$
f = 1 kHz			16			16		$nV/\sqrt{Hz}$
f = 10 kHz			13			13		$nV/\sqrt{Hz}$
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		$fA/\sqrt{Hz}$
Harmonic Distortion	R_L = 10k to 2.5 V							
f = 10 kHz	V_O = 0.25 V to 4.75 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.8			1.8		MHz
Full Power Response	V_O p-p = 4.5 V		210			210		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0.2 V to 4.5 V		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–0.2		4	–0.2		4	V
T_{MIN} to T_{MAX}		–0.2		4	–0.2		4	V
CMRR	V_{CM} = 0 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|0.5$			$10^{13}\|0.5$		Ω|pF
Common Mode			$10^{13}\|2.8$			$10^{13}\|2.8$		Ω|pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			25			25		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		620	800		620	800	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		66	80		dB
T_{MIN} to T_{MAX}		70			66			dB

(V_S = +5 volts (@ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.1	0.8		0.3	0.4	mV
Max Offset over Temperature			0.5	1.5		0.5	1	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = –5 V to 4 V		2	25		2	10	pA
at T_{MAX}			0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = 4 V to –4 V							
	R_L = 100k	400	1000		400	1000		V/mV
T_{MIN} to T_{MAX}		400			400			V/mV
	R_L = 10k	80	150		80	150		V/mV
T_{MIN} to T_{MAX}		80			80			V/mV
	R_L = 1k	20	30		20	30		V/mV
T_{MIN} to T_{MAX}		10			10			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		$nV/\sqrt{Hz}$
f = 100 Hz			21			21		$nV/\sqrt{Hz}$
f = 1 kHz			16			16		$nV/\sqrt{Hz}$
f = 10 kHz			13			13		$nV/\sqrt{Hz}$
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		$fA/\sqrt{Hz}$
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±4.5 V		–93			–93		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.8		MHz
Full Power Response	V_O p-p = 9 V		105			105		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±4.5 V		1.4			1.4		µs
to 0.01%			1.8			1.8		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–5.2		4	–5.2		4	V
T_{MIN} to T_{MAX}		–5.2		4	–5.2		4	V
CMRR	V_{CM} = –5 V to +2 V	66	80		72	80		dB
T_{MIN} to T_{MAX}		66			66			dB
Input Impedance								
Differential			$10^{13}\|\|0.5$			$10^{13}\|\|0.5$		Ω||pF
Common Mode			$10^{13}\|\|2.8$			$10^{13}\|\|2.8$		Ω||pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		15			15			mA
T_{MIN} to T_{MAX}		12			12			mA
Short Circuit Current			30			30		mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		650	800		620	800	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

AD820–SPECIFICATIONS (V_S = ±15 volts (@ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0 V unless otherwise noted)

Parameter	Conditions	AD820A Min	AD820A Typ	AD820A Max	AD820B Min	AD820B Typ	AD820B Max	Units
DC PERFORMANCE								
Initial Offset			0.4	2		0.3	1.0	mV
Max Offset over Temperature			0.5	3		0.5	2	mV
Offset Drift			2			2		µV/°C
Input Bias Current	V_{CM} = 0 V		2	25		2	10	pA
	V_{CM} = –10 V		40			40		pA
at T_{MAX}	V_{CM} = 0 V		0.5	5		0.5	2.5	nA
Input Offset Current			2	20		2	10	pA
at T_{MAX}			0.5			0.5		nA
Open-Loop Gain	V_O = +10 V to –10 V							
	R_L = 100k	500	2000		500	2000		V/mV
T_{MIN} to T_{MAX}		500			500			V/mV
	R_L = 10k	100	500		100	500		V/mV
T_{MIN} to T_{MAX}		100			100			V/mV
	R_L = 1k	30	45		30	45		V/mV
T_{MIN} to T_{MAX}		20			20			V/mV
NOISE/HARMONIC PERFORMANCE								
Input Voltage Noise								
0.1 Hz to 10 Hz			2			2		µV p-p
f = 10 Hz			25			25		$nV/\sqrt{Hz}$
f = 100 Hz			21			21		$nV/\sqrt{Hz}$
f = 1 kHz			16			16		$nV/\sqrt{Hz}$
f = 10 kHz			13			13		$nV/\sqrt{Hz}$
Input Current Noise								
0.1 Hz to 10 Hz			18			18		fA p-p
f = 1 kHz			0.8			0.8		$fA/\sqrt{Hz}$
Harmonic Distortion	R_L = 10k							
f = 10 kHz	V_O = ±10 V		–85			–85		dB
DYNAMIC PERFORMANCE								
Unity Gain Frequency			1.9			1.9		MHz
Full Power Response	V_O p-p = 20 V		45			45		kHz
Slew Rate			3			3		V/µs
Settling Time								
to 0.1%	V_O = 0 V to ±10 V		4.1			4.1		µs
to 0.01%			4.5			4.5		µs
INPUT CHARACTERISTICS								
Common-Mode Voltage Range[1]		–15.2		14	–15.2		14	V
T_{MIN} to T_{MAX}		–15.2		14	–15.2		14	V
CMRR	V_{CM} = –15 V to 12 V	70	80		74	90		dB
T_{MIN} to T_{MAX}		70			74			dB
Input Impedance								
Differential			$10^{13}\|\|0.5$			$10^{13}\|\|0.5$		Ω||pF
Common Mode			$10^{13}\|\|2.8$			$10^{13}\|\|2.8$		Ω||pF
OUTPUT CHARACTERISTICS								
Output Saturation Voltage[2]								
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7		5	7	mV
T_{MIN} to T_{MAX}				10			10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14		10	14	mV
T_{MIN} to T_{MAX}				20			20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55		40	55	mV
T_{MIN} to T_{MAX}				80			80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110		80	110	mV
T_{MIN} to T_{MAX}				160			160	mV
V_{OL}–V_{EE}	I_{SINK} = 15 mA		300	500		300	500	mV
T_{MIN} to T_{MAX}				1000			1000	mV
V_{CC}–V_{OH}	I_{SOURCE} = 15 mA		800	1500		800	1500	mV
T_{MIN} to T_{MAX}				1900			1900	mV
Operating Output Current		20			20			mA
T_{MIN} to T_{MAX}		15			15			mA
Short Circuit Current			45			45		mA
T_{MIN} to T_{MAX}								mA
Capacitive Load Drive			350			350		pF
POWER SUPPLY								
Quiescent Current	T_{MIN} to T_{MAX}		700	900		700	900	µA
Power Supply Rejection	V_S+ = 5 V to 15 V	70	80		70	80		dB
T_{MIN} to T_{MAX}		70			70			dB

(V_S = 0, 3 volts (@ T_A = +25°C, V_{CM} = 0 V, V_{OUT} = 0.2 V unless otherwise noted)

Parameter	Conditions	AD820A-3V Min	Typ	Max	Units
DC PERFORMANCE					
Initial Offset			0.2	1	mV
Max Offset over Temperature			0.5	1.5	mV
Offset Drift			1		µV/°C
Input Bias Current	V_{CM} = 0 V to +2 V		2	25	pA
at T_{MAX}			0.5	5	nA
Input Offset Current			2	20	pA
at T_{MAX}			0.5		nA
Open-Loop Gain	V_O = 0.2 V to 2 V				
	R_L = 100k	300	1000		V/mV
T_{MIN} to T_{MAX}		400			V/mV
	R_L = 10k	60	150		V/mV
T_{MIN} to T_{MAX}		80			V/mV
	R_L = 1k	10	30		V/mV
T_{MIN} to T_{MAX}		8			V/mV
NOISE/HARMONIC PERFORMANCE					
Input Voltage Noise					
0.1 Hz to 10 Hz			2		µV p-p
f = 10 Hz			25		nV/√Hz
f = 100 Hz			21		nV/√Hz
f = 1 kHz			16		nV/√Hz
f = 10 kHz			13		nV/√Hz
Input Current Noise					
0.1 Hz to 10 Hz			18		fA p-p
f = 1 kHz			0.8		fA/√Hz
Harmonic Distortion	R_L = 10k to 1.5 V				
f = 10 kHz	V_O = ±1.25 V		–92		dB
DYNAMIC PERFORMANCE					
Unity Gain Frequency			1.5		MHz
Full Power Response	V_O p-p = 2.5 V		240		kHz
Slew Rate			3		V/µs
Settling Time					
to 0.1%	V_O = 0.2 V to 2.5 V		1		µs
to 0.01%			1.4		µs
INPUT CHARACTERISTICS					
Common-Mode Voltage Range[1]		–0.2		2	V
T_{MIN} to T_{MAX}		–0.2		2	V
CMRR	V_{CM} = 0 V to +1 V	60	74		dB
T_{MIN} to T_{MAX}		60			dB
Input Impedance					
Differential			$10^{13}\|\|0.5$		Ω||pF
Common Mode			$10^{13}\|\|2.8$		Ω||pF
OUTPUT CHARACTERISTICS					
Output Saturation Voltage[2]					
V_{OL}–V_{EE}	I_{SINK} = 20 µA		5	7	mV
T_{MIN} to T_{MAX}				10	mV
V_{CC}–V_{OH}	I_{SOURCE} = 20 µA		10	14	mV
T_{MIN} to T_{MAX}				20	mV
V_{OL}–V_{EE}	I_{SINK} = 2 mA		40	55	mV
T_{MIN} to T_{MAX}				80	mV
V_{CC}–V_{OH}	I_{SOURCE} = 2 mA		80	110	mV
T_{MIN} to T_{MAX}				160	mV
V_{OL}–V_{EE}	I_{SINK} = 10 mA		200	400	mV
T_{MIN} to T_{MAX}				400	mV
V_{CC}–V_{OH}	I_{SOURCE} = 10 mA		500	1000	mV
T_{MIN} to T_{MAX}				1000	mV
Operating Output Current		15			mA
T_{MIN} to T_{MAX}		12			mA
Short Circuit Current		18	25		mA
T_{MIN} to T_{MAX}		15			mA
Capacitive Load Drive			350		pF
POWER SUPPLY					
Quiescent Current	T_{MIN} to T_{MAX}		620	800	µA
Power Supply Rejection	V_S+ = 3 V to 15 V	70	80		dB
T_{MIN} to T_{MAX}		70			dB

NOTES
[1]This is a functional specification. Amplifier bandwidth decreases when the input common-mode voltage is driven in the range ($+V_S$ –1 V) to $+V_S$. Common-mode error voltage is typically less than 5 mV with the common-mode voltage set at 1 volt below the positive supply.
[2]V_{OL}–V_{EE} is defined as the difference between the lowest possible output voltage (V_{OL}) and the minus voltage supply rail (V_{EE}). V_{CC}–V_{OH} is defined as the difference between the highest possible output voltage (V_{OH}) and the positive supply voltage (V_{CC}).
Specifications subject to change without notice.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD820 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic DIP (N) . . . . . 1.6 Watts
  SOIC (R) . . . . . 1.0 Watts
Input Voltage . . . . . ($+V_S$ + 0.2 V) to – (20 V + V_S)
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±30 V
Storage Temperature Range (N) . . . . . –65°C to +125°C
Storage Temperature Range (R) . . . . . –65°C to +150°C
Operating Temperature Range
  AD820A/B . . . . . –40°C to +85°C
Lead Temperature Range
  (Soldering 60 sec) . . . . . +260°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 160°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description
AD820AN	–40°C to +85°C	8-Pin Plastic Mini-DIP
AD820BN	–40°C to +85°C	8-Pin Plastic Mini-DIP
AD820AR	–40°C to +85°C	8-Pin SOIC
AD820BR	–40°C to +85°C	8-Pin SOIC
AD820AR-3V	–40°C to +85°C	8-Pin SOIC
AD820AN-3V	–40°C to +85°C	8-Pin Plastic Mini-DIP

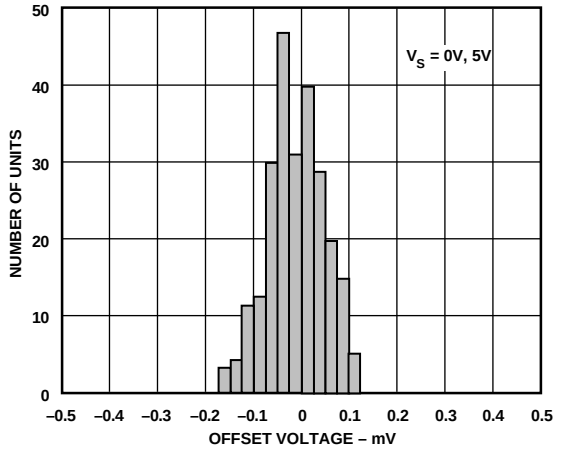


Figure 1. Typical Distribution of Offset Voltage (248 Units)

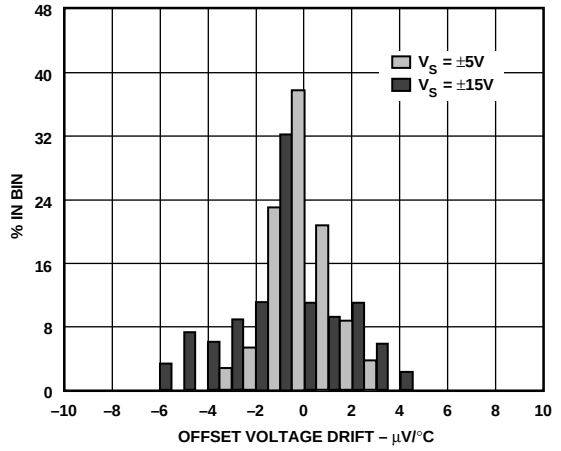


Figure 2. Typical Distribution of Offset Voltage Drift (120 Units)

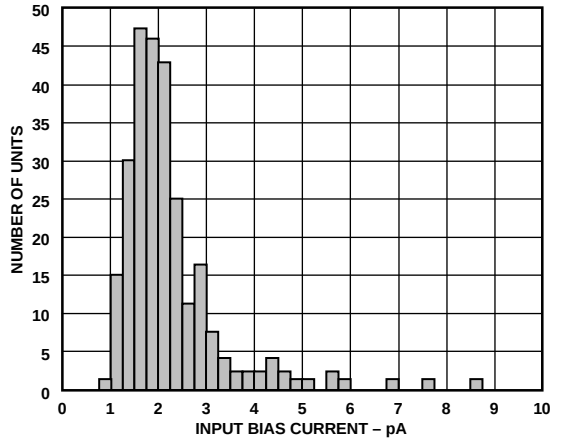


Figure 3. Typical Distribution of Input Bias Current (213 Units)

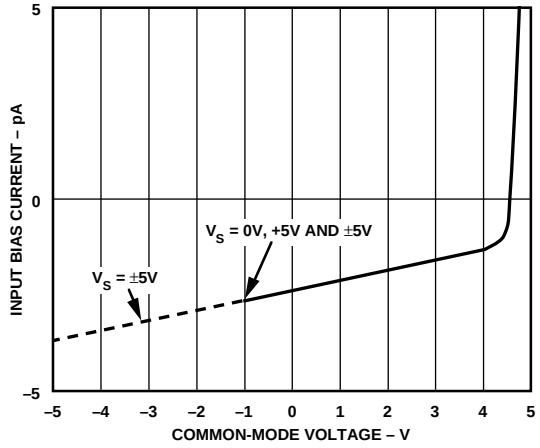


Figure 4. Input Bias Current vs. Common-Mode Voltage; V_S = +5 V, 0 V and V_S = ±5 V

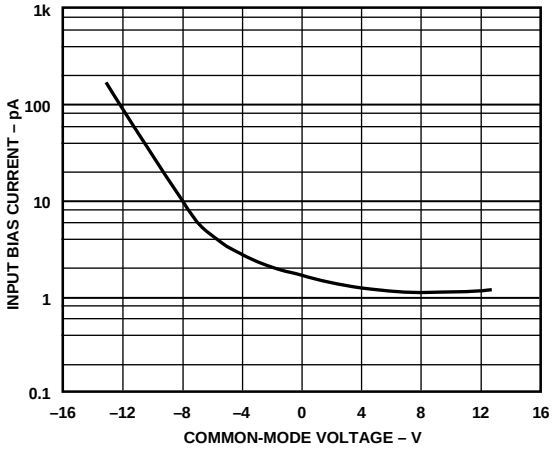


Figure 5. Input Bias Current vs. Common-Mode Voltage; V_S = ±15 V

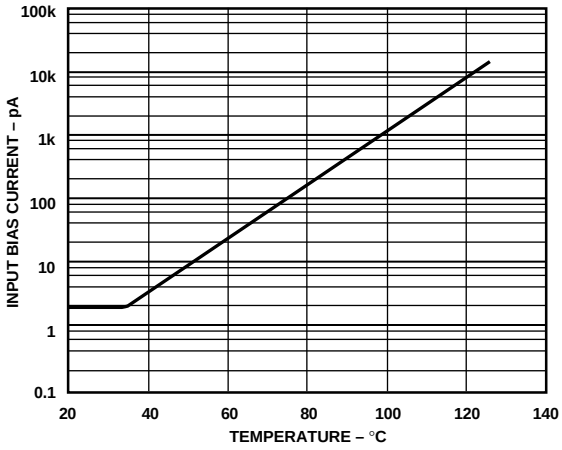


Figure 6. Input Bias Current vs. Temperature; V_S = 5 V, V_{CM} = 0

AD820–Typical Characteristics

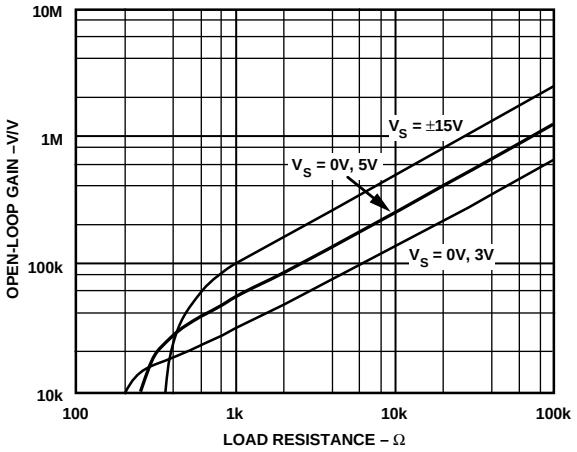


Figure 7. Open-Loop Gain vs. Load Resistance

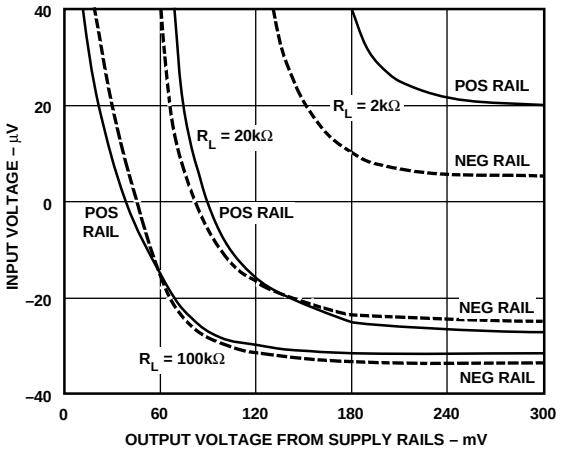


Figure 10. Input Error Voltage with Output Voltage within 300 mV of Either Supply Rail for Various Resistive Loads; V_S = ±5 V

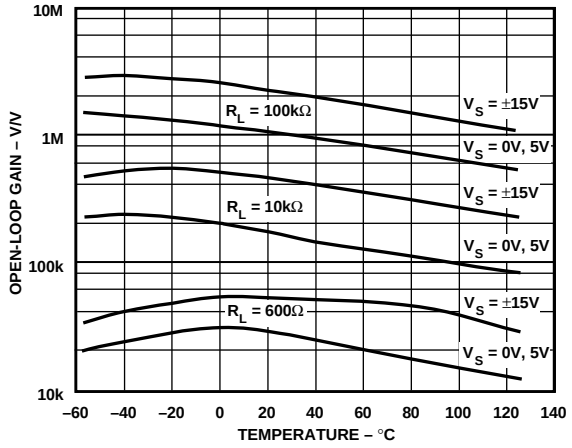


Figure 8. Open-Loop Gain vs. Temperature

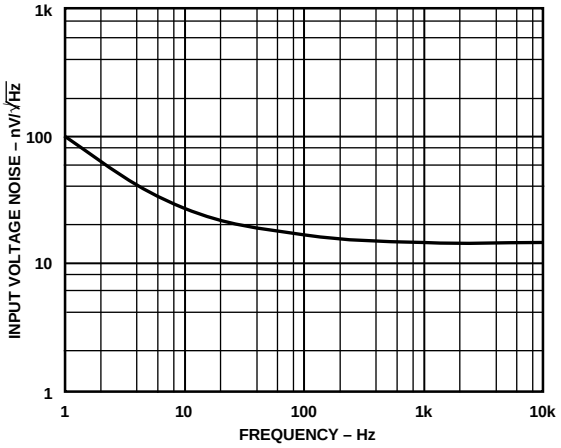


Figure 11. Input Voltage Noise vs. Frequency

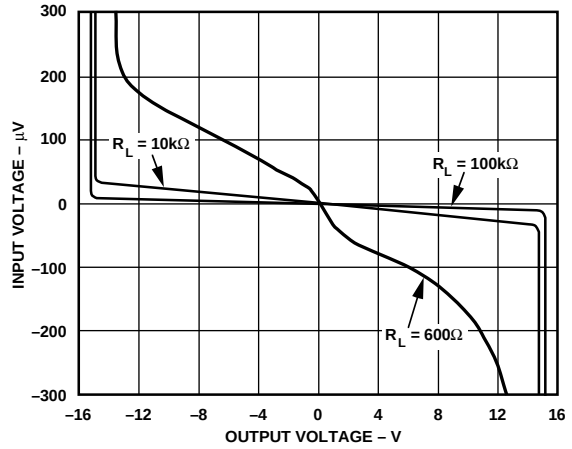


Figure 9. Input Error Voltage vs. Output Voltage for Resistive Loads

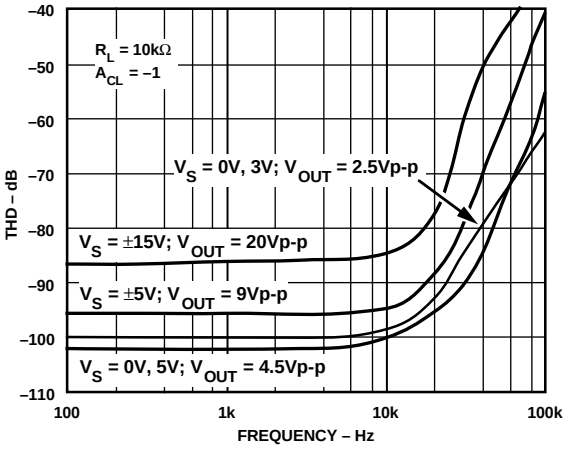


Figure 12. Total Harmonic Distortion vs. Frequency

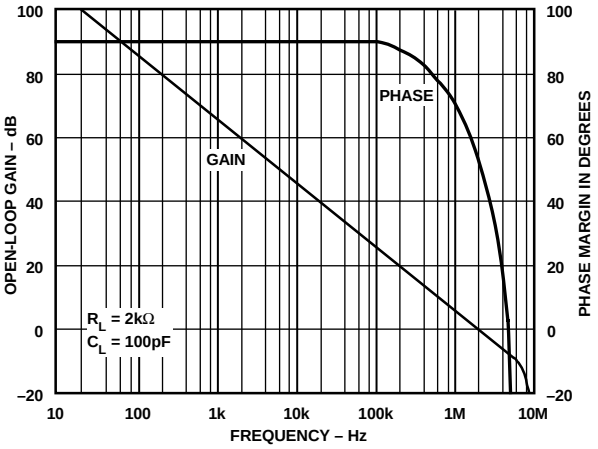


Figure 13. Open-Loop Gain and Phase Margin vs. Frequency

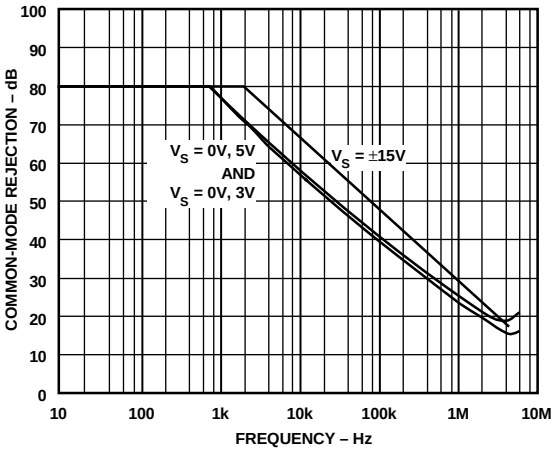


Figure 16. Common-Mode Rejection vs. Frequency

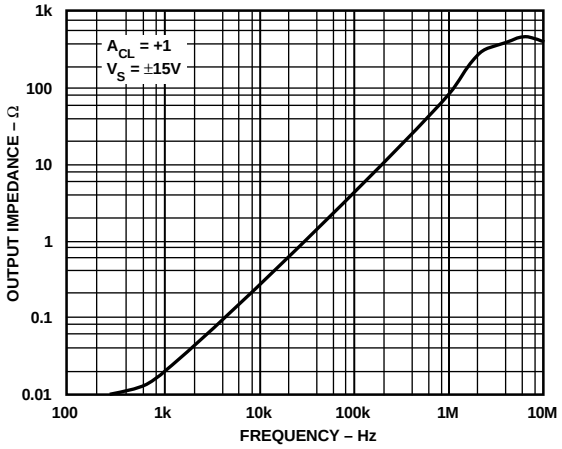


Figure 14. Output Impedance vs. Frequency

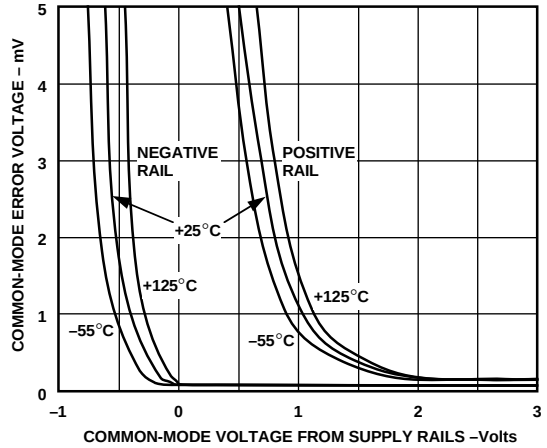


Figure 17. Absolute Common-Mode Error vs. Common-Mode Voltage from Supply Rails (V_S – V_{CM})

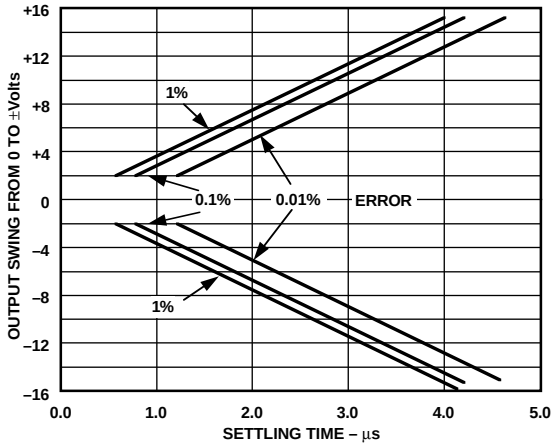


Figure 15. Output Swing and Error vs. Settling Time

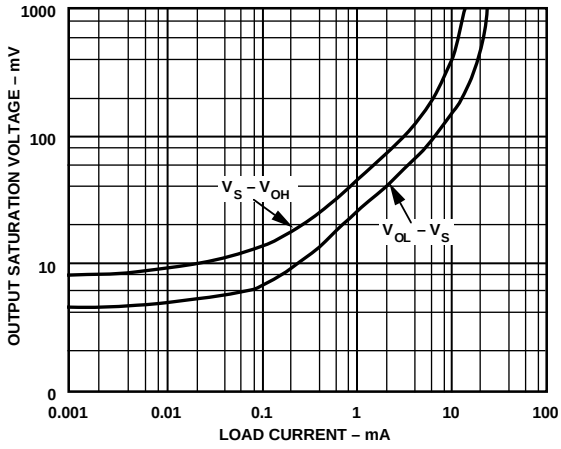


Figure 18. Output Saturation Voltage vs. Load Current

AD820–Typical Characteristics

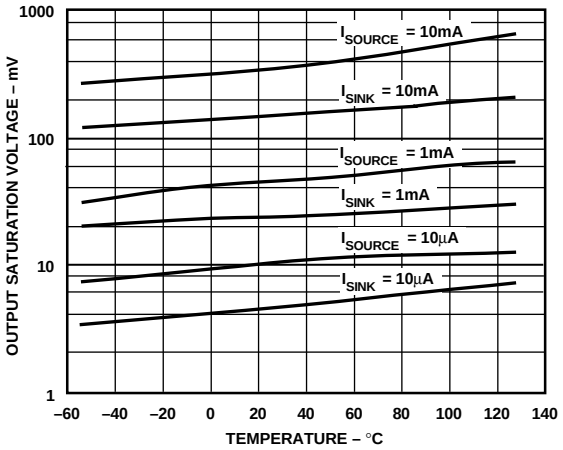


Figure 19. Output Saturation Voltage vs. Temperature

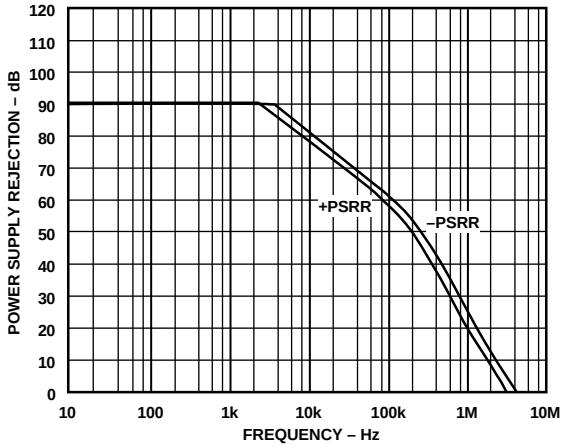


Figure 22. Power Supply Rejection vs. Frequency

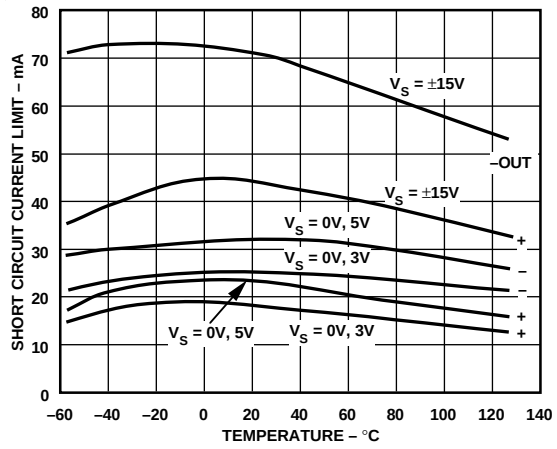


Figure 20. Short Circuit Current Limit vs. Temperature

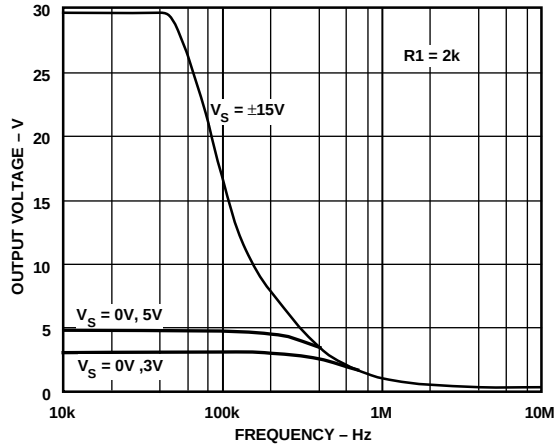


Figure 23. Large Signal Frequency Response

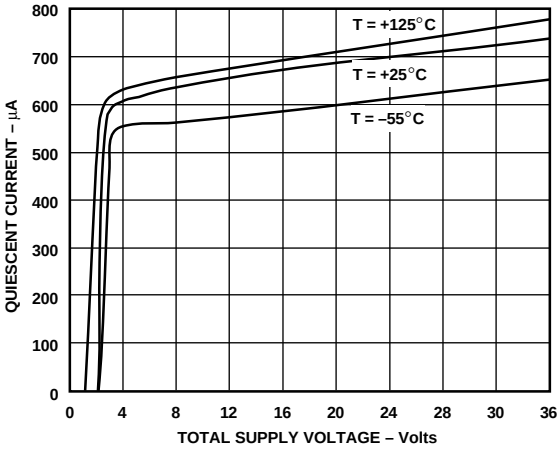


Figure 21. Quiescent Current vs. Supply Voltage vs. Temperature

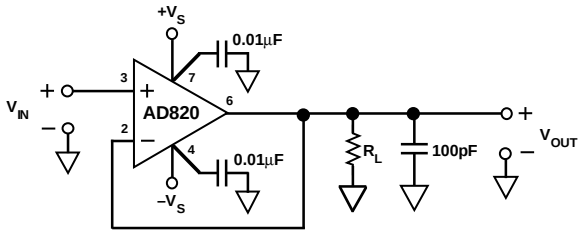


Figure 24. Unity-Gain Follower

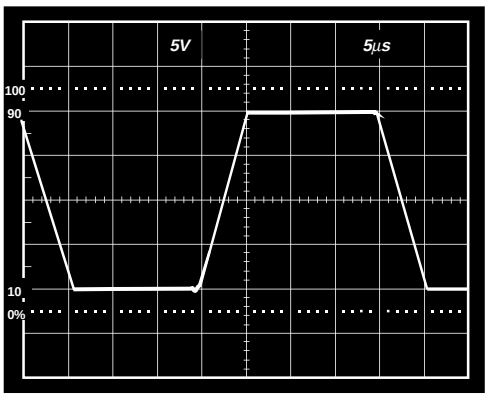


Figure 27. Large Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

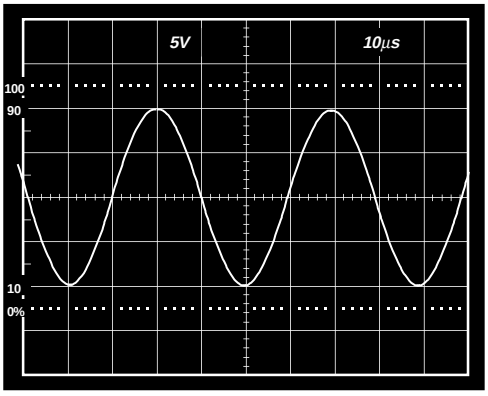


Figure 25. 20 V, 25 kHz Sine Input; Unity Gain Follower; $R_L = 600\ \Omega$, $V_S = \pm 15$ V

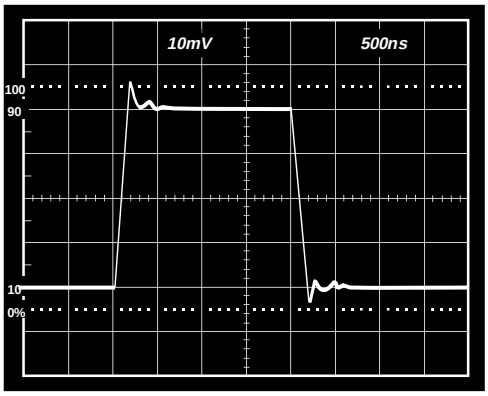


Figure 28. Small Signal Response Unity Gain Follower; $V_S = \pm 15$ V, $R_L = 10$ kΩ

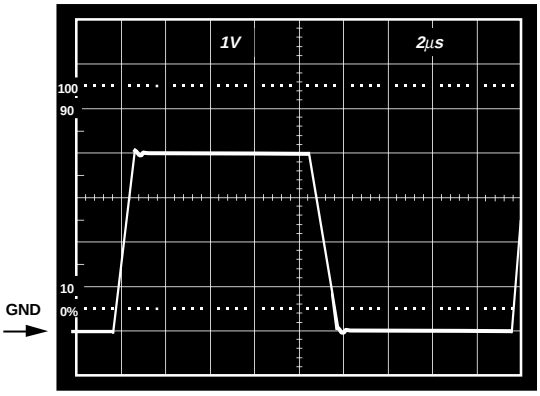


Figure 26. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 4 V Step

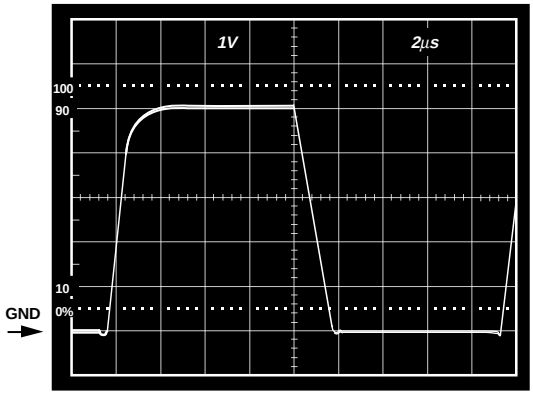


Figure 29. V_S = +5 V, 0 V; Unity Gain Follower Response to 0 V to 5 V Step

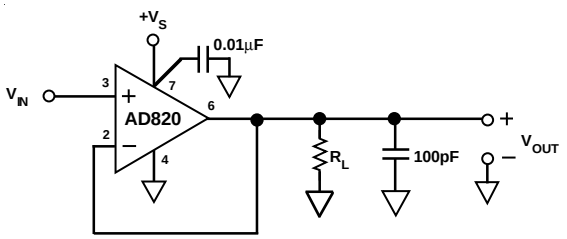


Figure 30. Unity-Gain Follower

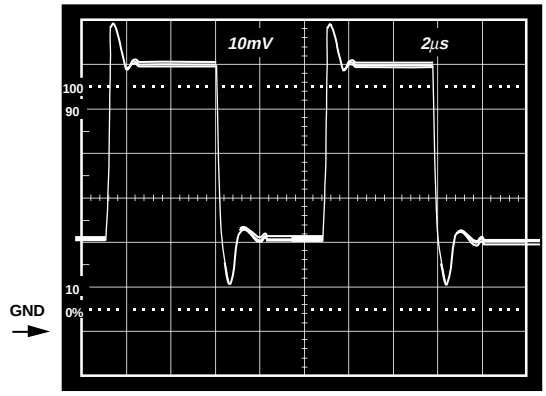


Figure 33. V_S = +5 V, 0 V; Unity Gain Follower Response to 40 mV Step Centered 40 mV Above Ground

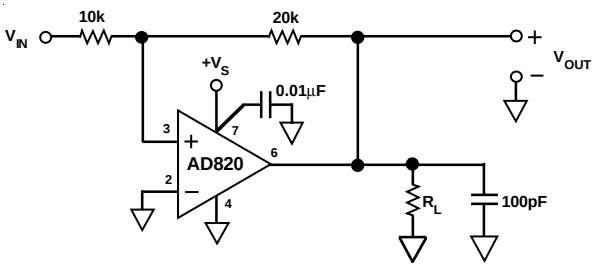


Figure 31. Gain of Two Inverter

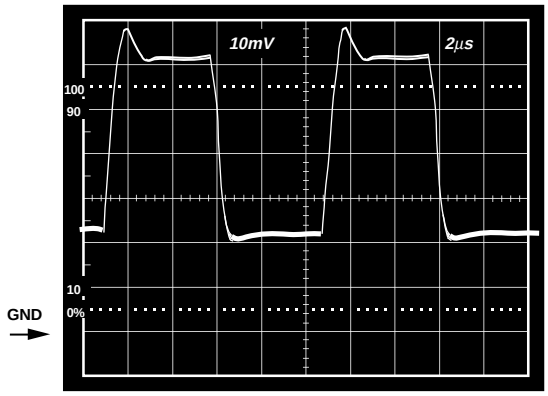


Figure 34. V_S = +5 V, 0 V; Gain of Two Inverter Response to 20 mV Step, Centered 20 mV Below Ground

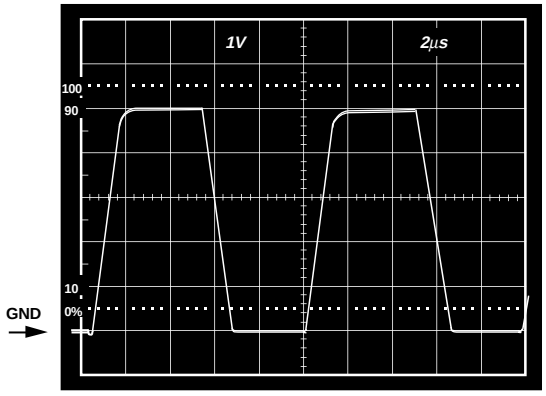


Figure 32. V_S = +5 V, 0 V; Gain of Two Inverter Response to 2.5 V Step Centered –1.25 V Below Ground

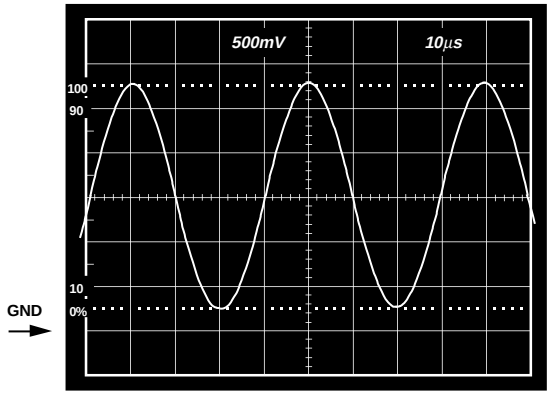


Figure 35. V_S = 3 V, 0 V; Gain of Two Inverter, V_{IN} = 1.25 V, 25 kHz, Sine Wave Centered at –0.75 V, R_L = 600 Ω

APPLICATION NOTES

INPUT CHARACTERISTICS

In the AD820, n-channel JFETs are used to provide a low offset, low noise, high impedance input stage. Minimum input common-mode voltage extends from 0.2 V below $-V_S$ to 1 V less than $+V_S$. Driving the input voltage closer to the positive rail will cause a loss of amplifier bandwidth (as can be seen by comparing the large signal responses shown in Figures 26 and 29) and increased common-mode voltage error as illustrated in Figure 17.

The AD820 does not exhibit phase reversal for input voltages up to and including $+V_S$. Figure 36a shows the response of an AD820 voltage follower to a 0 V to +5 V ($+V_S$) square wave input. The input and output are superimposed. The output polarity tracks the input polarity up to $+V_S$—no phase reversal. The reduced bandwidth above a 4 V input causes the rounding of the output wave form. For input voltages greater than $+V_S$, a resistor in series with the AD820's plus input will prevent phase reversal, at the expense of greater input voltage noise. This is illustrated in Figure 36b.

Since the input stage uses n-channel JFETs, input current during normal operation is negative; the current flows out from the input terminals. If the input voltage is driven more positive than $+V_S - 0.4$ V, the input current will reverse direction as internal device junctions become forward biased. This is illustrated in Figure 4.

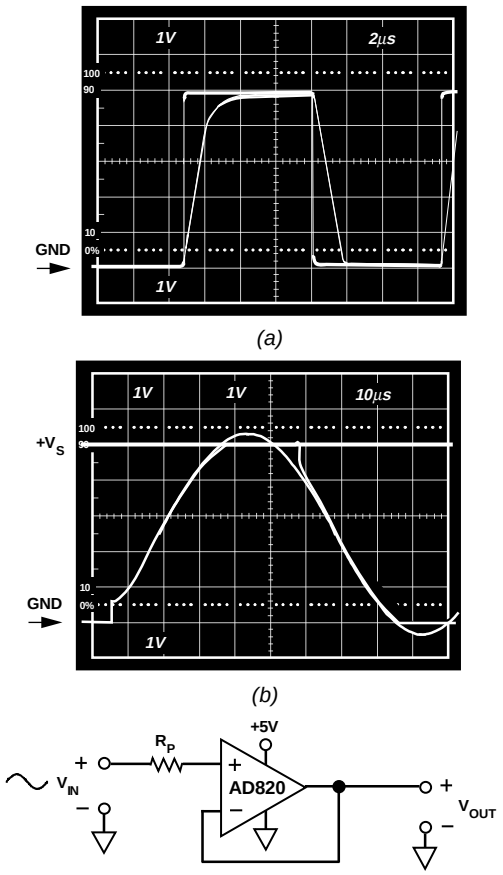


Figure 36. (a) Response with $R_P = 0$; V_{IN} from 0 to $+V_S$
(b) V_{IN} = 0 to $+V_S$ + 200 mV
V_{OUT} = 0 to $+V_S$
R_P = 49.9 kΩ

A current limiting resistor should be used in series with the input of the AD820 if there is a possibility of the input voltage exceeding the positive supply by more than 300 mV, or if an input voltage will be applied to the AD820 when $\pm V_S = 0$. The amplifier will be damaged if left in that condition for more than 10 seconds. A 1 kΩ resistor allows the amplifier to withstand up to 10 volts of continuous overvoltage, and increases the input voltage noise by a negligible amount.

Input voltages less than $-V_S$ are a completely different story. The amplifier can safely withstand input voltages 20 volts below the minus supply voltage as long as the total voltage from the positive supply to the input terminal is less than 36 volts. In addition, the input stage typically maintains picoamp level input currents across that input voltage range.

The AD820 is designed for 13 nV/$\sqrt{\text{Hz}}$ wideband input voltage noise and maintains low noise performance to low frequencies (refer to Figure 11). This noise performance, along with the AD820's low input current and current noise means that the AD820 contributes negligible noise for applications with source resistances greater than 10 kΩ and signal bandwidths greater than 1 kHz. This is illustrated in Figure 37.

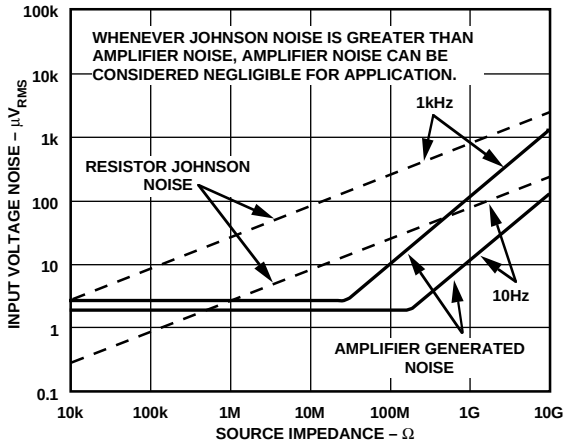


Figure 37. Total Noise vs. Source Impedance

OUTPUT CHARACTERISTICS

The AD820's unique bipolar rail-to-rail output stage swings within 5 mV of the minus supply and 10 mV of the positive supply with no external resistive load. The AD820's approximate output saturation resistance is 40 Ω sourcing and 20 Ω sinking. This can be used to estimate output saturation voltage when driving heavier current loads. For instance, when sourcing 5 mA, the saturation voltage to the positive supply rail will be 200 mV, when sinking 5 mA, the saturation voltage to the minus rail will he 100 mV.

The amplifier's open-loop gain characteristic will change as a function of resistive load, as shown in Figures 7 through 10. For load resistances over 20 kΩ, the AD820's input error voltage is virtually unchanged until the output voltage is driven to 180 mV of either supply.

If the AD820's output is driven hard against the output saturation voltage, it will recover within 2 µs of the input returning to the amplifier's linear operating region.

Direct capacitive load will interact with the amplifier's effective output impedance to form an additional pole in the amplifier's feedback loop, which can cause excessive peaking on the pulse response or loss of stability. Worst case is when the amplifier is used as a unity gain follower. Figure 38 shows the AD820's pulse response as a unity gain follower driving 350 pF. This amount of overshoot indicates approximately 20 degrees of phase margin—the system is stable, but is nearing the edge. Configurations with less loop gain, and as a result less loop bandwidth, will be much less sensitive to capacitance load effects. Figure 39 is a plot of capacitive load that will result in a 20 degree phase margin versus noise gain for the AD820. Noise gain is the inverse of the feedback attenuation factor provided by the feedback network in use.

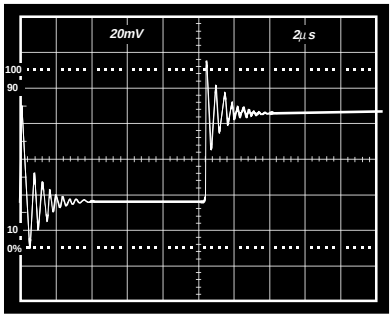


Figure 38. Small Signal Response of AD820 as Unity Gain Follower Driving 350 pF Capacitive Load

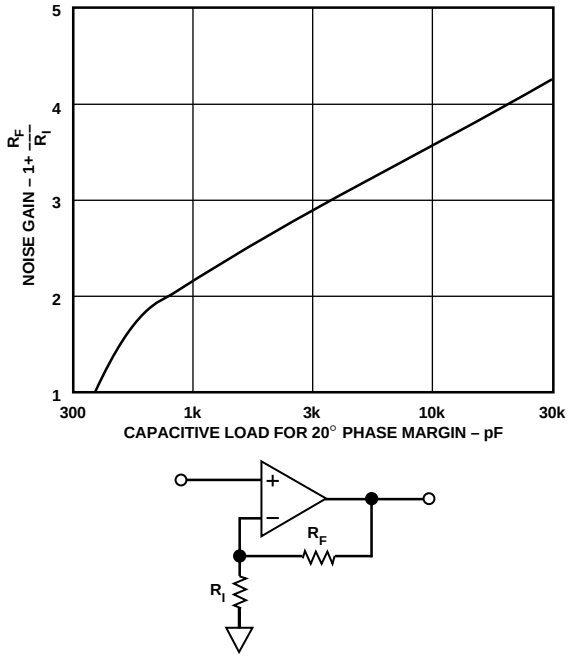


Figure 39. Capacitive Load Tolerance vs. Noise Gain

Figure 40 shows a possible configuration for extending capacitance load drive capability for a unity gain follower. With these component values, the circuit will drive 5,000 pF with a 10% overshoot.

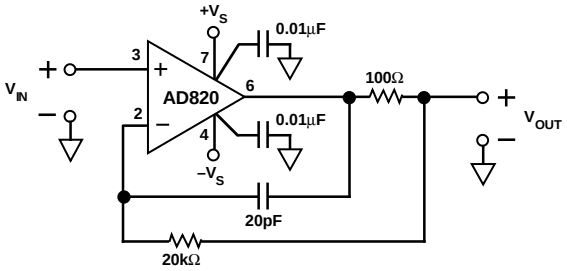


Figure 40. Extending Unity Gain Follower Capacitive Load Capability Beyond 350 pF

OFFSET VOLTAGE ADJUSTMENT

The AD820's offset voltage is low, so external offset voltage nulling is not usually required. Figure 41 shows the recommended technique for AD820's packaged in plastic DIPs. Adjusting offset voltage in this manner will change the offset voltage temperature drift by 4 μV/°C for every millivolt of induced offset. The null pins are not functional for AD820s in the SO-8 "R" package.

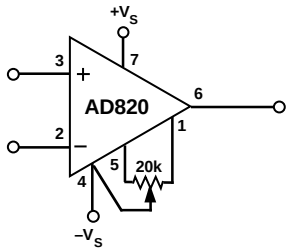


Figure 41. Offset Null

APPLICATIONS

Single Supply Half-Wave and Full-Wave Rectifiers

An AD820 configured as a unity gain follower and operated with a single supply can be used as a simple half-wave rectifier. The AD820's inputs maintain picoamp level input currents even when driven well below the minus supply. The rectifier puts that behavior to good use, maintaining an input impedance of over $10^{11}\Omega$ for input voltages from 1 volt from the positive supply to 20 volts below the negative supply.

The full and half-wave rectifier shown in Figure 42 operates as follows: when V_{IN} is above ground, R1 is bootstrapped through the unity gain follower A1 and the loop of amplifier A2. This forces the inputs of A2 to be equal, thus no current flows through R1 or R2, and the circuit output tracks the input. When V_{IN} is below ground, the output of A1 is forced to ground. The noninverting input of amplifier A2 sees the ground level output of A1, therefore A2 operates as a unity gain inverter. The output at node C is then a full-wave rectified version of the input. Node B is a buffered half-wave rectified version of the input. Input voltages up to ±18 volts can be rectified, depending on the voltage supply used.

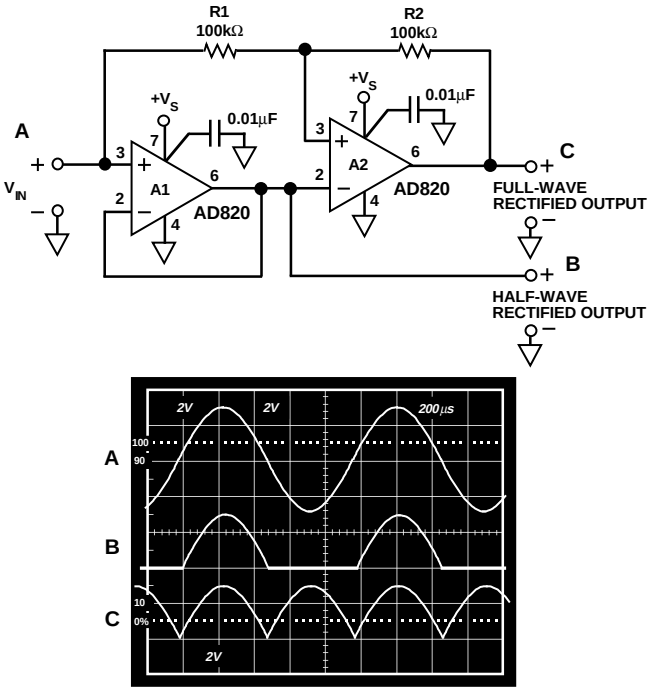


Figure 42. Single Supply Half- and Full-Wave Rectifier

4.5 Volt Low Dropout, Low Power Reference

The rail-to-rail performance of the AD820 can be used to provide low dropout performance for low power reference circuits powered with a single low voltage supply. Figure 43 shows a 4.5 volt reference using the AD820 and the AD680, a low power 2.5 volt bandgap reference. R2 and R3 set up the required gain of 1.8 to develop the 4.5 volt output. R1 and C2 form a low-pass RC filter to reduce the noise contribution of the AD680.

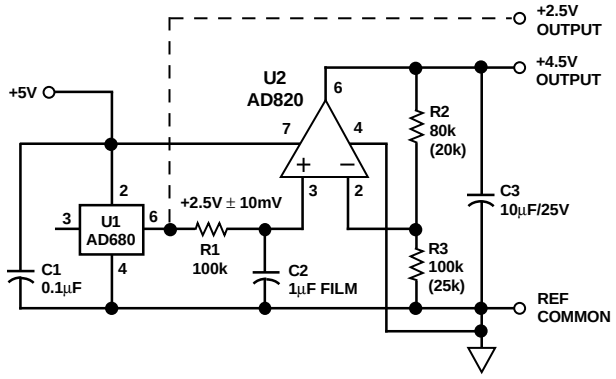


Figure 43. Single Supply 4.5 Volt Low Dropout Reference

With a 1 mA load, this reference maintains the 4.5 volt output with a supply voltage down to 4.7 volts. The amplitude of the recovery transient for a 1 mA to 10 mA step change in load current is under 20 mV, and settles out in a few microseconds. Output voltage noise is less than 10 μV rms in a 25 kHz noise bandwidth.

Low Power Three-Pole Sallen Key Low-Pass Filter

The AD820's high input impedance makes it a good selection for active filters. High value resistors can be used to construct low frequency filters with capacitors much less than 1 μF. The AD820's picoamp level input currents contribute minimal dc errors.

Figure 44 shows an example, a 10 Hz three-pole Sallen Key Filter. The high value used for R1 minimizes interaction with signal source resistance. Pole placement in this version of the filter minimizes the Q associated with the two-pole section of the filter. This eliminates any peaking of the noise contribution of resistors R1, R2, and R3, thus minimizing the inherent output voltage noise of the filter.

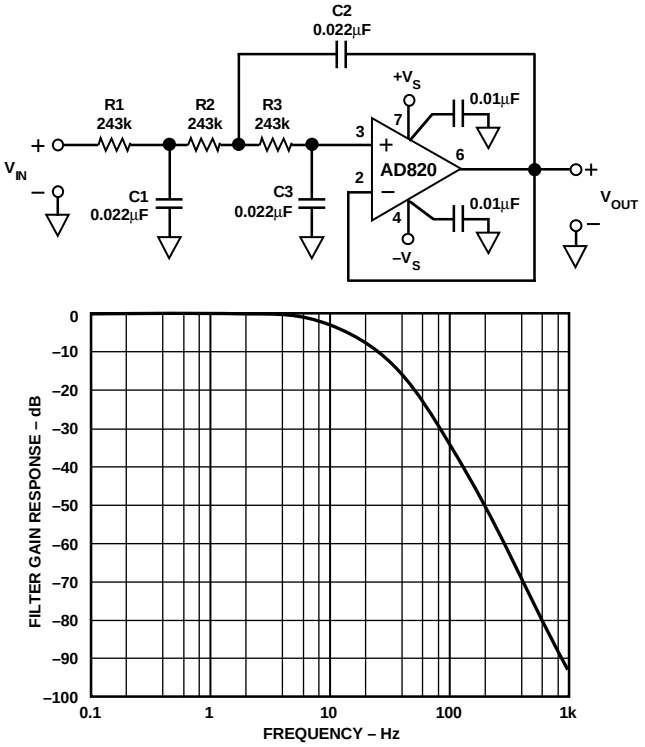
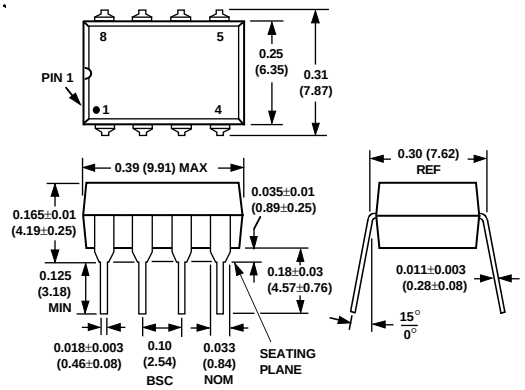


Figure 44. 10 Hz Sallen Key Low-Pass Filter

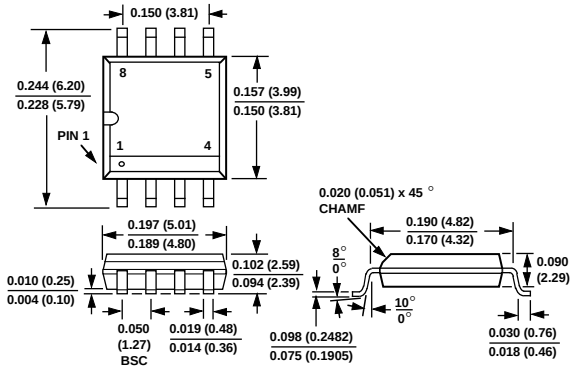
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Mini-DIP (N) Package



SOIC (R) Package



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