PLC810PG
HiperPLC系列

集成半桥驱动器的连续模式PFC和LLC控制器

产品特色

特性

- 集成度高，省去了额外的元件
- PFC与LLC的频率和相位同步
  - 降低了噪音和EMI
  - 降低PFC输出电容中的纹波电流
  - 避免边缘冲突技术可简化布板
- 全面的PFC和LLC故障处理及电流限制
- 拥有专利的连续导通模式PFC，效率高，元件成本低
- 高效率、零电压开关(ZVS)LLC
- 关断时间PFC控制可省去AC输入检测元件
- 可配置的精确的死区时间控制和频率限制
  - 防止MOSFET硬开关
- LLC占空比严格对称以平衡输出整流管电流
- 无铅无卤素的绿色封装

应用

- 32”至60” LCD电视机电源
- 150 W至600 W效率优化的离线式电源
- LED路灯

描述

PLC810PG集PFC及LLC离线式控制器与集成高电压半桥驱动器于一体。图1所示为采用PLC810PG器件的电源结构简图，其中LLC谐振电感集成在变压器中。PLC810PG的PFC部分采用无需正弦信号输入参考的通用输入连续电流模式(CCM)设计，从而减少了系统成本和外部元件。

DC-DC控制器驱动LLC谐振拓扑。这个变频控制器可使MOSFET在零电压时进行开关操作，从而消除大部分的开关损耗，提高效率。LLC控制器的核心是一个电流控制的振荡器，其频率控制范围支持电视机电源的传统工作频率。

为了确保零电压开关，PLC810PG中LLC开关的死区时间被严格控制在容差范围之内，并可通过一个外部电阻进行调节。高低压两端的占空比紧密匹配，以提供平衡的输出电流，从而降低输出二极管的成本。

典型PLC810PG LLC设计的工作频率为100 kHz（在额定工作条件下）。视LLC电路的设计而定，开关频率可以是额定工作频率的二分之一到三倍不等，这与输入电压和负载变化有关。

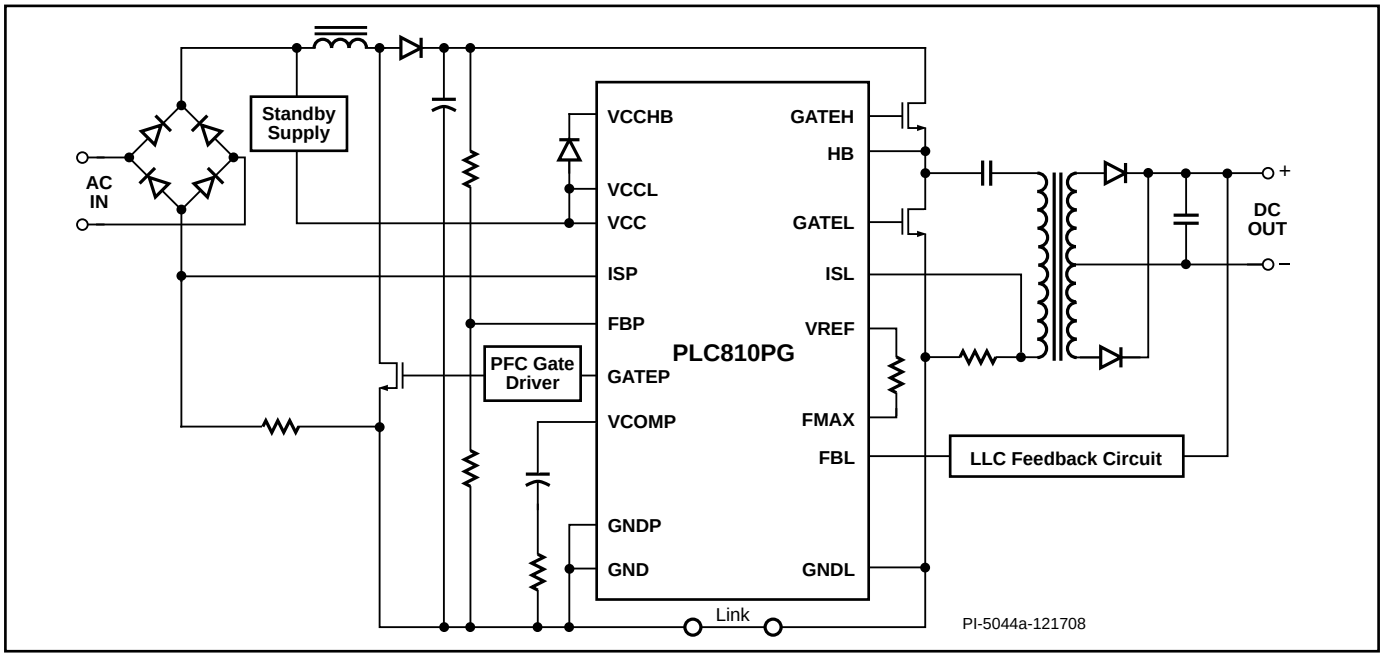


图 1. 典型应用电路 — LCD电视机电源

PFC转换器的频率锁定于LLC，以降低噪音和电磁干扰。在轻载时提高PFC频率与LLC同步可降低PFC升压转换器在转换为非连续模式时的电流，从而改善轻载工作状况和降低电源线谐波。该设计还提供PFC和LLC初级侧故障管理功能。

可根据LLC相位对PFC PWM输出相位进行动态调节，以便于开关沿与PWM和LLC时序电路中的噪音敏感部分不相交。避免边缘冲突技术可简化电源布板并提高性能。相位同步可降低EMI频谱成分和PFC电容的纹波电流。

引脚描述

VCC引脚

VCC
VCC为IC中的弱信号模拟电路供电。必须在VCC引脚和GND引脚间连接一个旁路电容。该电容应该为10 µF的陶瓷电容，或者是一个10 µF电解电容与一个0.1 µF陶瓷电容的并联组合。

VCCL
VCCL是LLC低压端驱动器的供电输入引脚。它仅为LLC低压端MOSFET驱动器以及模拟电路与LLC驱动器之间的通信电路供电。必须在VCC引脚和GNDL引脚之间连接一个1 µF的陶瓷旁路电容。该电容可提供瞬间电流用来导通LLC低压端MOSFET栅极。

VCCHB
VCCHB是LLC高压端驱动器的浮动供电输入引脚，以HB引脚为参考。反过来，HB引脚又连接到LLC MOSFET半桥中心点。必须，且必须在VCCHB引脚到HB引脚之间连接一个1 µF的陶瓷旁路电容。该电容可提供瞬间电流以导通LLC高压端LLC MOSFET的栅极。

在典型应用中，VCC与待机电源相连。VCCL应通过一个5 Ω电阻连接到VCC引脚，这样可以预防噪音。VCCHB通过一个高压二极管与一个5 Ω电阻组成的串联电路连接到待机电源。一旦LLC低端MOSFET导通，此二极管与电阻组合将为1 µF的退耦电容充电。电阻限制峰值瞬间充电电流。见图4中的R42和D8。

GND引脚

GND
GND是所有模拟弱信号的返回节点。所有弱信号引脚旁路电容必须通过短接线连接到该引脚。该引脚必须有一个单点连接，并通过专用走线连接到PFC电流检测电阻，同时该电阻又必须放置在PFC MOSFET附近。禁止将该引脚连接到PFC/LLC传动电路中的任何其他连接点。VCC旁路电容也必须连接到该引脚。

GNDP
GNDP**仅**为PFC栅极驱动信号的返回引脚。该引脚必须直接连接到PCB上的GND引脚。

GNDL
GNDL仅为LLC低压端栅极驱动器的返回引脚。必须通过一条专用走线和一个小的铁氧体磁珠将该引脚连接到LLC低压端MOSFET源极引脚。该引脚必须经由一个1 Ω电阻连接到GND引脚，这样可以预防噪音。VCCL旁路电容也必须返回到该引脚。

其他引脚

HB
半桥引脚。该引脚是LLC高压端MOSFET驱动器的返回引脚。必须将该引脚连接到由LLC MOSFET组成的半桥中心位置。VCCHB旁路电容也必须返回到该引脚。

ISP
电流检测，PFC。它用于检测电流检测电阻上的负电压（可描述PFC电感电流）。该检测电阻连接PFC MOSFET源极和桥“-”端子。信号必须穿过时间常数介于100到200 ns之间的RC低通滤波器。由于ISP引脚要求有内部偏移电流，因此电阻不得大于150 Ω。平均电感电流（经过数个开关周期测得）用于PFC控制算法。该引脚也执行逐脉冲电流限制功能。

ISL
电流检测，LLC。该引脚用于检测变压器初级电流，可检测LLC过载情况。应将它连接到LLC低压端MOSFET源极引脚和变压器初级侧低部之间所连接的电流检测电阻。信号必须穿过时间常数介于200 ns到1 µs之间的RC低通滤波器。低通滤波器中的电容必须连接到GND引脚。流限有两个级别，较低及较慢的一级是用于输出过载，较高及较快的一级用于元件故障保护。低通滤波器中的串联电阻应为1 kΩ或更大，以限制流入ISL引脚的电流。

GATEP
PFC MOSFET栅极驱动电路的栅极驱动输出信号。

GATEL
低压端LLC MOSFET的栅极驱动。

GATEH
高压端LLC MOSFET的栅极驱动。

VREF
LLC反馈电路的3.3 V参考引脚。必须连接一个1 µF的陶瓷退耦电容，且从V_{REF}引脚到GND引脚进行走线。

FBP
反馈PFC引脚连接到用于检测PFC输出电压的外部电阻分压器。这是跨导放大器的同相输入。跨导放大器输出连接到VCOMP引脚，反馈补偿也连接到该引脚。必须在FBP引脚到GND引脚之间连接一个10 µF的退耦电容。

VCOMP
该引脚是PFC反馈环路元件的连接点。引脚上的电压用作PFC控制器乘法器的输入。此引脚的额定线性电压范围为0.5 V到2.5 V，其中，电压越高，表明功率越小。

FBL

LLC反馈引脚。进入该引脚的电流可确定LLC开关频率。它有一个额定电压和电阻分别为0.65 V和3.3 kΩ的戴维南等效电路。FBL必须用一个1 µF的电容退耦到GND引脚。注意，该电容与输入电阻形成了一个点。

FMAX

该引脚通过一个电阻与VREF相连，用于设定LLC的最大频率。如果FBL引脚电流所需的频率超过最大设定频率的95%，LLC高低压两端的驱动器将会同时关断两个LLC MOSFET。该引脚必须用一个1 µF的电容退耦到GND引脚。

RSVD1, RSVD2, and RSVD3

RSVD1必须连接到VREF。RSVD2和RSVD3必须连接到GND引脚。

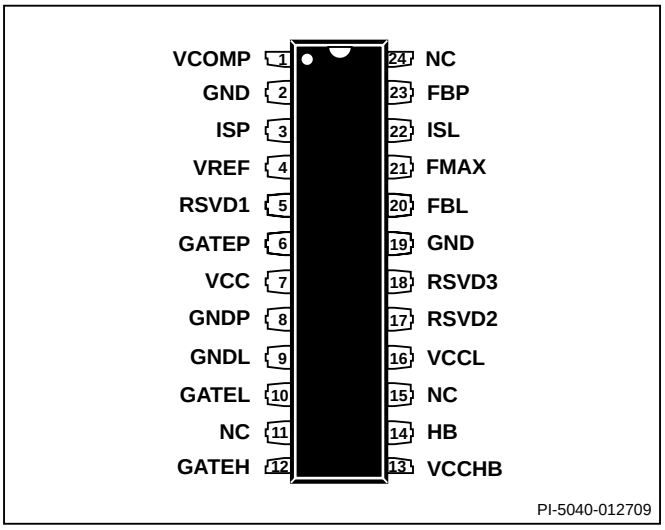


图 2. 引脚编号与名称（顶视图）

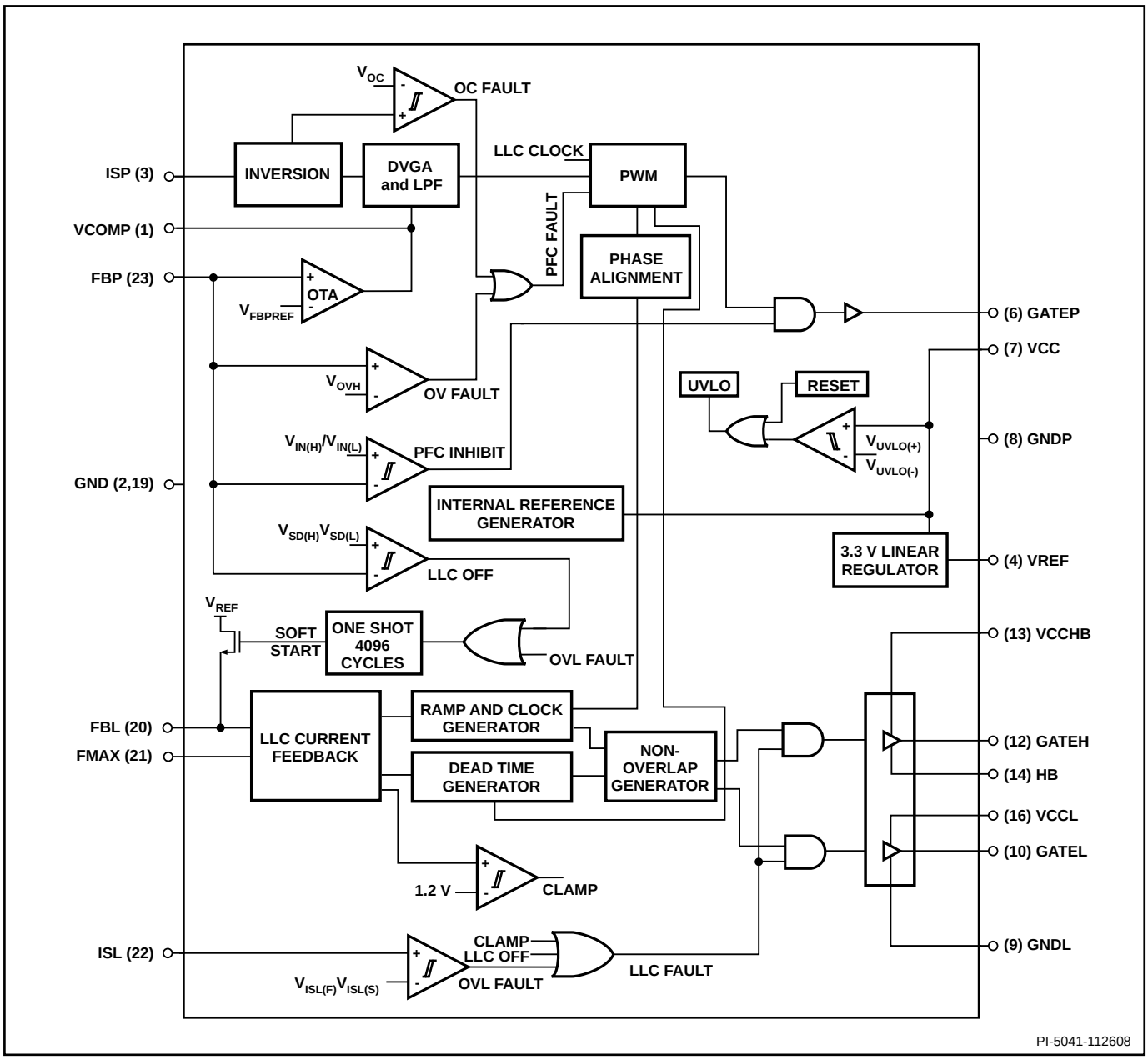


图 3. PLC810PG结构图。未显示预留的引脚

结构图

图3所示为构成PLC810PG功能的结构图。本结构图中未显示预留的引脚。预留这些引脚的目的，是供PI在生产和测试过程中使用。结构图上半部分显示的是PLC810PG PFC控制模块和电路，而下半部分则是LLC控制模块。一些功能模块是共用的。

PLC810PG电源模块

PLC810PG通过VCC和VCCL引脚供电。VCCL引脚为LLC驱动器供电，而VCC则为该器件的其他部分供电。VCC引脚供电电压必须是介于$V_{UVLO(+)}$和15 V之间的一个值。所提供的电源始终以$V_{UVLO(+)}$和$V_{UVLO(-)}$阈值为参照来启动或关断PLC810PG。当VCC超过$V_{UVLO(+)}$阈值时，PLC810PG将使欠压锁存电路(UVLO)信号失效以启动器件。如果VCC降至$V_{UVLO(-)}$以下，UVLO信号有效，这时将关断PLC810PG。

VCCL引脚为LLC驱动器供电，VCCHB为LLC高压端MOSFET的栅极驱动充电。

内部线性稳压器用于生成一个电压值为3.3V的电压总线，为PLC810PG内部的低压电路供电。该3.3 V电压引出到VREF引脚上，这样PLC810PG可为外部低压电路供电。

PLC810PG PFC控制模块

PLC810PG PFC是升压转换器，用于调节平均输入电流，使其与输入电压（通常情况下）成正弦变化并与输入电压保持同相。在正常工作条件下，PFC以连续导通模式(CCM)工作。在轻载条件下，视PFC电感值而定，转换器可能进入非连续导通模式(DCM)。PLC810PG PFC控制器无需检测输入电压。由于输入电压以60 Hz的频率变化而开关频率是它的1500倍，因此输入电压(V_{IN})在几个临近的开关周期内可视为恒定 — PLC810PG PFC控制器正是利用了这一特性。使用平均输入电压和输出电压值，可计算出升压转换器的关断时间：

$$D_{OFF} = (1 - D) = \frac{V_{IN}}{V_O}$$

输入电流与电感电流（检测的电流）相同，因此从上面的公式中可以推导出：

$$\frac{V_{IN}}{I_{IN}} = D_{OFF} \times \frac{V_O}{I_{SENSE}}$$

为了使输入电阻表现出阻性，输入电流必须与输入电压成比例：

$$\frac{V_{IN}}{I_N} = R_E$$

因此，必须通过下面的公式计算出D_{off}的值：

$$D_{OFF} = \left(\frac{R_E}{V_O}\right) \times I_{SENSE}$$

如果(D_{OFF})随着输入电压缓慢变化，平均电流将与输入电压保持同相。PLC810PG PFC模块控制PFC关断时间（D_{OFF} = (1–D)）。

由于输出电压保持恒定，R_E的值需要根据负载及输入电压的关系进行调整。

PLC810PG PFC有两个输入：

- 反馈PFC输出电压通过电阻分压并由FBP引脚进行检测。
- 瞬时电感电流通过ISP引脚进行检测。

外部电阻分压器在FBP引脚对PFC输出电压进行检测，目的是降低所需的DC升压（典型值为385 V）以便与内部生成的V_{FBPREF} (2.2 V)参考电压相符。FBP输入引脚和V_{FBPREF}电压是跨导运算放大器(OTA)的输入。OTA输出为VCOMP引脚提供驱动，可对低频电压环路进行外部补偿。

相位校准模块用于设定PFC MOSFET栅极驱动信号的边缘以避开LLC转换器开关沿。这样可消除LLC和PFC电路之间的开关噪音耦合。

补偿元件连接在VCOMP和模拟接地引脚(GND)之间。VCOMP引脚用于将补偿施加到低频电压环路。

PFC电流检测电阻生成并施加到ISP引脚的电压是以过流阈值（内置迟滞特性）为参照。这样可执行逐脉冲电流限制来防止PFC MOSFET出现过流。

ISP引脚电压还会（经过几个开关周期后）被均分，用作PFC乘法器的输入电压。

分立式可变增益放大器DVGA/LPF模块负责平均ISP引脚电压（经过几个开关周期），在VCOMP信号控制下完成PFC控制环路中乘法器的功能。

使用FBP反馈电压可提供PFC和LLC电路保护：

- **PFC过压保护**：FBP引脚上的反馈电压以过压阈值($V_{OV(H)}$)为参照。如果FBP引脚的电压超过$V_{OV(H)}$，PFC MOSFET栅极信号将立即关断且关断时间至少持续一个周期。如果FBP的电压降至$V_{OV(H)}$以下，PFC开关将重新开始导通。
- **最小升压检测**：FBP引脚上的反馈电压以最小升压阈值($V_{IN(H)}$/$V_{IN(L)}$)为参照。如果FBP电压低于$V_{IN(L)}$，PFC将被抑制。如果FBP电压超过$V_{IN(H)}$，PFC MOSFET栅极将通过GATEP来驱动。这样做可防止PFC在电压跌落期间或AC故障情况下启动。
- **LLC启动的最小升压**：FBP引脚上的反馈电压以LLC关断电压阈值($V_{SD(H)}$/ $V_{SD(L)}$)为参照。这样可抑制LLC启动，直至PFC输出电压接近稳压。$V_{SD(L)}$的用途在于当PFC输出电压降低（额定值的~64%）时关断LLC。在AC电压跌落期间、关断或过载情况下可能会出现这种情况。
- **PFC开环保护**：FBP引脚包括一个高阻抗(5 MΩ)下拉电阻，可防止开环条件引起的FBP引脚浮动。

PLC810 LLC控制模块

PLC810PG LLC控制器支持半桥拓扑结构。LLC电路依赖半桥拓扑结构中的两个开关，驱动一个谐振回路(LLC)和功率变压器。LLC电路有两个谐振频率：串联谐振频率和并联谐振频率。通常在额定电压下，LLC转换器设计的工作频率比串联谐振频率略高。在此工作阶段，MOSFET开关可以零电压运行，从而降低开关损耗。在一般工作模式下，LLC控制器的开关频率将会在较小频率范围内变化以调节输出电压。

反馈及最大频率限值

PLC810PG LLC控制器的额定工作频率为100 kHz。对于稳压，随着输入电压和负载的变化，工作频率将随之发生变化且可能会超过250 kHz。最大频率由FMAX引脚上的电阻来设定，该值通常选取为额定工作频率的两到三倍。在VREF引脚和FMAX引脚之间连接一个电阻，并利用图15中的曲线设定适当的最大频率。FMAX引脚上的电阻还设定LLC死区时间间隙（见图14）。

FBL引脚提供输出稳压。因此，进入该引脚的电流可调节开关

频率。电流越大，开关频率越高。FMAX引脚设定开关频率的上限以确保零电压开关。通过调节施加到FBL引脚上的最小偏压来确定最小开关频率。

如果外部反馈电路尝试将LLC控制器的频率提升到等于或高于由FMAX引脚设定的最大频率限值，LLC MOSFET栅极驱动输出将关断，直至流入FBL引脚的电流降低到FMAX引脚电流以下。栅极输出的关断时间与整个周期的时钟同步。

LLC软启动

LLC控制器执行软启动以防止启动期间的过量电流以及反馈环路工作时的输出电压过冲。软启动时间由FBL引脚上的外部元件确定。如果LLC电路因LLC失效而关断，则允许外部电路放电，从而开始新的软启动。如果软启动信号有效，FBL引脚的电压将被上拉至V_{REF} (3.3 V)，保持将最大的电流施加到FBL引脚上。在软启动周期，LLC输出导通，开关频率逐渐从最大值衰减到额定工作点。

LLC过流检测（ISL引脚）

LLC转换器中的过流通过与变压器初级绕组低端串联的检测电阻进行检测。如果检测到过流情况，LLC MOSFETS将关断。过流检测有两个阈值：快速过流阈值($V_{ISL(F)}$)和慢速过流阈值($V_{ISL(S)}$)。快速过流阈值通常由非正常的高电流所触发。如果ISL引脚上的脉冲超过该阈值，LLC将立即关断。慢速过流阈值要低于快速过流阈值。如果ISL引脚电压超过该阈值的时间达到八个连续脉冲周期，将触发慢速过流响应并使LLC关断。

通常情况下，($V_{ISL(F)}$)阈值用于检测严重故障，如元件短路，而慢速$V_{ISL(S)}$阈值则用于检测过载情况。该过流检测电路可防止LLC转换器在LLC的容性区域工作，从而避免转换器元件因过热而产生故障。

其他LLC控制模块

不重叠（死区时间）生成器可生成两个导通时间相同但不同时导通的信号来驱动LLC MOSFET。两个LLC MOSFET驱动信号的占空比相同，各占一半。PFC和LLC共用的死区时间模块作用在于控制开关功能的死区时间。PLC810PG中的死区时间可通过FMAX引脚配置。死区时间允许零电压开关，这样可减少体二极管在开关MOSFET中的损耗，并缩短体二极管的反向恢复时间。

启动

一旦VCC电压达到启动电压($V_{UVLO(+)}$)，PLC810PG即开始开关PFC MOSFET，且PFC输出呈斜坡式上升到额定值。当PFC升压（通过FBP引脚检测）使FBP引脚电压上升到超过LLC启动阈值($V_{SD(H)}$)时，LLC电路将使能且开始LLC软启动。

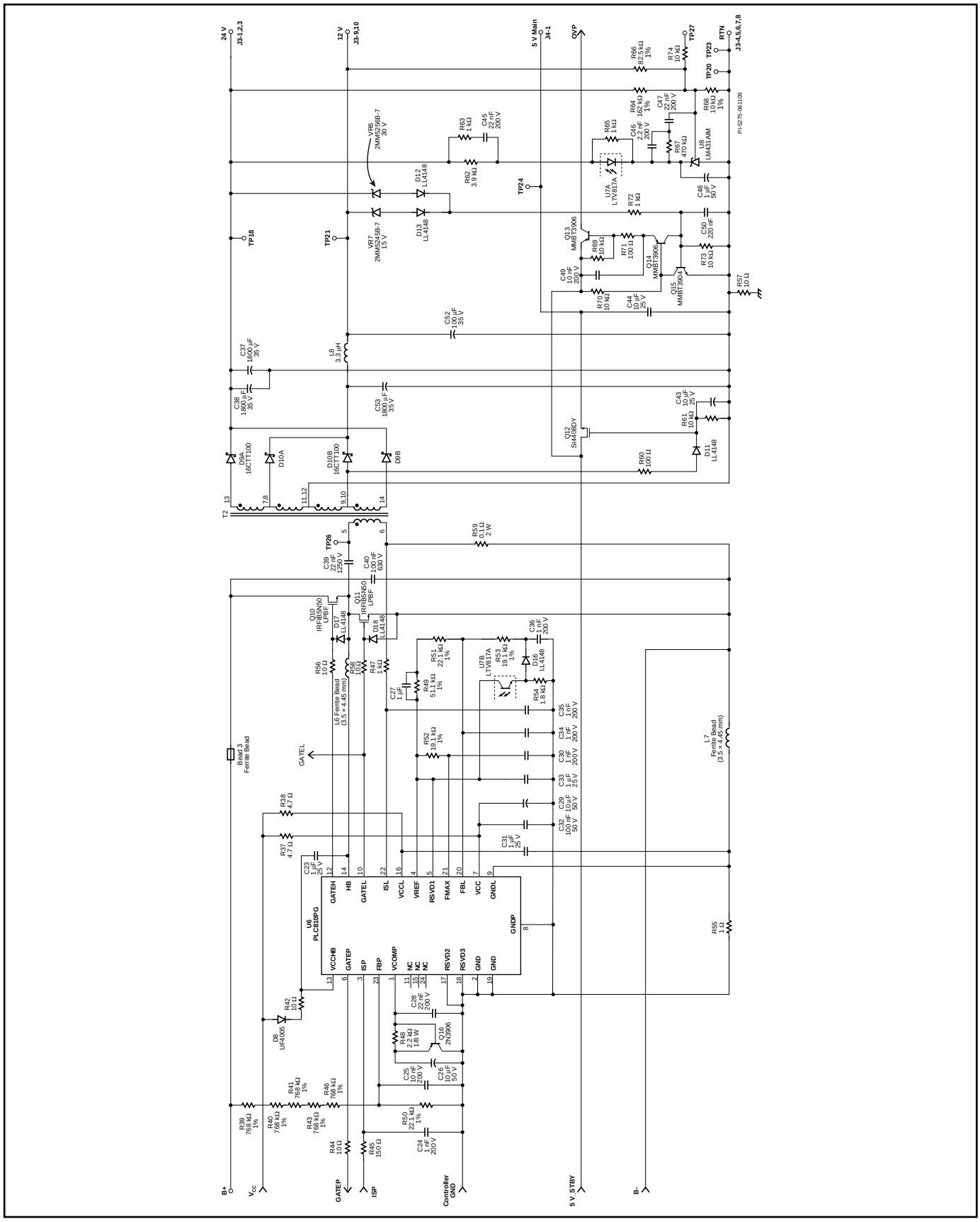


图 4. PLC810PG LCD电视机电源应用电路，PFC电路控制输入和LLC级

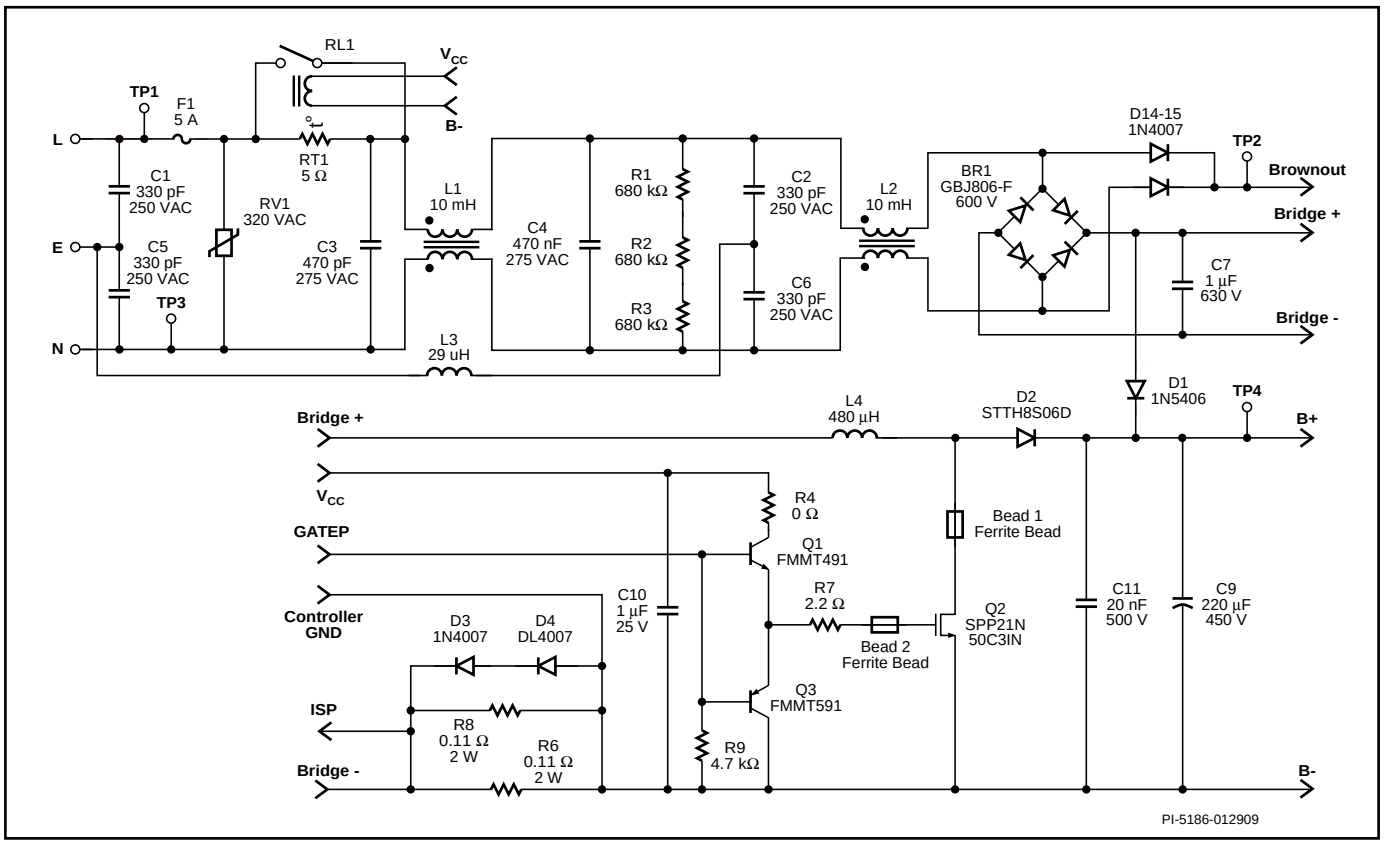


图 5. PLC810PG LCD电视机电源应用电路，输入电路和PFC功率级

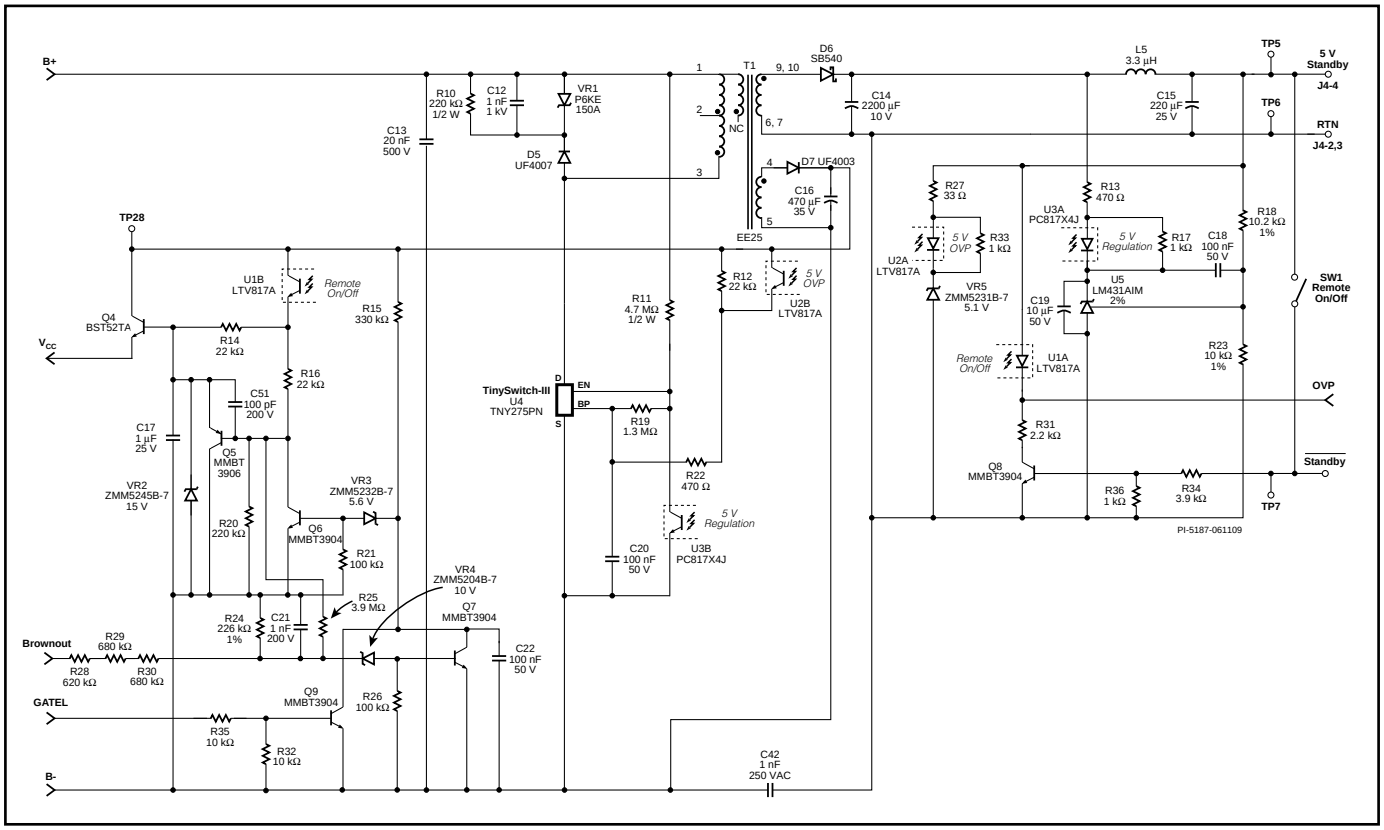


图 6. PLC810PG LCD电视机电源应用，待机电源

应用范例

电路描述

图4、5和6所示为典型的280 W LCD电视机电源应用的电路图，设计中采用了HiperPLC和TinySwitch-III器件。PSU中包含使用PLC810PG来提供高功率输出的PFC + LLC级，以及使用TNY275PN的待机电源。

该设计有四个输出：12 V和24 V；5 V主输出和5 V待机输出。5 V主输出和5 V待机输出由TinySwitch-III反激式电路提供。Power Integrations网站上提供了有关TinySwitch-III反激式转换器的说明，详见网站上TinySwitch-III数据手册中的“典型应用”部分。

PSU有一个待机输入信号，用于启动主转换器(PLC810PG)。

EMI滤波和整流

电容C42、C1、C5、C3、C4、C2和C6以及共模扼流圈L1和L2执行EMI滤波。桥式二极管BR1对输入AC进行整流，D14和D15为电压跌落电路提供单独的全波整流信号。

浪涌限制

热敏电阻RT1用于限制浪涌。它与由电源遥控导通信号驱动的继电器(RL1)进行跨接。使用继电器可将效率提高大约1%。二极管D3给浪涌电流提供一个到C9的旁路通路，使其不经过PFC电感L4，避免电感饱和。

PFC级

主PFC电感L4、MOSFET Q2、升压二极管D2以及大容量电容C9共同形成一个PFC升压转换器。电容C8和R5可衰减D2上的反向恢复振荡。电感L4使用低成本的铁硅铝磁芯。此连续模式PFC设计的两大优势在于低纹波电流允许使用：

1. 高B_{SAT}材料（如低成本的铁硅铝），这样可减少匝数，节约铜片成本和减小变压器尺寸。
2. 低成本的漆包线，而无需使用利兹线。

二极管D2是低成本的硅超快PFC升压二极管。

元件Q1、Q3、C10和R7形成栅极驱动电路。请参见“建议的PFC栅极驱动电路”下的说明。

D3和D4对PFC电流检测电阻R6和R8进行箝位，在浪涌期间为控制器IC提供电流检测输入保护。电容C11放置在PFC MOSFET和二极管附近，这样可限制元件Q2、D2和C9周围高频环路的大小，从而降低EMI。低损耗薄膜电容C7用作PFC升压转换器的输入电容，也可对EMI进行滤波。

LLC级

LLC输入级

MOSFET Q10和Q11形成LLC半桥。它们由PLC810通过栅极电阻R56和R58直接驱动。电容C39是初级谐振电容，因此应为低损耗型电容，在出现最大负载时其额定值容许最高RMS电流。变压器T2有一个内在的大容量漏感，与C39共同作用，形成串联谐振回路。电容C40用于局部旁通，与Q10和Q11相邻。电阻R59检测控制器的初级电流以提供过载保护。

LLC输出

变压器二级输出T2由D9、D10、C38、C39和C53整流和滤波，实现+12和+24 V输出。

开关控制的+5 V主输出

MOSFET Q12用于开关+5 V逻辑电源的输出。来自12 V输出整流管一侧的AC信号经由R60、R61、D11和C43为Q12提供驱动。电容C44在靠近输出连接端提供滤波。

偏置稳压器/远程导通（关断）和电压跌落关断电路

元件Q4、U1、C17和相关元件形成偏置稳压器，提供远程导通/关断功能。达林顿晶体管Q4、R14和VR2形成一个简单的射极跟随器稳压器，经由光耦器U1开关。电容C17限制偏置电压的上升率。当光耦器U1关断时，晶体管Q5和R20迅速使C17放电。

在次级侧，当待机信号为高电平时，光耦器U1通过Q8导通，从而导通PFC LLC级。

在输出因电压跌落而关断时，电压跌落关断电路将主动关断PSU。

该电路通过检测AC输入电压和LLC控制器的GATEL信号来工作。在电压跌落期间，PFC输出电压将下降，直至VFB引脚电压下降至INH（此时关断LLC级）。如果此时AC电压低于82 VAC，电压跌落电路将通过偏置稳压器关断PLC810，从而防止PFC再次对大容量电容充电、重启动LLC并重复周期（以及产生输出电压不良波动）。

电阻R24、R26、R28-30、C21、VR4和Q7用于检测AC输入电压。该电路的电压阈值设定为低于待机/初级偏置转换器的导通阈值。AC电压充足时，将导通Q7，此时电容C22放电（它通过R15充电）。元件R32、R35和Q9检测开关GATEL信号。检测到开关信号时，晶体管Q9将为电容C22放电。

如果AC输入电压较低，Q7和Q9将关断，此时C22放电。晶体管Q6、R21和VR3检测C22上的电压。当C22充满电时，Q6导通，随之将经由Q5关断初级偏置电源，依次关断PLC810以及PFC和LLC级。

控制器

图4所示为U13主控制器IC周围的电路，为输入PFC和输出LLC级提供了控制功能。

PFC控制

PFC升压级输出电压经由R39-41、R43、R46和R50反馈到PLC810PG的FBP引脚。一个10 nF的电容(C25)用于滤波噪音。电容C26、C28和R48为PFC提供频率补偿。R45和C24对来自电阻R6和R8的PFC电流检测信号滤波。PFC驱动信号经由电阻R44送到主开关MOSFET，这样可抑制PFC驱动信号中由PLC810PG和PFC栅极驱动电路之间的走线长度而引起的振荡。

旁路/接地隔离

请参见“针脚说明”部分下的“GND引脚”和“VCC引脚”。电容C29和C32为VCC引脚退耦。电容C31为VCCL引脚退耦。R37为可选电阻，为VCC引脚提供额外滤波。这样有助于抑制待机电源长的Vcc走线所产生的任何噪音。

电容C24、C25、C32、C29、C30、C31、C33、C34和C35必须连接正确的接地引脚，且必须使用较短的接线将它们连接到PLC810PG。请参见“引脚说明”部分。

电阻R55将GND与GNDL引脚隔开。R55与铁氧体磁珠L7配合工作，在GND和GNDL引脚之间形成高频隔离。低压端LLC MOSFET Q11的GATEL输出栅极驱动通过铁氧体磁珠L7返回到GNDL。高压端LLC MOSFET Q10的GATEH输出栅极驱动通过铁氧体磁珠L6返回到HB。该磁珠为可选元件，但可与L7形成对称。

LLC控制

来自LLC输出检测/误差放大器电路的反馈由光耦器U7提供。电阻R54是光耦器负载。二极管D16允许光耦器仅上拉LLC反馈引脚(FBL)。请参见“LLC控制器”部分中有关R54、C36、R53、R51、R49和C27所执行功能的说明。R47和C35对来自电阻R59的LLC电流检测信号滤波。电容C23、R42和D8为LLC高压端MOSFET驱动器提供自举电源。请参见“引脚说明”部分下的“GND引脚”和“VCC引脚”。

LLC次级控制电路

图4所示为LLC级的次级控制电路图。

电压反馈

LLC转换器的12 V和24 V输出通过电阻R64、R66和R68进行检测、加权和求和。电阻R62为主增益设定电阻。电阻R63和C45形成相位超前补偿器，可扩展反馈环路的交越频率和增加相位裕量。电阻R67、C46、C47和R68共同设定低频补偿。电容C48是一种“软结束”电容，在输出电压上升时导通，减少启动时的输出过冲。它不会影响主反馈环路的特性。

OVP

齐纳稳压管VR6-7、D12和D13检测12 V或24 V输出的任何过压情况。来自12 V或24 V输出的过压信号用于触发双极性晶体管组成的锁存电路（Q14、Q15、R70和R73），这将导通晶体管Q13。该晶体管用于使远程导通电路失效，这样可关断初级偏置电源并进而关断PLC810PG。

电源模块功能和关键设计细节

PFC控制段

PFC控制器使用的是运关断占空比控制算法的连续导通模式。该方法无需对输入AC电压进行检测。关断时间与平均电感电流（若干开关周期的平均值）和误差放大器输出电压的乘积成比例。这将自动形成平均输入电流，与输入AC电压的形成方式相同。

PLC810PG的PFC电路频率和相位锁定到LLC电路。PLC810PG采用冲突避免技术，将PFC的边缘跨骑在LLC的边缘，以防止PFC和LLC段的边缘同时发生转换。这样可降低PFC和LLC电路之间的干扰。

PFC部分有两个输入引脚：电流检测引脚（ISP引脚）和电压反馈输入（FBP引脚）。有两个输出引脚。VCOMP引脚用于放置反馈补偿元件，MOSFET栅极信号输出专用于与外部MOSFET驱动器配合工作。

电感电流通过ISP引脚来检测，ISP引脚可以监测PFC电流检测电阻上产生的负电压。该电阻连接PFC MOSFET源极。电流经过若干开关周期后被均分并用于PFC控制算法。该引脚还执行逐脉冲电流限制来防止PFC MOSFET出现短路。时间常数为100-200 ns的RC滤波器可消弱高频开关噪音，但其检测饱和PFC电容的速度必须足够快才能为PFC MOSFET提供保护。

PFC输出电压通过一个电阻分压网络由FBP引脚检测。FBP引脚与跨导运算放大器(OTA)的输入端相连。该OTA的输出连接到VCOMP引脚。反馈环路可将FBP引脚的电压（以及相关的PFC输出电压）保持在一个固定值，具体情况视电阻分压比而定。当PFC输出电压超过设定点时，跨导放大器将输出电流，使VCOMP引脚的电压上升。当PFC输出电压低于设定点时，跨导放大器将吸入电流，使VCOMP引脚的电压下降。该级的增益等于OTA增益(G_M)与VCOMP引脚上连接的网络电阻的乘积。

PFC控制器检测VCOMP引脚上的电压。高电压可以降低PFC MOSFET的占空比，而低电压则可增加占空比。

VCOMP引脚有一个0.5 V到2.5 V的线性工作范围，比例分压后与平均电感电流相乘可以得出D_{OFF}值，即PFC栅极信号断开占空

比。在闭环稳定工作期间，VCOMP电压是线电压和PFC负载的函数。VCOMP电压低，表明功率高，同理，电压高，功率就低。

VCOMP引脚从内部连接到一个乘法器的输入。乘法器是PFC调制器的一个部分。该引脚的线性电压范围为0.5 V到2.5 V。0.5 V表示最高功率，2.5 V表示最低功率。

FBP引脚有3个启动和关断电压阈值。

1. INH – 禁止PFC在低AC输入电压下启动。
2. $V_{SD(H)}$ – 禁止LLC在PFC启动后启动。LLC启动将会延迟，直至PFC输出电压接近稳压设定点。
3. $V_{SD(L)}$ – 在大容量电容放电至低压时关断LLC转换器 – 通常出现在保持时间结束时。

在PFC启动前，大容量电容上的电压近似等于输入电压的峰值，并且INH将充当AC欠压锁存功能。PFC启动后，PFC输出电压不再跟踪输入电压，此时AC低压关断功能不存在。

在PFC电压设定点为385 V的典型设计中，当高电压<100 V（典型值）时，PFC被抑制。该值相当于VAC <71 V（典型值）。LLC启动将会被抑制，直至PFC输出电压达到368 V（典型值）。对于相同设计，LLC在PFC输出电压下降到246 V（典型值）以下时将关断。

LLC控制器段

LLC转换器是一种变频转换器（LLC转换器的输出随着频率的增加而降低）。设计师需要设定PLC810PG的最小及最大频率，以便满足传动电路的需求。

FMAX引脚

FMAX引脚通过设定的电阻连接到VREF引脚。该电阻设定进入FMAX引脚的电流。该引脚有一个额定电压和电阻分别为0.65 V和1.5 kΩ的戴维南等效电路。设定进入FMAX引脚的电流控制以下两个参数：

1. LLC栅极（GATEL和GATEH）死区时间。电阻值越小，电流就越大，最大频率也更高，参见图15。
2. 最大LLC工作频率。当FBL引脚电流增加到超过FMAX引脚电流时，LLC MOSFET将关断。当FBL引脚电流下降到低于FMAX引脚电流时，开关将重启动。

死区时间应大于LLC半桥中心点（最小负载下的最长时间）的实际电压上升和下降时间。如果设定的死区时间少于实际上升和下降的时间，MOSFET将停止在ZVS阶段工作且损耗将会增加。死区时间略高于所需的最小时间对效率几乎没有任何影响。

死区时间较长时，LLC开关MOSFET的体二极管将在导通之前的一瞬间传导电流，与其他损耗相比，额外的传导损耗非常小。FMAX引脚设定电阻设置死区时间和最大频率。如果需要较低的最大频率，建议将死区时间设置为大于空载时所需的时间。

如果所需的死区时间非常长，且得出的F_{MAX}低于空载稳压（最大输入电压时出现的最差情况）所需的值，那么要保持输出稳压，解决方法是限制F_{MAX}并允许LLC在轻载（最大频率）时进入突发模式。在100-0%负载阶段将出现最大输入电压，这将导致PFC输出电压过冲到VOV(H)，触发PFC输出过压保护电路（一般为PFC额定电压设定点的105%）。对于典型设计，LLC转换器所需的F_{MAX}为额定工作频率的1.5 ~ 2倍（满载和额定输入电压下测得）。

如果在轻载条件下需要突发模式稳压，则必须选择FBL引脚电阻且需满足以下条件：由反馈环路驱动的流入FBL引脚的最大电流大于FMAX引脚电流（由FMAX引脚电阻设定）。当FBL引脚电流大于FMAX引脚电流时，LLC栅极驱动器将同时关断两侧的MOSFET。在输入电压/负载突变条件下（要求频率高于F_{MAX}以保持稳压），LLC转换器将进入迟滞突发模式以保持稳压。

如果使用突发模式，请务必小心，确保启动时峰值初级电流不会触发初级过流（ISL引脚）。这是由于开关频率不可超过F_{MAX}（即使在软启动期间也是如此），具有低软启动频率的峰值初级电流因此将更高。

FBL引脚

FBL引脚是稳压反馈引脚。它可在正常工作条件下吸收电流。输入电流越大，LLC开关频率越高。频率特性与分流电阻（连接到VREF）大小之间的比例关系见图16。FBL引脚有一个额定电压和电阻分别为0.65 V和3.3 kΩ的戴维南等效电路。应当注意的是，1 nF退耦电容C_{FBL}（见图7）与FBL引脚上产生的3.5 kΩ输入阻抗结合在一起形成LLC传递函数的一个极点。应将它视为LLC反馈环路的组成部分。为确保环路的稳定性，不应增大1 nF电容。

典型的反馈电路使用TL431和一个光耦器进行输出稳压。光耦器调节流入FBL引脚的电流。光耦器和FBL引脚之间的电阻网络设定流入FBL引脚的最小电流、最大电流以及启动电流。
在图7中，光耦器U1 B通过电阻R1、R2、R3、R4和电容C_{START}组成的电阻网络连接到FBL引脚。C_{START}仅在软启动期间有作用，在一般工作状态下可以忽略它。Copto是一种滤波电容，可以降低光耦器长走线产生的噪音。(R3 + R4)的值可设定FBL引脚最小电流并随之设定LLC的最小频率F_{MIN}（在光耦器关断的情况下）。这出现在持续时间末期，这时大容量电容已放电到稳

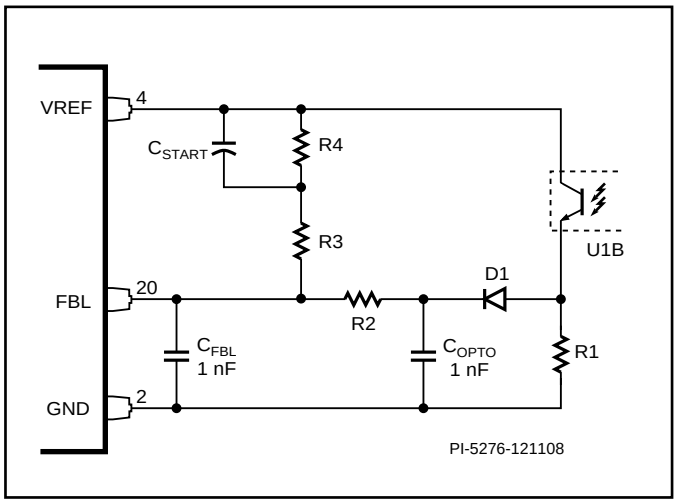


图7. 典型的*LLC*反馈电路

压设定点的64%（标称值）。

FBL引脚的最大电流（以及反馈环路由此可控制的LLC最大频率）由R2、R3及R4设定。当光耦器完全饱和时将出现最大频率，如一个输出负载突降期间LLC输出将超过设定点一样。应注意的是，如果FBL引脚的最大电流大于F_{MAX}引脚电流，LLC栅极驱动器将同时关断两侧的MOSFET。

R3的值决定启动电流（以及与此相关的启动频率）。请注意，在启动期间，C_{START}是一个短路，光耦器将关断，FBL引脚的所有电流均来自R3。

选择电阻值的步骤如下。

选择R1

R1是与光耦器串联的主要负载电阻。选取1.8 kΩ的电阻值将获得较佳的频率响应，并可获得约为2 mA的可接受的集电极最大负载电流。请注意，整个环路增益将与该电阻值成比例。

选择F_{START}（启动时的初始频率）

F_{START}通常取值等于或小于F_{MAX}。根据图16确定与所需的F_{START}值对应的电阻值。将R3设定为此值。R3的值通常会与F_{MAX}电阻的值相近。

下一步是设定F_{MIN}。F_{MIN}是LLC在满载条件下进行调整时所需的频率，F_{MIN}的大小由R3和R4的总和(R3 + R4)决定。在图16中查找所需的F_{MIN}值对应的电阻值R。根据下面的公式设定R4的值。

$$R4 = R - R3$$

计算R2的值

$I_{FBL(MAX)}$是在光耦器饱和时流入FBL引脚的电流。它代表反馈环路可通过FBL引脚进行控制的最大频率。如果该电流大于F_{MAX}引脚电流（由F_{MAX}引脚电阻设定），LLC转换器将被迫进入迟滞突发模式，以便调整零负载或轻载下的输出电压。如果不需要突发模式，$I_{FBL(max)}$必须设定为小于F_{MAX}引脚电流。此时，应确保F_{MAX}引脚电阻提供充足的死区时间。如果F_{MAX}小于轻载条件下进行调整所需的频率，则必须采用突发模式工作。

从图17中可以看出I_{FBL}（FBL引脚电流）与频率之间的关系。$I_{FBL(max)}$与电阻值之间的关系由下面的公式来表示(1)：

$$I_{FBL(MAX)} = \frac{V_{REF} - V_{FBL}(I_{FBL(MAX)})}{R3 + R4} + \frac{V_{REF} - V_{CESAT} - V_{FBL}(I_{FBL(MAX)}) - V_D}{R2} \quad (1)$$

V_{R2}（R2上的电压）可以定义为：

$$V_{R2} = V_{REF} - V_{CESAT} - V_{FBL}(I_{FBL(MAX)}) - V_D \quad (2)$$

我们然后将(2)代入(1)，重新调整得出以下公式：

$$R2 = V_{R2} \frac{R3 + R4}{I_{FBL(MAX)}R3 + I_{FBL(MAX)}R4 - V_{REF} + V_{FBL}]I_{FBL(MAX)}g} \quad (3)$$

其中，V_{FBL}是I_{FBL}的函数

V_{CESAT} = 光耦器在饱和状态下的V_{CE}（典型值为0.3 V）

V_D = 二极管正向电压降

V_{REF} = 3.25 V（额定）

LLC软启动

LLC软启动由C_{START}（见图7）执行。LLC以高频启动，然后斜降直至达到输出稳压。软启动是必需的，因为这样可以使谐振回路开始振荡。软启动还可防止启动时产生大LLC初级电流，以免超过ISL引脚上的过流阈值。

PLC810PG启动后，FBL引脚内部拉升至VREF (3.25 V)，LLC输出被禁止。这样可确保对软启动电容C_{START}进行放电。然后释放FBL引脚电压降至约0.8 V；PLC810PG开始检测流入FBL引脚的电流，LLC栅极驱动输出开始开关。启动时，光耦器内将没有电流流动（因为LLC转换器输出较低），FBL引脚电流将等于$I_{FBLSTART}$。当C_{START}充电时，流入FBL引脚的电流开始减小，LLC开关频率降低，LLC转换器输出升高。达到稳压后，反馈环路闭合，光耦器对FBL电流进行调节。正常工作时，C_{START}保持被充电状态，不会有任何电流。

启动时间常数的计算公式如下：

$$\tau_{START} = C_{START} \times \frac{R3 \times R4}{R3 + R4}$$

LLC保护及自动重启动

LLC引脚通过与变压器初级绕组低端串联的检测电阻来检测LLC初级电流。需要使用一个RC低通滤波器，建议的值分别是1 kΩ和1 nF。ISL引脚有两个阈值。较高的阈值为$V_{ISL(F)}$，可使引脚在发生元件故障时立即关断并对LLC MOSFET提供保护。较低的阈值为$V_{ISL(S)}$，如果超过8个连续周期，引脚也会关断LLC，以免发生输出过流。其中任何一个故障模式都会启动和重启动序列。发生任何一种故障时，FBL引脚会内部拉升至VREF，对软启动电容进行放电。控制器会计数4096个时钟周期，然后开始新的启动（软启动）序列。通常4096个周期足以完全对软启动电容进行放电，确保LLC将以F_{START}的频率重启动。

布局注意事项

PFC功率部分布局

PFC布局

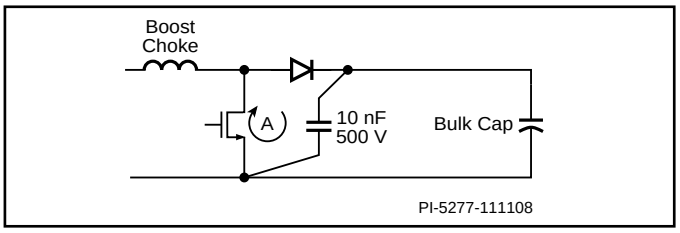


图 8. 升压转换器级中的功率元件

图8所示为使用单个大容量电容设计的典型PFC升压转换器（有些设计可能出于纹波电流要求而使用两个大容量电容）。

使用单个大容量电容时，该大容量电容距PFC MOSFET的位置应比LLC MOSFET更近。PFC MOSFET、二极管和大容量电容应彼此靠近放置，并用短引线连接它们。此外，建议使用10 nF-47 nF高频旁路电容来降低EMI。该电容还应连接在PFC MOSFET和二极管附近，以便减小环路面积（电路图中的“A”）。由于该环路面积可能会造成di/dt值达到最高，因此必须使其减小。在有些情况下，可选阻尼电阻与10 nF电容串联能够降低开通时漏极电流振荡和随之产生的EMI。该电阻的建议值应介于0.2 Ω和1 Ω之间。

LLC功率部分布局

大容量电容的放置

如果使用两个并联的大容量电容来满足纹波电流要求，那么第一个电容应靠近PFC MOSFET放置，第二个电容应靠近LLC MOSFET放置。如果只使用一个大容量电容，建议高压退耦电容(10 nF-100 nF)跨HVDC总线和初级返回端进行连接，并通过短连接与LLC MOSFET相连。（请参见图4所示电路图中的C40以及图9中的PCB布局）。LLC转换器MOSFET具有高di/dt值，这种高压退耦电容将降低EMI。

高压引脚

器件上的三个引脚具有高的电压和高的dv/dt，原因是它们可跟踪LLC MOSFET的半桥输出。这些引脚分别是HB、VCCHB和GATEH（引脚12、13和14）。这些引脚必须与PLC810PG上的其他引脚隔离（通过省去引脚11和15还可提供额外的封装隔离）。由于这些引脚的dv/dt值较高，因此与其相连的走线和元件必须与低压引脚隔离开。这些节点与低压节点之间存在杂散电容，所以（高阻抗）引脚将造成噪音耦合和工作不稳定。应在这些引脚之间保持160 mil (4 mm)的间距，并围绕低压节点放置。请参见图10中突出显示的间距。

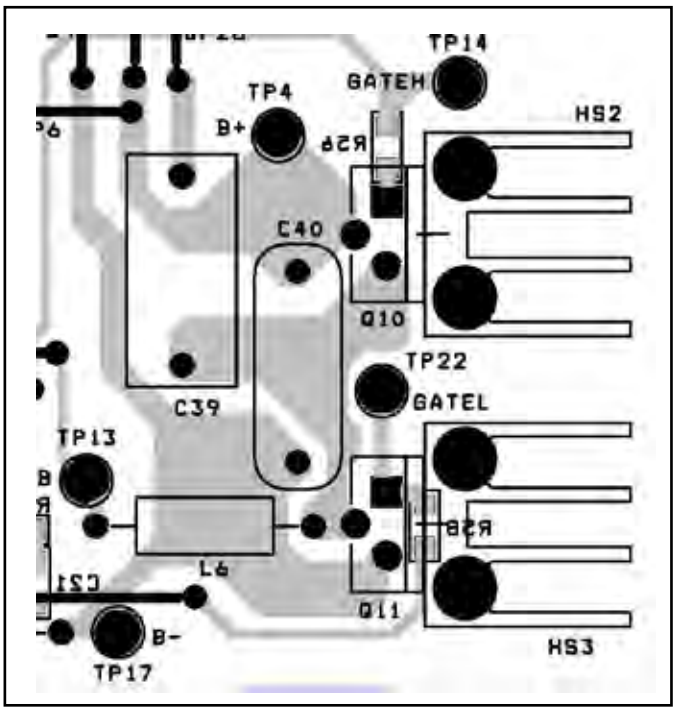


图 9. LLC高压薄膜退耦电容C40的位置

低压信号引脚

所有引脚退耦电容都必须靠近IC放置，并以短连接方式与引脚相连。所有退耦电容均应返回到GND引脚，但VCCL和VCCHB的退耦电容除外。

有多个引脚要求使用外部RC低通滤波器。它们分别是ISP、ISL、FBP和FBL引脚。电容和电阻应靠近IC放置。这样可以防止与dv/dt节点发生电容耦合。ISP引脚是信号最小和带宽最宽的输入引脚。它不仅可以检测PFC扼流圈中的平均电流，还可以检测峰值电流，以执行峰峰值电流限流（从而保护PFC MOSFET）。电流限流功能要求具有宽的带宽。

使用时间常数介于100 ns和200 ns之间的RC低通滤波器，将其放置在器件附近。低通滤波器中的电容应返回到GND引脚。将PFC检测电阻靠近PFC MOSFET放置。

从GND引脚到PFC MOSFET源极引脚与PFC检测电阻的结点进行专门走线。在GND引脚到PFC/LLC功率元件之间的走线上不应该有任何其他连接。

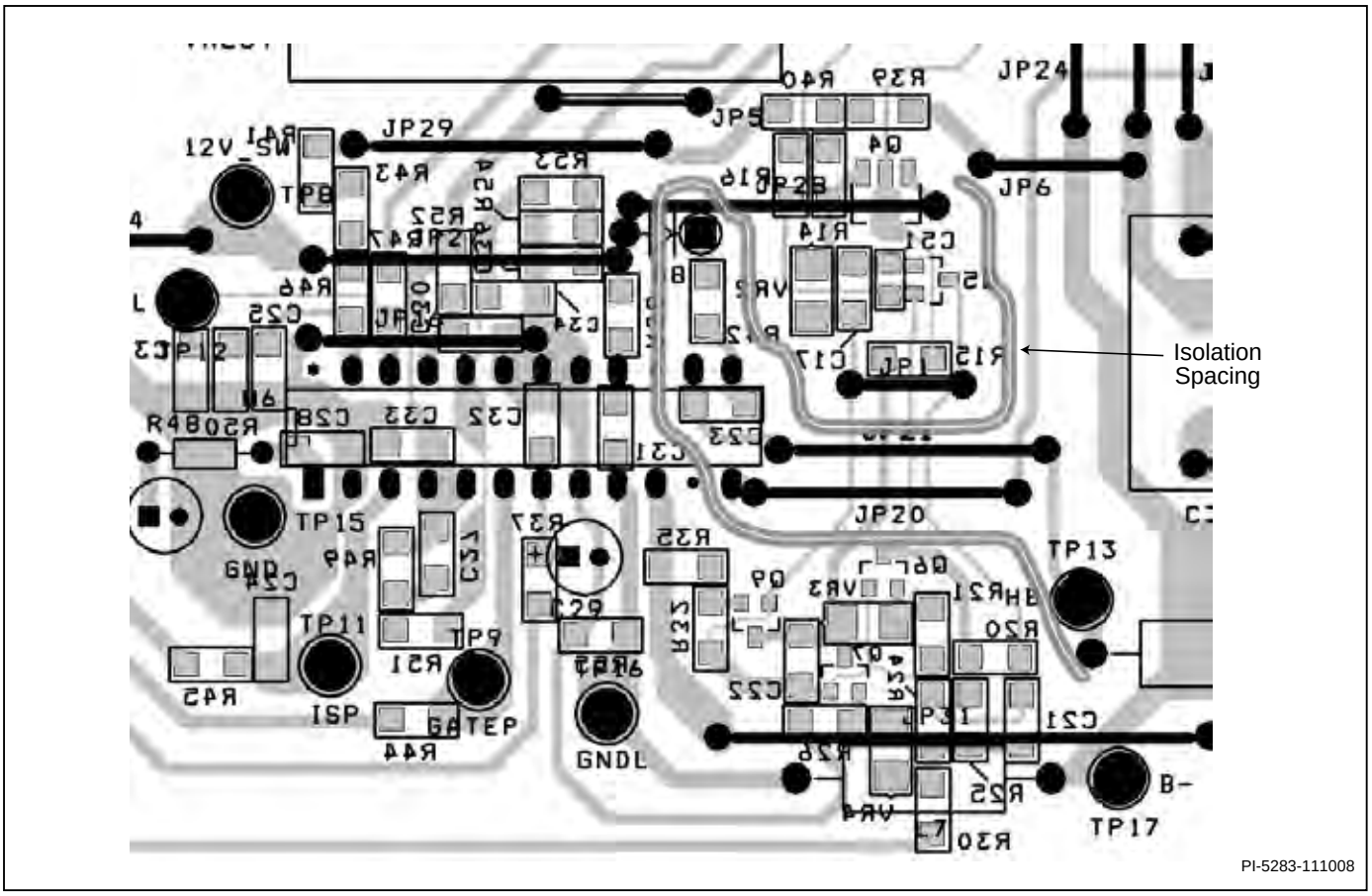


图 10. 高dv/dt引脚与低压引脚和走线的隔离设计

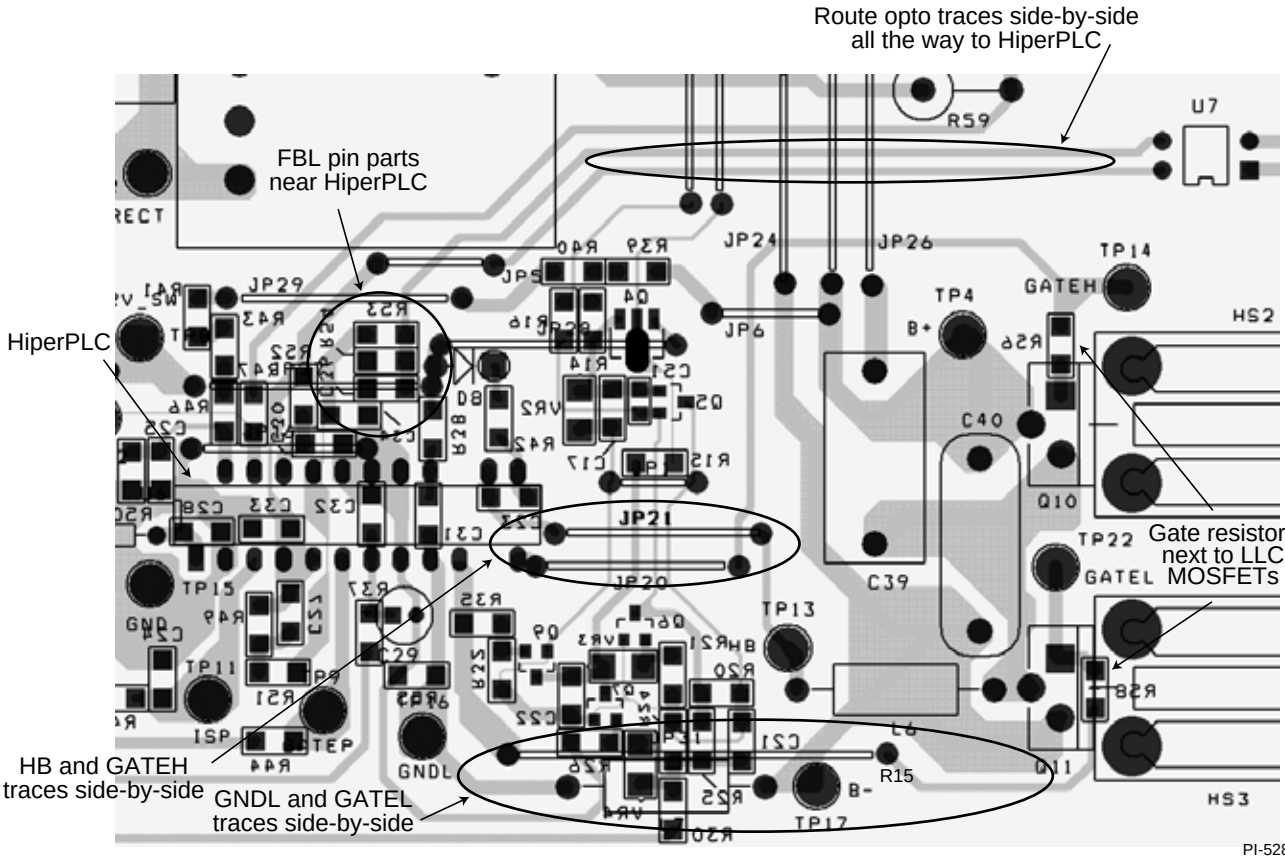


图 11. 栅极驱动和反馈PCB布局设计建议

从ISP引脚上RC低通滤波器的电阻到PFC检测电阻进行专门走线。为避免di/dt噪音对环路的干扰（这可能影响信号的完整性），这条走线必须沿从GND引脚到PFC MOSFET源极引脚的走线进行设计。

将PFC驱动电路靠近PFC MOSFET放置。进行连接GATEP和PFC驱动电路的走线，使其靠近连接到检测电阻的ISP走线。最好使GND走线介于GATEP走线与ISP信号走线之间。这样将降低GATEP走线与ISP走线之间潜在的噪音耦合。请参见图12。

FBL引脚电路和光耦器

请参见图13。FBL引脚电路应靠近PLC810PG放置。反馈光耦器通常远离IC放置。从光耦器（发射极和集电极）引出的两条走线应并行走到FBL电路。这样可缩小环路面积和限制杂散的di/dt（电感性）噪音耦合。

GATEL和GNDL

请参见图11。从GATEL引脚引出的线路与从GNDL引脚引出的线路（分别连接到LLC低端MOSFET栅极和源极）应当并行走线。

GNDL引脚应通过铁氧体磁珠连接到LLC低端MOSFET源极引脚。栅极电阻(R28)也应当靠近MOSFET放置。

HB和GATEH

请参见图11。HB和GATEH线路应从LLC高端MOSFET到PLC810PG并行走线。栅极电阻(R26)应靠近MOSFET放置。

建议的PFC栅极驱动电路

图13所示为建议的PFC　MOSFET栅极驱动电路。该电路需要靠近PFC MOSFET放置。栅极关断电流由R33进行控制，而栅极导通电流则由R33和R4值的总和来控制。电阻R4还可以防止开关沿时高直通电流流过两个BJT。电阻R4与Q8集电极而不是发射极串联放置，因为这样将防止Q8中出现负的Vbe电压，由此导致结被击穿。电阻R3和R4对PFC效率和EMI有很强的影响。局部1µF旁路电容C28需要靠近BJT（Q8和Q9）放置。电阻R107用于在PLC810PG断电后使MOSFET保持关断。

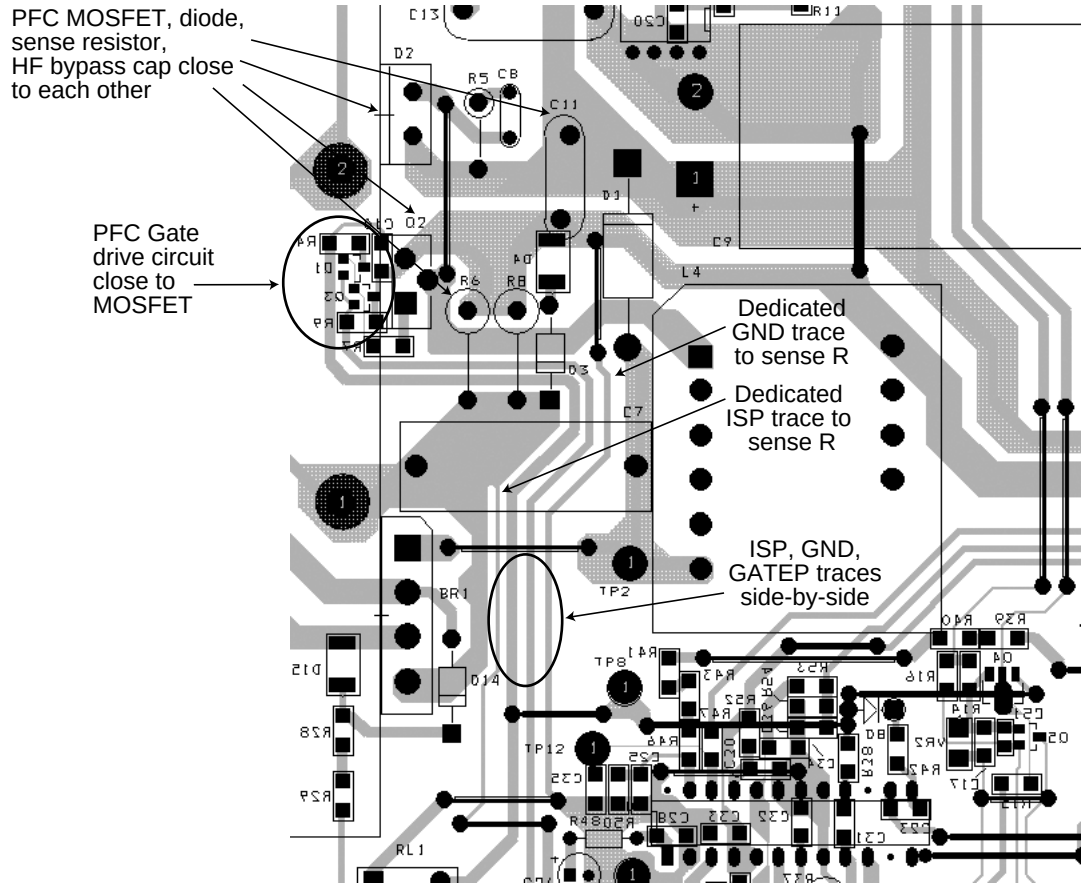


图 12. PFC功率和信号布局设计建议

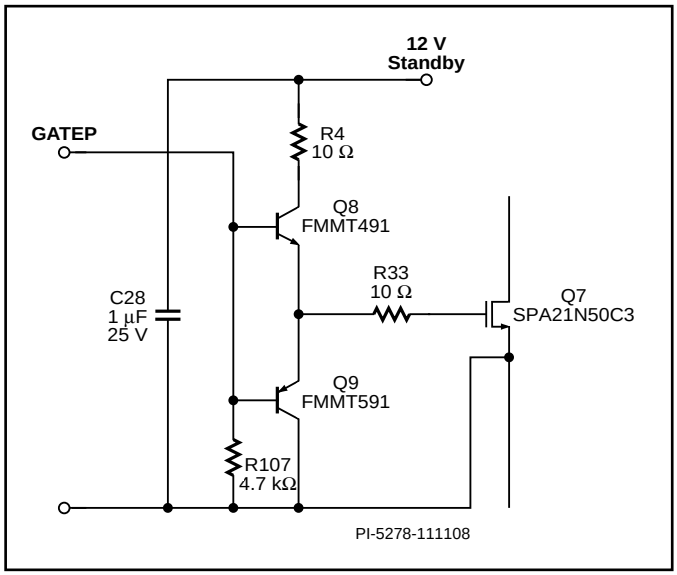


图 13 PFC栅极驱动电路设计建议

绝对最大额定值

表1列出了绝对最大额定值。超过这些限值的应力可能会造成PLC810PG的永久性损坏。长时间使用高于器件建议的工作限值时，会对产品的性能和可靠性造成影响。建议了解常见的ESD处理注意事项。

绝对最大额定值	
结温度	-40 °C到+125 °C
贮存温度	-65 °C到+150 °C
$Theta_{JA}$	35 °C/W
连续电源电压(VCC, VCCL)	-0.3 V到15 V
LLC电压（HB引脚）	-0.3 V到600 V
LLC高压端浮动电源电压（VCCHB引脚相对于HB引脚）	-0.3 V到V_{CCL}
LLC高压端浮动输出电压(GATEH)	V_{HB}-0.3到V_{VCCHB}+0.3
LLC低压端输出电压(GATEL)	-0.3 V到VCCL+0.3
GNDP到GND	-0.3 V到+0.3
GND到GNDL	-0.3 V到+0.3
功率耗散	700 mW
相对于GND的终端电压	
3.3 V容差引脚	-0.3 V到V_{REF}+0.3 V
ISL和ISP引脚	-0.65 V到V_{REF}+0.3 V
ISL和ISP引脚，最大电流	-100 mA
I_{FMAX}	120 µA

表 1 绝对最大额定值

直流工作特性

表2列出了PLC810PG的所有输入及输出的最小、典型及最大直流工作电压及电流。负电流流出IC，正电流流入IC。除非另有说明，否则直流工作特性应为结温度-10 °C到125 °C，VCC = 12 V。所有电压均与GNDP、GNDL或GND (0 V)相关。VCC指定的引脚名称是指VCC、VCCL及VCCHB。该引脚上的电压分别是指GNDP/GND、GNDL及HB。

参数	符号	引脚	注释	最小值	典型值	最大值	单位
电源电流							
启动电流	I_{CCOFF}	VCC	VCC/VCCL = UVLO - VCCHB = 0		60	120	µA
		VCCL			1.1	2	mA
抑制电流	$I_{CCINHIBIT}$	VCC	V(FBP) < INH（抑制状态）VCC/VCCL = 12 V VCCHB = 0		0.7	1.5	mA
		VCCL			1.1	2	
工作电流	I_{CCON}	VCC	PFC和LLC工作频率100 kHz / 占空比50%，GATE输出无负载，V_{REF}空载 VCC/VCCL/VCCHB = 12 V		3.0	4.5	mA
		(VCCL + VCCHB)			7	9	
漏电流	I_{OZ}	ISP, ISL, FBP, VCOMP, FMAX	0 < Vin < V_{REF}器件处于UVLO状态	-10		10	µA
漏电流	I_{OZ}	ISP	Vin = -0.48 V		-10	-800	µA

参数	符号	引脚	注释	最小值	典型值	最大值	单位
欠压锁存							
VCC启动阈值电压	$V_{UVLO(+)}$	VCC	VCC超过$V_{UVLO(+)}$时器件退出UVLO状态	8.2	9.1	10	V
		VCCHB - HB			9.2		
VCC关断阈值电压	$V_{UVLO(-)}$	VCC	VCC低于$V_{UVLO(-)}$时器件进入UVLO状态	7.2	8.1	9.0	V
		VCCHB - HB			8.7		
VCC启动/关断迟滞	$V_{UVLO(HYST)}$	VCC		0.7	1.0	1.3	V
LLC VCO							
VCO频率范围	F_{RANGE}	FBL	LLC/PFC同步	50		300	kHz
VCO最小频率限值的精确度	F_{MINACC}	FBL	R(FBL) = 100 kΩ到VREF	-15		+15	%
VCO最大频率限值的精确度	F_{MAXACC}	FMAX	R(FMAX) = 17.8 kΩ到VREF	-15		+15	%
LLC占空比	DVCO	GATEH, GATEL	导通时间匹配 GATEH (GATEH + GATEL)	49	50	51	%
死区时间精确度	$t_{DVCOACC}$	GATEH, GATEL	R(FMAX) = 17.8 kΩ到VREF	-8		+12	%
最大FMAX电流	I_{FMAX}	FMAX	功率耗散限值，I_{FBL}由流入FMAX的电流进行控制			135	µA
FBL电流上限	I_{FBL}	FBL	FBL控制VCO的工作范围		95		% I_{FMAX}
FBL等效输入电路	$V_{IN(FBL)}$	FBL	FBL输入用作与$V_{IN(FBL)}$串联的$R_{IN(FBL)}$ $I_{(FBL)}$从50 µA到130 µA		0.65		V
	$R_{IN(FBL)}$				3.3		kΩ
FBL引脚电压	V_{FBL}	FBL	F_{VCO} = 100 kHz		0.83		V
FBL软启动上拉电阻	$R_{PU(SS)}$	FBL	软启动复位时内部上拉至V_{REF}（4096 F_{MAX}个瞬态周期）		900	1500	Ω
LLC快速过流故障电压阈值	$V_{ISL(F)}$	ISL		1.33	1.4	1.47	V
LLC慢速过流故障电压阈值	$V_{ISL(S)}$	ISL	8周期去抖	0.385	0.5	0.525	V
LLC过流故障脉宽	T_{OVL}	ISL	VISL超过每周期$V_{ISL(F)}$/$V_{ISL(S)}$触发故障的最短时间		75		ns

参数	符号	引脚	注释	最小值	典型值	最大值	单位
PFC							
PFC过流限制阈值	V_{OC}	ISP	静态测量 参见注释2	-440	-480	-520	mV
PFC输出连续占空比范围	DC_{PFC}	GATEP		0		100	%
PFC误差放大器参考	V_{FBPREF}	FBP			2.2		V
PFC误差放大器参考精确度	FBPREF	FBP		-2		2	%
PFC过压阈值	$V_{OV(H)}$	FBP	参见注释1	103	105	107	$\%V_{FBPREF}$
PFC抑制上限阈值	INH	FBP	参见注释1	25	26	27	$\%V_{FBPREF}$
PFC抑制下限阈值	INL	FBP	参见注释1	22	23	24	$\%V_{FBPREF}$
跨导	G_M	FBP	$V_{FBP} = V_{FBPREF}$ ±85 mV	55	85	115	µA/V
LLC							
LLC关断上限阈值	$V_{SD(H)}$	FBP	参见注释1	94.5	95.5	96.5	$\%V_{FBPREF}$
LLC关断下限阈值	$V_{SD(L)}$	FBP	参见注释1	63	64	65	$\%V_{FBPREF}$
参考							
参考电压	V_{REF}	V_{REF}	负载电流I_{REF}	3.09	3.25	3.41	V
V_{REF}引脚的电流源能力	I_{REF}	V_{REF}				5	mA
V_{REF}电容容量	C_{REF}	V_{REF}	V_{REF}引脚上所需的外部退耦电容容量	1			µF
PFC GATE输出							
PFC GATE输出电压	$V_{GATE(P)}$	GATEP		GND		VCC	
输出短路高驱动电流	$I_{SC(H)}$	GATEP			25		mA
输出短路低驱动电流	$I_{SC(L)}$	GATEP			60		mA
输出高压	$V_{O(H)}$	GATEP	VCC = 12 V I_{OH} = 1.25 mA	11.5	11.8		V
输出低压	$V_{O(L)}$	GATEP	VCC = 12 V I_{OL} = 5 mA		0.5	0.75	V

参数	符号	引脚	注释	最小值	典型值	最大值	单位
LLC GATE驱动器							
LLC高压端输出电压	$V_{GATE(H)}$	GATEH		VHB		VCCHB	
LLC低压端输出电压	$V_{GATE(L)}$	GATEL		VCOM		VCCL	
输出高压	$V_{O(H)}$	GATEH, GATEL	VCCL/VCCHB = 12 V I_{OH} = -65 mA	11	11.4		V
输出低压	$V_{O(L)}$	GATEH, GATEL	VCCL/VCCHB = 12 V I_{OL} = 130 mA		0.5	1	V
输出短路高驱动电流	$I_{SC(H)}$	GATEH/ GATEL	VCCL/VCCHB = 12 V PW <10 μS		-0.8	-0.5	A
输出短路低驱动电流	$I_{SC(L)}$	GATEH/ GATEL	VCCL/VCCHB = 12 V PW <10 μS	0.9	1.4		A
HB引脚上的最大允许压摆率	$dV_{HB/dt}$	HB			10		V/nsec
导通上升时间 (10% - 90%)	T_R	GATEH, GATEL	VCCL/VCCHB = 12 V 1000 pF load capacitance		50		nsec
关断下降时间 (90% - 10%)	T_F	GATEH, GATEL	VCCL/VCCHB = 12 V 1000 pF load capacitance		25		nsec

表 2. 直流工作特性

注释：

1. 该参数跟踪V_{FBPREF}。

典型性能特性

图 14. 从FMAX引脚到VREF引脚的上拉电阻与死区时间要求的比例关系

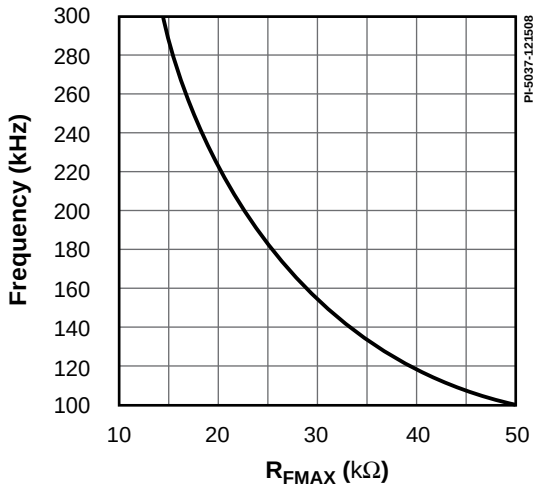


图 15. 最大频率限值与从FMAX引脚到VREF引脚的上拉电阻的比例关系

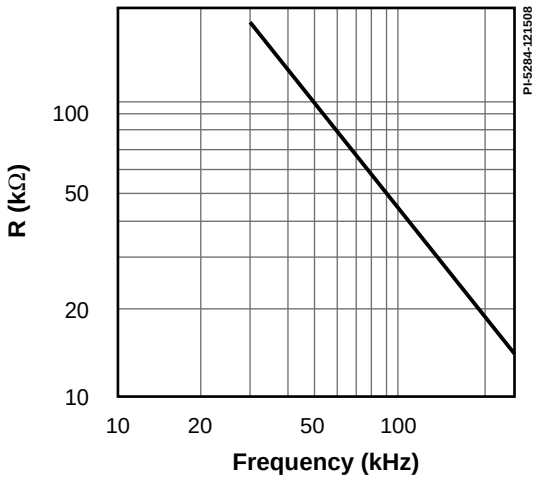


图 16. 从FBL引脚到VREF引脚的上拉电阻与开关频率的比例关系

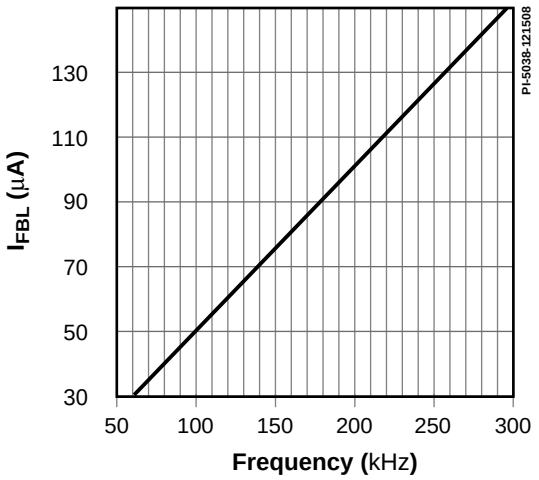
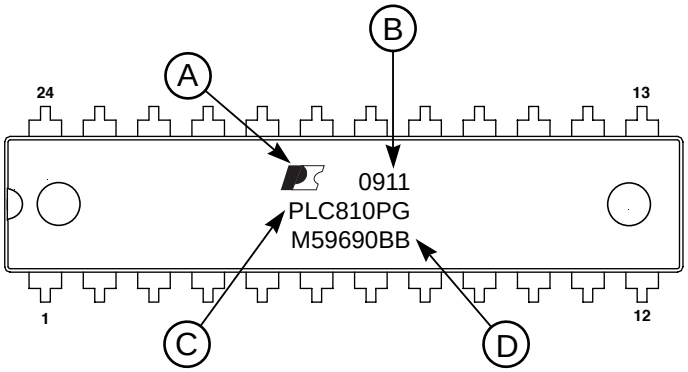


图 17. FBL引脚电流与开关频率的比例关系

封装信息与元件标识

PLC810PG采用24 Lead 0.300 PDIP封装（图18所示为PLC810PG
元件标识）。图19所示为封装外形及尺寸。

HiperPLC MARKING

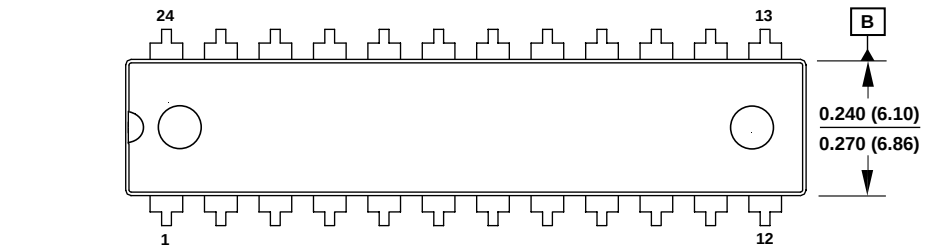


A. Power Integrations Registered Trademark
B. Encapsulation Date Code (last two digits of year followed by 2-digit work week)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code

PI-5163-081309

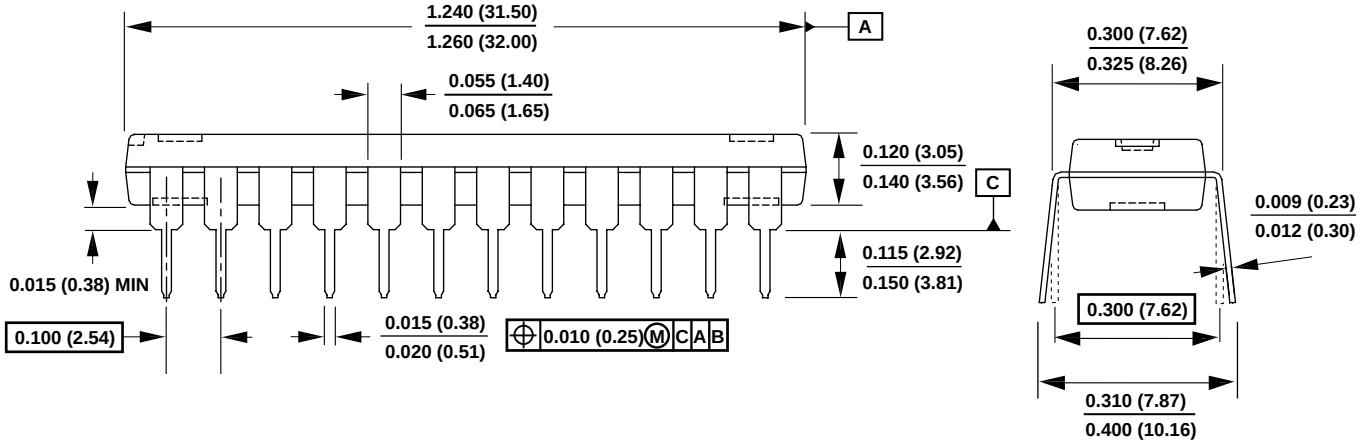
图 18. PLC810PG元件标识

PDIP-24 (0.300”)



Notes:

1. **Package dimensions conform to JEDEC specification MS-001.**
2. **Controlling dimensions are inches. Dimensions in millimeters are in parenthesis.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed 0.006 (0.15) on any side.**
4. **A and B are reference datums on the molded body. C is the datum at the seating plane.**
5. **Dimensioning and tolerancing per ASME Y14.5M-1994**



PI-5181-110708

图 19. PDIP-24封装标识

注释

注释

版本	注释	日期
A	初始版本	11/08
B	图片和文字修订	11/08
C	文字和电路图更新	12/08
D	电路图更新	02/09
E	更改了图4并从参数表中去掉注释2	05/09
F	更改了图4、6、14、18	08/09

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Design Example Report

Title	***150 W Power Factor Corrected LLC Power Supply Using HiperPLC (PLC810PG)***
Specification	140 – 265 VAC Input; 150 W (48 V at 0.05 A – 3.125 A) Output
Application	LED Street Light
Author	Applications Engineering Department
Document Number	DER-212
Date	June 1, 2009
Revision	1.1

Summary and Features

- Integrated PFC and LLC controller
- Continuous mode PFC using small low-cost ferrite core and magnet wire
- Frequency and Phase locked PFC and LLC for ripple cancellation in bulk capacitor for reduced ripple current, reduced bulk capacitor size and reduced EMI filter cost
- Tight LLC duty-cycle matching
- Tight LLC dead-time control
- >95% full load PFC efficiency at 140 VAC using conventional ultrafast rectifier
- >95% full load LLC efficiency
- >92% full load system efficiency

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Table of Contents

Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a 150 W reference design power supply for 230 VAC input LED street lights and also serves as a general purpose evaluation board for the PLC810PG

The design is based on the PLC810PG controller IC which integrates both continuous current mode (CCM) boost PFC and resonant half-bridge (LLC) control functions together with high-side and low side drivers for the LLC stage MOSFETs. To allow optimum design of the LLC transformer (T1) for high efficiency (high k factor – the ratio of parallel to series inductance) the design operates in burst mode at zero load. The supply is thus protected against output overvoltage at low/zero load, but it will not deliver a steady output voltage at zero load. A practical LED street light power supply design that includes an auxiliary output winding to power the LED driver circuitry may not have this limitation.

DER-212 demonstrates a design using the commonly employed single transformer and resonant inductor magnetic component (integrated magnetics) for the LLC stage (common in display applications). However, the PLC810 may as easily be used with separated transformer and resonating inductor. PI design materials support both approaches.

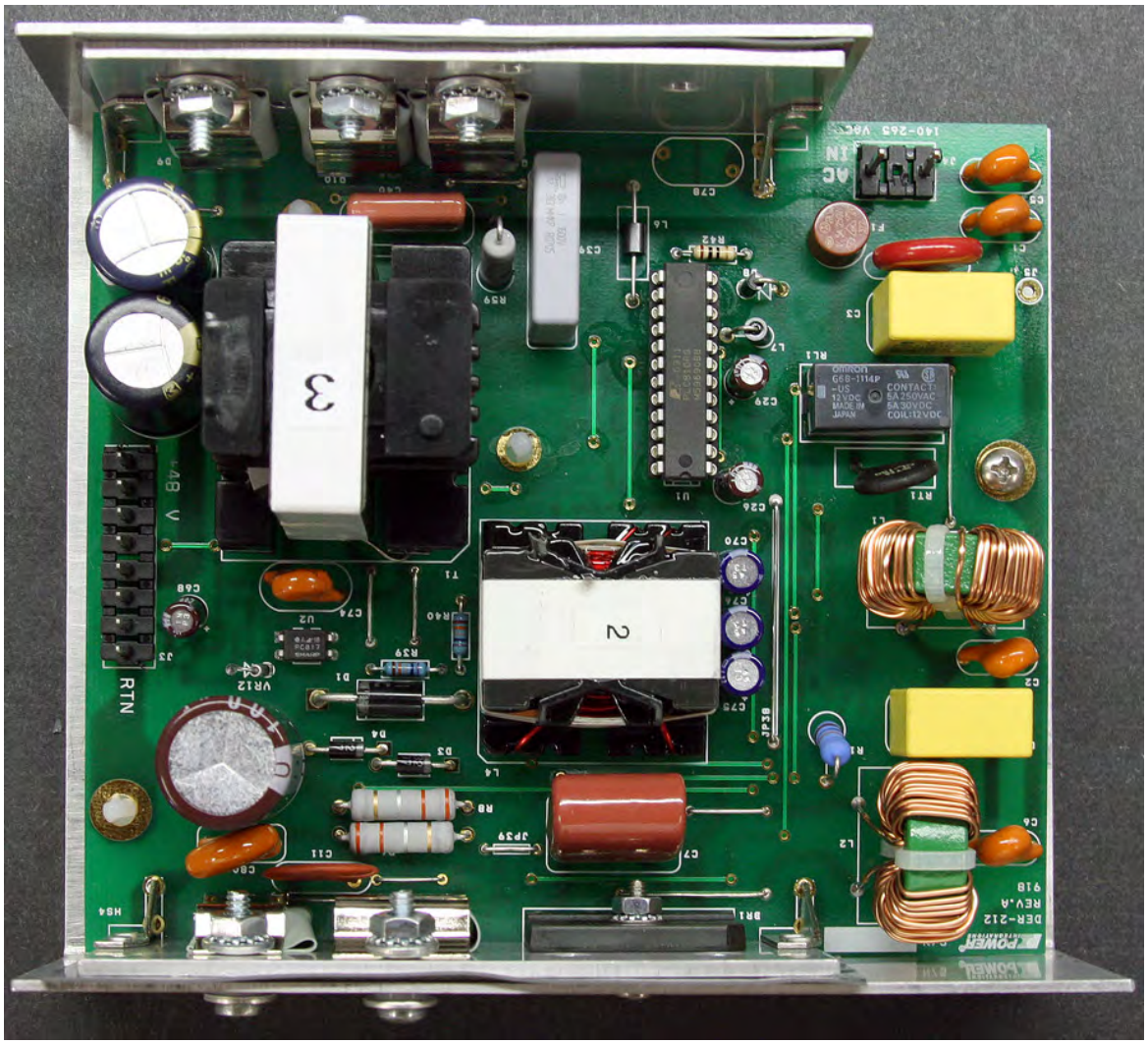

Figure 1 – DER-212 Photograph, Top View.

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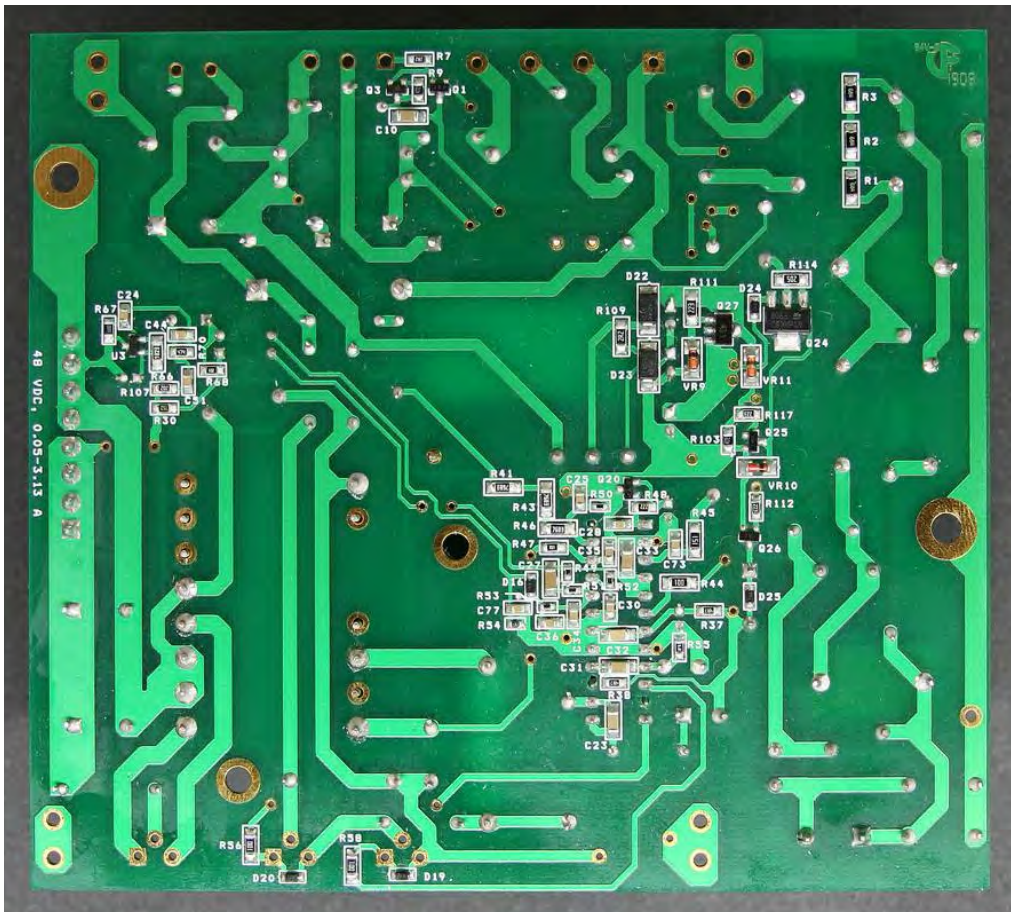

Figure 2 – DER-212 Photograph, Bottom View.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	140		265	VAC	3 Wire input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Power Factor	**PF**	0.97				Full load, 230 VAC
Main Converter Output						
Output Voltage	V_{LG}	45.6	48	50.4	V	48 VDC ± 5%
Output Ripple	$V_{RIPPLE(LG)}$			150	mV P-P	20 MHz bandwidth
Output Current	I_{LG}	0.05*	3.13	3.13	A	*Supply is protected under no-load conditions
Total Output Power						
Continuous Output Power	P_{OUT}		150		W	
Efficiency						
Total system at Full Load	η_{Main}	91 92			%	Measured at 140 VAC, Full Load Measured at 230 VAC, Full Load
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950 / UL1950 Class II				
Surge						1.2/50 µs surge, IEC 1000-4-5,
Differential		1			kV	Differential Mode: 2 Ω
Common Mode		2			kV	Common Mode: 12 Ω
100 kHz Ring Wave		2			kV	500 A short circuit current
Ambient Temperature	T_{AMB}	0		60	°C	See thermal section for conditions

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3 Schematic

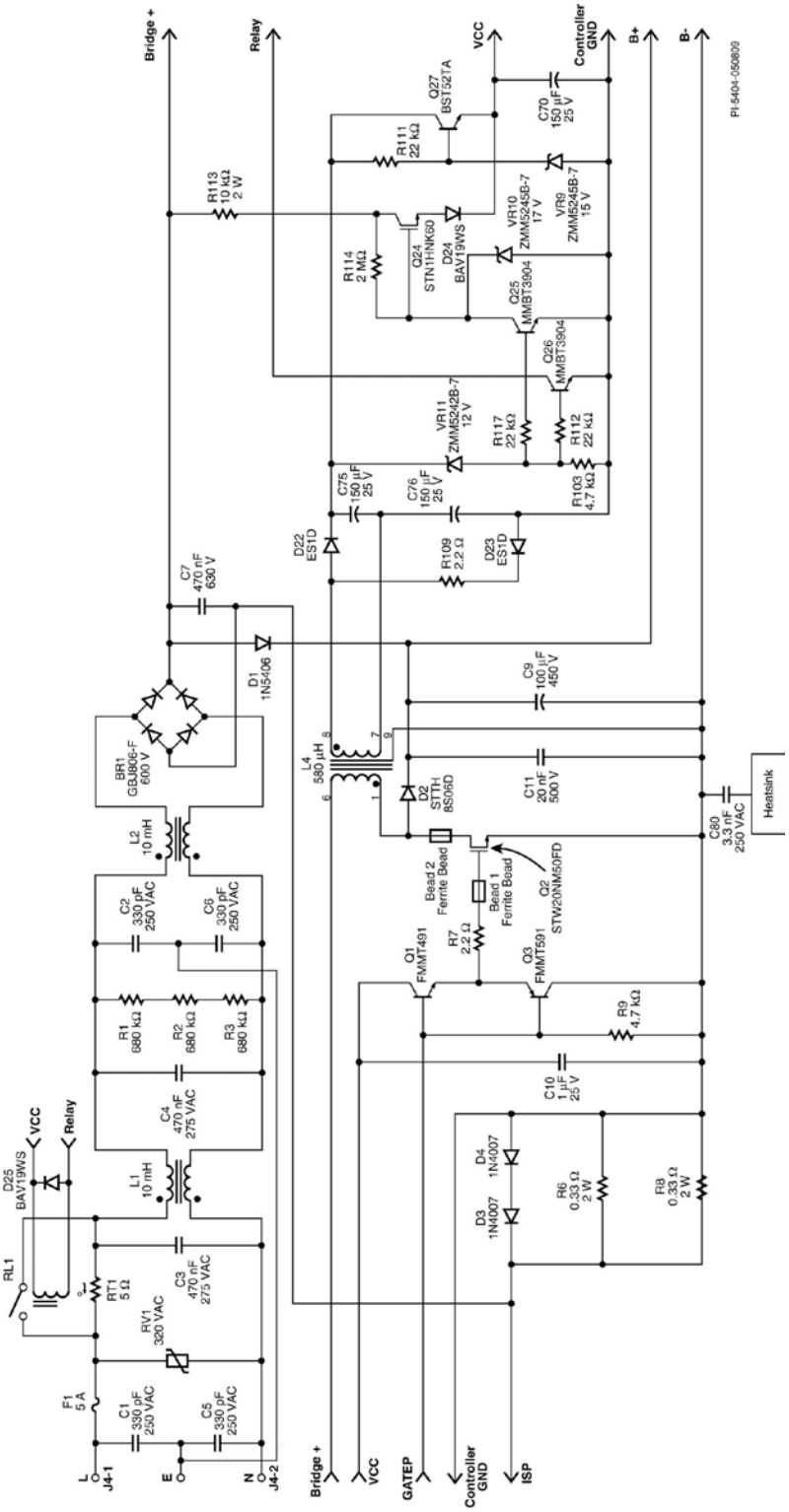

Figure 3 – Schematic of PLC810PG LCD Street Light Power Supply Application Circuit, Input Circuit and PFC Power Stage.

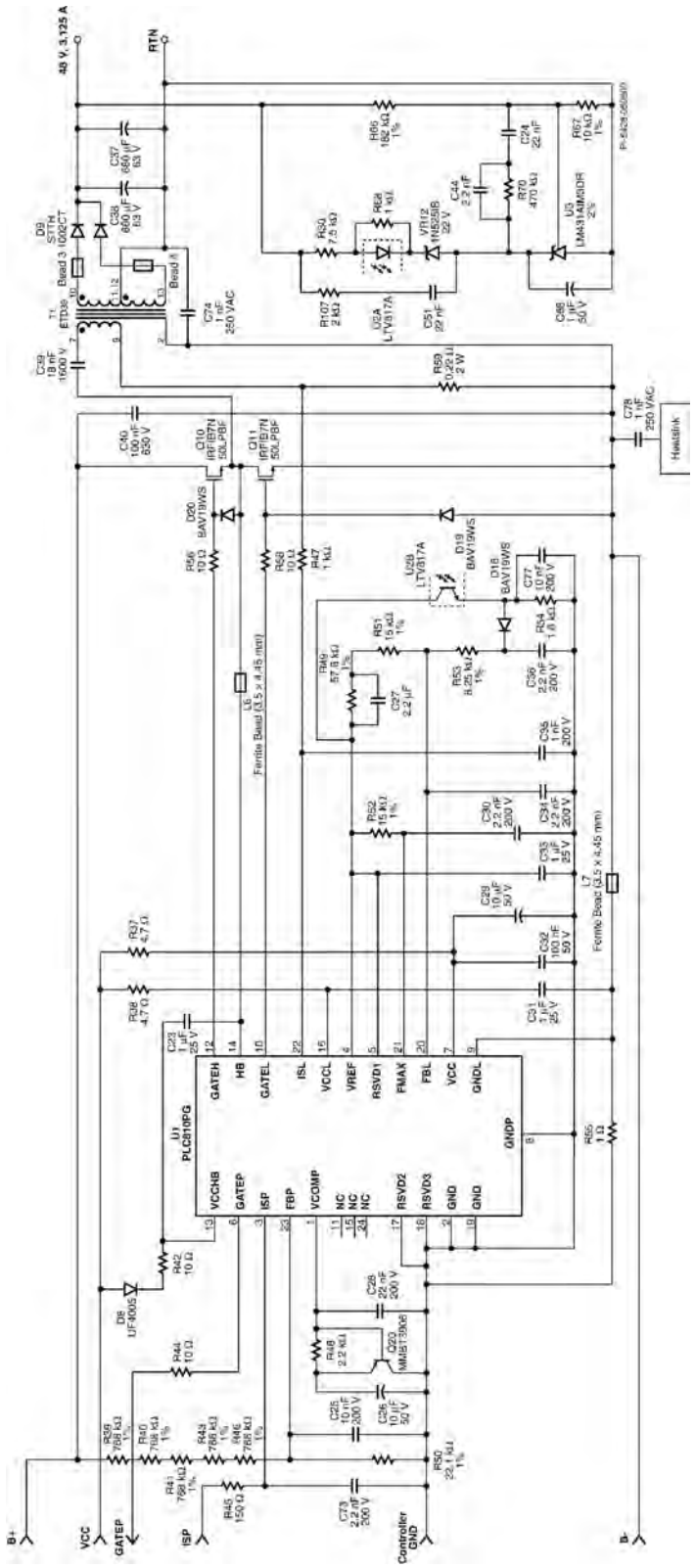

Figure 4 – Schematic of PLC810PG LCD Street Light Power Supply Application Circuit, PFC Circuit Control Inputs and LLC Stage.

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4 Circuit Description

The main converter uses the PLC810PG in a primary-side-control, PFC + LLC configuration.

4.1 Input Filter / Boost Converter / Bias Supply

The schematic in Figure 3 shows the input EMI filter, main PFC stage, and primary bias supply/start-up circuit.

4.1.1 EMI Filtering

Capacitors C1 and C5 are connected directly from Line and Neutral to protective Earth ground and are used to control common mode noise at frequencies greater than 30 MHz. Common mode inductors L1 and L2 control EMI at low frequencies and mid-band (<10 MHz), respectively. Capacitors C2 and C6 control resonant peaks in the mid-band region.

PFC inductor L4 has a grounded shield band to prevent electrostatic and magnetic noise coupling to the EMI filter components. Capacitors C3 and C4 provide differential mode EMI filtering. To meet safety requirements resistors R1, R2 and R3 discharge these capacitors when AC is removed. The heat sink for PFC switch FET Q2 and PFC output diode D2 is tied to primary return at the cathode of D3 via capacitor C80 to eliminate the heat sink as a source of conducted noise into the chassis/protective Earth ground.

4.1.2 Inrush Limiting

Thermistor RT1 provides inrush limiting. It is shorted by relay RL1 during normal operation, increasing efficiency by approximately 1 - 1.5%.

4.1.3 Main PFC Stage

Components C9, C11, L4, Q2, and D2 form a continuous mode power factor correction circuit. Components Q1, Q3, R7, R9 and bead 1 buffer the PWM drive signal for Q2 from the PLC810 controller. Resistor R7 allows the turn-off speed of Q2 to be adjusted to optimize the losses between D2 and Q2. In this design it was found that efficiency and EMI were both improved by reducing the value of R7 and adding ferrite beads to the gate and drain of Q2 (bead 1 and bead 2 respectively). In general, increasing MOSFET turn on drive current reduces MOSFET switching losses but increases the reverse recovery current through D2 and associated ringing. An ultra fast diode was selected for D2 as a lower cost alternative to a silicon carbide or other proprietary diode technology. These may provide higher efficiency by reducing reverse recovery charge, but significantly increase solution cost.

A 220 MΩ, 500 V power MOSFET was selected for Q2 to maximize the efficiency of the PFC stage. A TO-247 package device was selected for better heat transfer.

Capacitor C10 provides local bypassing for the drive circuit. Current sensing for the PFC stage is provided by R6 and R8. The sense voltage is clamped to two diode drops by D3 and D4, protecting the current sense input of the controller IC during fault conditions. Diode D1 charges the PFC output capacitor (C9) when AC is first applied. This routes the inrush current around the PFC inductor L4 preventing it from saturating and causing stress in Q2 and D2 when the PFC stage begins to operate. Capacitor C11 is used to shrink the high frequency loop around components Q2, D2 and C9 to reduce EMI. The incoming AC is rectified by BR1 and filtered by C7. Capacitor C7 was selected as a low-loss polypropylene type due to its low loss and low impedance characteristics. This capacitor provides the high instantaneous current through L4 during Q2 on-time.

4.1.4 Primary Bias Supply / Start-up

Components D22, D23, C75, C76, and R109 act as a voltage doubler circuit to rectify and filter the output of a floating bias winding on PFC choke L4, providing a bias voltage relatively independent of input voltage.

Components Q24, Q25, Q27, VR9, VR10, VR11, D24, C70, R103, R111, R113, R114, and R117 constitute the bias regulator and start-up functions. Resistor R113 charges capacitor C70 through mosfet Q24 to provide start-up bias for controller U1. The Q24 output voltage is clamped by VR10. Transistor Q25 shuts off the start-up circuit when the primary bias supply reaches regulation. Darlington transistor Q27, R111, and VR9 form a simple emitter-follower voltage regulator. Transistor Q26 switches on relay RL1 when the primary bias supply reaches regulation, shorting out thermistor RT1.

4.2 Controller / Main LLC Output

Figure 4 shows the schematic of the main controller circuit and LLC converter stage.

4.2.1 LLC Input Stage

MOSFETs Q10 and Q11 are the switch MOSFETs for the LLC converter. They are driven directly by the controller IC via resistors R56 and R58. Capacitor C39 is the primary resonating capacitor, and should be a low-loss type rated for the RMS current at maximum load. Capacitor C40 is used for local bypassing, and is positioned adjacent to Q10 and Q11. Resistor R59 provides primary current sensing to the controller for overpower protection.

4.2.2 LLC Outputs

The secondaries of transformer T1 are rectified and filtered by D9, and C37-38 to provide the +48 V output.

4.2.3 Controller

Figure 4 also shows the circuitry around the main controller IC U1, which provides control functions for the input PFC and output LLC stages.

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4.2.4 PFC Control

The PFC boost stage output voltage is fed back to the boost voltage sense pin (FBP of U13) via resistors R39-41, R43, R46, and R50. Capacitor C25 filters noise. Components C26, C28 and R48 provide frequency compensation for the PFC. Transistor Q20 turns on during large signal excursions, bypassing C26. This allows fast slewing of the PFC control loop in response to a large load step. The PFC current sense signal from resistors R6 and R8 is filtered by R45 and C73. The PFC drive signal from the GATEP pin is routed to the main switching FET via R44. This damps any ringing in the PFC drive signal caused by the trace length from U1 to PFC switch MOSFET Q2.

4.2.5 Bypassing / Ground Isolation

Capacitors C29, C31, and C32 provide supply bypassing for the analog and digital supply rails for U1. Resistor R55 and ferrite bead L7 provide ground isolation between the PFC and LLC ground systems. Resistors R37 and R38 isolate the IC analog and digital supply rails. Ferrite bead L6 provides high frequency isolation between the LLC stage high side MOSFET drive return and the controller IC.

4.2.6 LLC Control

Feedback from the LLC output sense/feedback circuit is provided by U2, which develops a feedback voltage across resistor R54. Capacitor C77 filters the feedback signal. Resistors R49, R51, and R53 set the lower frequency limit for the LLC converter stage. Capacitor C27 is used to provide output soft start. Resistor R52 sets the LLC upper frequency limit. Capacitors C30 and C36 are noise filters. The LLC overload sense signal from resistor R59 is filtered by R47 and C35. Components C23, R42, and D8 provide bootstrapping for the LLC top side MOSFET drive. Resistors R52 and R53 were selected to force the LLC converter into burst mode at low/zero output load, protecting the output from overvoltage. This operation mode was selected (vs. allowing operation at a higher frequency at no-load) to give adequate dead time and ensure ZVS operation. The alternative would be to adjust the ratio of parallel and series inductance (k factor) however this reduces full load efficiency.

4.3 LLC Secondary Control Circuits

Figure 4 shows the secondary control schematic for the LLC stage.

4.3.1 Voltage Feedback

The LLC converter 48 V output is sensed by resistors R67 and R68. Zener diode VR12 drops the 48 V output to protect regulator U3. Components C24, C44, C51, R30, R70, and R107 provide frequency compensation for the LLC stage.

5 PCB Layout

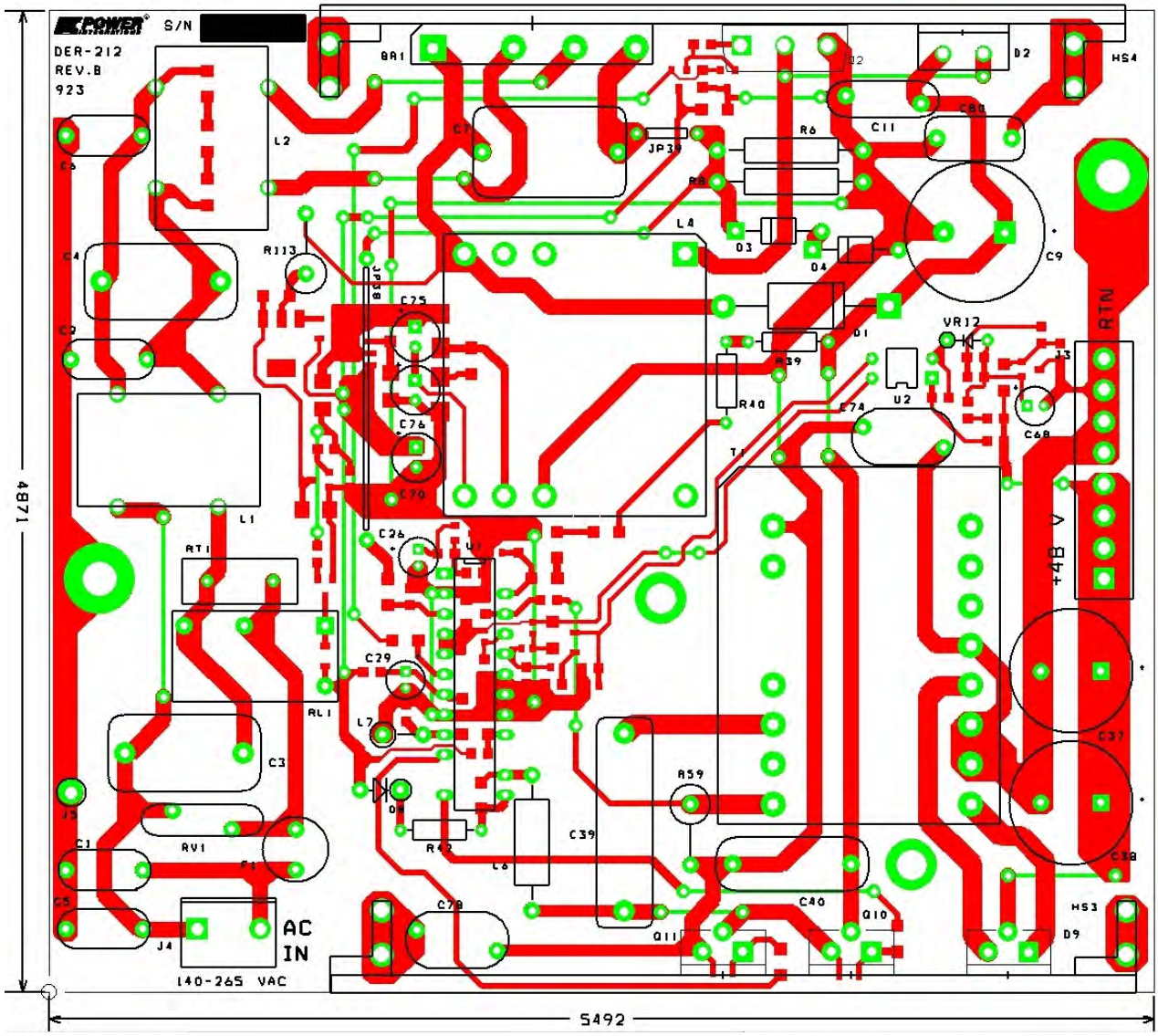

Figure 5 – Printed Circuit Layout, Top Side.

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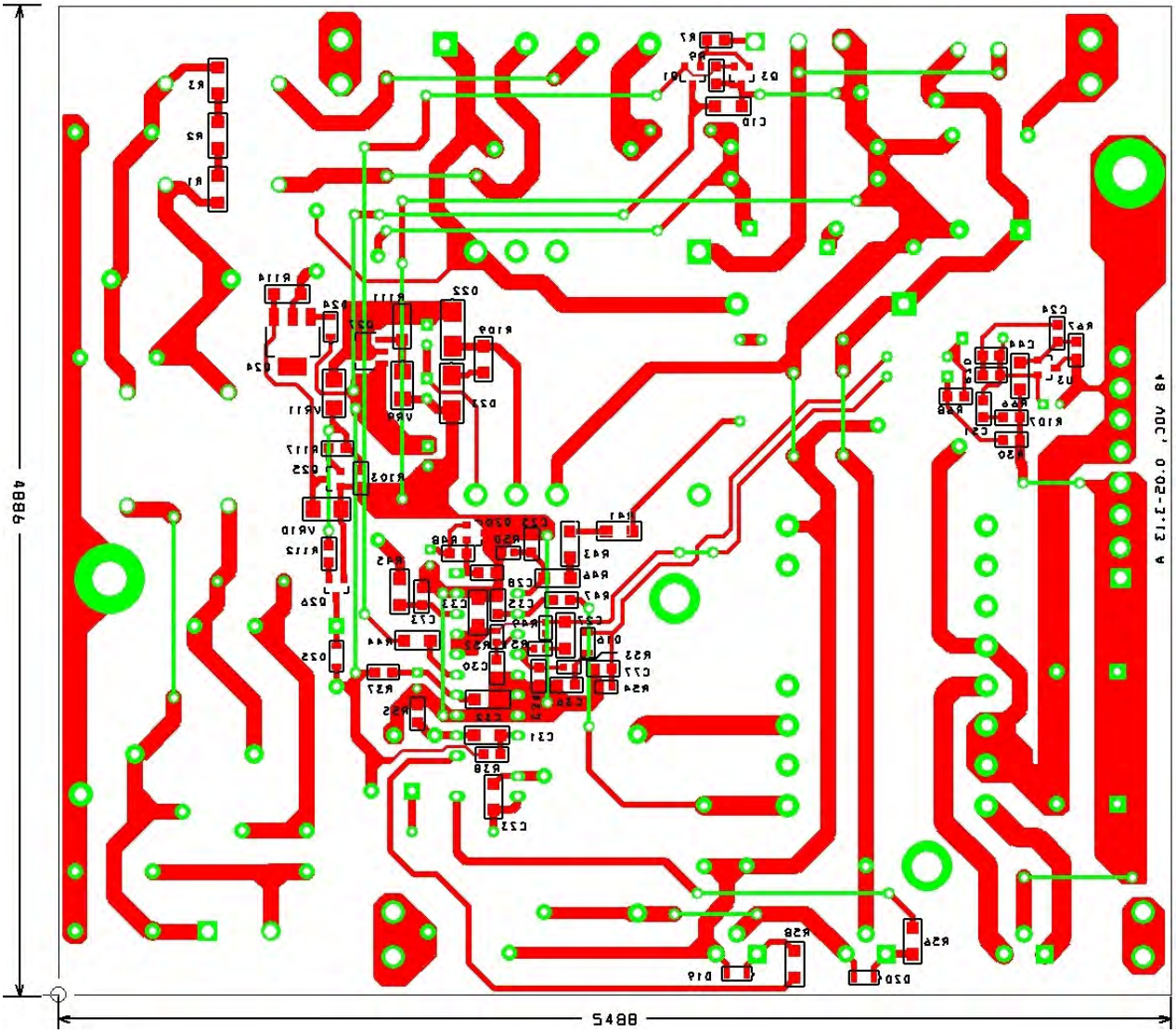

Figure 6 – Printed Circuit Layout, Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	4	BEAD1 BEAD2 BEAD3 BEAD4	3.5 mm D x 3.25 L mm, 21 Ω at 25 MHz, 1.6mm (.063) hole, Ferrite Bead	2643001501	Fair-Rite
2	1	BR1	600 V, 8 A, Bridge Rectifier, GBJ Package	GBJ806-F	Diodes Inc
3	4	C1 C2 C5 C6	330 pF, Ceramic Y1	440LT33-R	Vishay
4	2	C3 C4	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli
5	1	C7	470 nF, 630 V, Polypropylene Film	ECW-F6474JL	Panasonic
6	1	C9	100 µF, 450 V, Electrolytic, Low ESR, (18 x 30)	EPAG451ELL101MM35S	Nippon Chemi-Con
7	4	C10 C23 C31 C33	1 µF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E105K	Panasonic
8	1	C11	20 nF, 500 V, Disc Ceramic	D203Z59Z5UL63L0R	Vishay/BC
9	3	C24 C28 C51	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX Corp
10	2	C25 C77	10 nF, 200 V, Ceramic, X7R, 0805	08052C103KAT2A	AVX Corp
11	2	C26 C29	10 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
12	1	C27	2.2 µF, 25 V, Ceramic, X7R, 1206	ECJ-3YB1E225K	Panasonic
13	5	C30 C34 C36 C44 C73	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX Corp
14	1	C32	100 nF, 50 V, Ceramic, X7R, 1206	ECJ-3VB1H104K	Panasonic
15	1	C35	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX Corp
16	2	C37 C38	680 µF, 63 V, Electrolytic, Low ESR, 50 mΩ, (16 x 25)	EEU-FC1J681	Panasonic
17	1	C39	18 nF, 1600 V, Film	2222 383 50183	Vishay
18	1	C40	100 nF, 630 V, Film	ECQ-E6104KF	Panasonic
19	1	C68	1 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL1R0ME11D	Nippon Chemi-Con
20	3	C70 C75 C76	150 uF, 25 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ250ELL151MF15D	Nippon Chemi-Con
21	2	C74 C78	1 nF, Ceramic, Y1	440LD10-R	Vishay
22	1	C80	3.3 nF, Ceramic, Y1	440LD33-R	Vishay
23	1	D1	600 V, 3 A, Recitifier, DO-201AD	1N5406	Vishay
24	1	D2	600 V, 8 A, Ultrafast Recovery, 12 ns, TO-220AC	STTH8S06D	ST Semiconductor
25	2	D3 D4	1000 V, 1 A, Rectifier, DO-41	1N4007-E3/54	Vishay
26	1	D8	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
27	1	D9	200 V, 10 A, Dual Ultrafast Recovery, 25 ns, TO-220AB	STTH1002CT	ST
28	5	D16 D19 D20 D24 D25	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
29	2	D22 D23	200 V, 1 A, Ultrafast Recovery, 25 ns, DO-214AC	ES1D	Vishay
30	1	DER-212 PRIMARY INSULATOR	Thermal Conductive insulator, DER-212 Pri Htsnk, 0.5mm Silicone		Power Integrations
31	1	DER-212 SECONDARY INSULATOR	Thermal Conductive insulator, DER-212 Sec Htsnk, 0.5mm Silicone		Power Integrations
32	1	F1	5 A, 250 V, Slow, TR5	3721500041	Wickman

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33	1	GREASE1	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics
34	1	GND CABLE ASSY, DER-212	Cable ASSY, 18 GA GRN/YEL, 6 in, with ring terminal		
35	1	HS/BRACKET, DER-212	Heatsink/Mounting Bracket, DER-212		
36	2	HS3 HS4	HEATSINK, Custom, Al, 1100, 0.090" Thk		Power Integrations
37	1	J3	8 Position (1 x 8) header, 0.156 pitch, Vertical	26-48-1081	Molex
38	1	J4	3 Position (1 x 3) header, 0.156 pitch, Vertical	B3P-VH	JST
39	1	JP38	Wire Jumper, Non insulated, 22 AWG, 1.4 in	298	Alpha
40	1	JP39	Wire Jumper, Non insulated, 22 AWG, 0.3 in	298	Alpha
41	2	L1 L2	Common Mode Choke Toroidal	P/N T22148-902S (Order PI Taiwan)	Fontaine Tech CO. LTD
42	1	L4	CC Mode PFC Choke, PQ32/20		
43	2	L6 L7	3.5 mm x 4.45 mm, 68 Ohms at 100 MHz, 22 AWG hole, Ferrite Bead	2743001112	Fair-Rite
44	4	MAX CLIP1 MAX CLIP2 MAX CLIP3 MAX CLIP4	Hardware, Heatsink MaxClip, TO220/Max247 11.2lb 0.87 x 12 mm	MAX07G	Aavid Thermalloy
45	1	MAX CLIP5	Hardware, Heatsink MaxClip, TO218/TO247 16.9lb 0.93 x 18 mm	MAX08G	Aavid Thermalloy
46	1	NUT1	Nut, Hex, Kep 4-40, S ZN Cr3 plateing RoHS	4CKNTZR	Olander
47	6	NUT2 NUT3 NUT4 NUT5 NUT6 NUT7	Nut, Hex, Kep 6-32, Zinc Plate	6CKNTZR	Olander
48	1	Q1	NPN, 60 V 1000 MA, SOT-23	FMMT491TA	Zetex Inc
49	1	Q2	500 V, 20 A, 220 mOhm, N-Channel, TO-247AC	STW20NM50FD	ST
50	1	Q3	PNP, 60 V 1000 MA, SOT-23	FMMT591TA	Zetex Inc
51	2	Q10 Q11	500 V, 6.8 A, 320 mOhm. N-Channel, TO-247AC	IRFIB7N50LPBF	IR/Vishay
52	1	Q20	PNP, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3906LT1G	On Semiconductor
53	1	Q24	600 V, 400 mA, 8.5 Ohm, N-Channel, SOT 223	STN1HNK60	ST
54	2	Q25 Q26	NPN, Small Signal BJT, 40 V, 0.2 A, SOT-23	MMBT3904LT1G	On Semiconductor
55	1	Q27	NPN, DARL 80 V 500 MA, SOT-89	BST52TA	Zetex Inc
56	3	R1 R2 R3	680 kΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ684V	Panasonic
57	2	R6 R8	0.33 Ω, 5%, 2 W, Metal Oxide	MO200J0R33B	Synton-Tech corporation
58	1	R7	2.2 Ω, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ2R2V	Panasonic
59	2	R9 R103	4.7 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ472V	Panasonic
60	1	R30	7.5 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ752V	Panasonic
61	2	R37 R38	4.7 Ω, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ4R7V	Panasonic
62	2	R39 R40	768 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-768K	Yageo
63	3	R41 R43 R46	768 kΩ, 1%, 1/4 W, Metal Film, 1206	ERJ-8ENF7683V	Panasonic
64	1	R42	10 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-10R	Yageo
65	3	R44 R56 R58	10 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ100V	Panasonic
66	1	R45	150 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ151V	Panasonic
67	2	R47 R68	1 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ102V	Panasonic
68	1	R48	2.2 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ222V	Panasonic

69	1	R49	57.6 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF5762V	Panasonic
70	1	R50	22.1 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF2212V	Panasonic
71	2	R51 R52	15 kΩ, 1%, 1/16 W, Metal Film, 0603	ERJ-3EKF1502V	Panasonic
72	1	R53	8.25 kΩ, 1%, 1/8 W, Metal Film, 0603	ERJ-3EKF8251V	Panasonic
73	1	R54	1.8 kΩ, 5%, 1/10 W, Metal Film, 0603	ERJ-3GEYJ182V	Panasonic
74	1	R55	1 Ω, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ1R0V	Panasonic
75	1	R59	0.22 Ω, 5%, 2 W, Metal Oxide	MO200J0R22B	Synton-Tech Corporation
76	1	R66	182 kΩ, 1%, 1/4 W, Metal Film, 1206	ERJ-8ENF1823V	Panasonic
77	1	R67	10 kΩ, 1%, 1/8 W, Metal Film, 0805	ERJ-6ENF1002V	Panasonic
78	1	R70	470 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ474V	Panasonic
79	1	R107	2 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ202V	Panasonic
80	1	R109	2.2 Ω, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ2R2V	Panasonic
81	1	R111	22 kΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ223V	Panasonic
82	2	R112 R117	22 kΩ, 5%, 1/8 W, Metal Film, 0805	ERJ-6GEYJ223V	Panasonic
83	1	R113	10 kΩ, 5%, 2 W, Metal Oxide	RSF200JB-10K	Yageo
84	1	R114	2 MΩ, 5%, 1/4 W, Metal Film, 1206	ERJ-8GEYJ205V	Panasonic
85	1	RL1	SPST-NO, 5A 12VDC, PC MNT	G6B-1114P-US-DC12	OMRON
86	1	RT1	NTC Thermistor, 5 Ohms, 4.7 A	CL150	Thermometrics
87	1	RV1	320 V, 84J, 15.5 mm, RADIAL	S14K320	Epcos
88	1	SCREW1	SCREW MACHINE PHIL 4-40X1/2 SS	PMSSS 440 0050 PH	Building Fasteners
89	5	SCREW2 SCREW3 SCREW4 SCREW5 SCREW6	SCREW MACHINE PHIL 6-32X1/2 SS	PMSSS 632 0050 PH	Building Fasteners
90	1	SCREW7	SCREW MACHINE PHIL 6-32X1/4 SS	PMSSS 632 0025 PH	Building Fasteners
91	4	SCREW8 SCREW9 SCREW10 SCREW11	SCREW MACHINE PHIL Flat head, Undercut 6-32 X ¼" Zinc Plated	6C25PFUZR	Olander
92	2	STDOFF1 STDOFF3	Standoff Hex,6-32, .375L,Alum	2209	Keystone Elect
93	2	STDOFF2 STDOFF4	Standoff Hex, 6-32/snap, .375L,Nylon	FTA-A 375	Eagle Hardware
94	1	T1	Custom Transformer, LLC, ETD39,Vertical, 14Pins		
95	4	TUBE-TO-220	Heatpad, TO-220 Tube 13.5 x 25 mm	SPT400-12-11-25	Bergquist
96	1	TUBE-TO-247	Heatpad, TO-247 Tube 13.5 x 25 mm	SPT400-12-13.5-25	Bergquist
97	1	U1	Controller, PFC/LLC, 24-pin DIP	PLC818PG	Power Integrations
98	1	U2	Opto coupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
99	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semiconductor
100	1	VR9	15 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5245B-7	Diodes Inc
101	1	VR10	17 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5247B-7	Diodes Inc
102	1	VR11	12 V, 5%, 500 mW, DO-213AA (MELF)	ZMM5242B-7	Diodes Inc
103	1	VR12	22 V, 5%, 500 mW, DO-35	1N5251B	Microsemi

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104	2	WASHER1 WASHER2	WASHER FLAT #4 SS	FWSS 004	Building Fasteners
105	11	WASHER3 WASHER4 WASHER5 WASHER6 WASHER7 WASHER8 WASHER9 WASHER10 WASHER11 WASHER12 WASHER13	Washer Flat #6, SS	FWSS 006	Building Fasteners
106	1	WASHER14	Bushing Nylon #4 X 0.125	MNI#4-8	Richco Plastic Co.
107	5	WASHER15 WASHER16 WASHER17 WASHER18 WASHER19	Bushing Nylon #6 X 0.125	MNI#6-8	Richco Plastic Co.

7 Magnetics

7.1 Main LLC 48 V Transformer (T1) Specification

7.1.1 Electrical Diagram

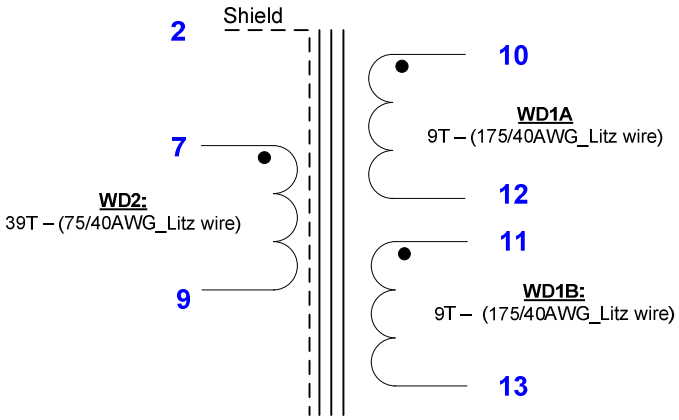

Figure 7 – Transformer Electrical Diagram.

7.1.2 Electrical Specifications

Electrical Strength	60 second, 60 Hz, from pins 1 - 9 to pins 10 - 18	3000 VAC
Primary Inductance	Pins 7 - 9, all other windings open, measured at 100 kHz, 0.4 VRMS	820 µH ±10%
Resonant Frequency	Pins 7- 9, all other windings open	700 kHz (Min.)
Primary Leakage Inductance	Pins 7 - 9, with pins 10 - 18 shorted, measured at 100 kHz, 0.4 VRMS	100 µH ±10%

7.1.3 Materials

Item	Description
[1]	Core: ETD39, Ferroxcube 3F3 material or equivalent, gap for inductance coefficient (A_L) of 539 nH/t².
[2]	Bobbin: ETD39 vertical, flanged Pinshine P-3907
[3]	Tape: Polyester film, 3M 1350F-1 or equivalent, 10.6 mm wide.
[4]	Wire: Litz, 75 strands 40WAG, solderable single coated.
[5]	Wire: Litz, 175 strands 40WAG, solderable single coated.
[6]	Tape: Copper foil 9.0 mm wide.
[7]	Tape: Polyester film, 10.0 mm wide.
[8]	Copper bus wire #24 AWG.

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7.1.4 Winding Diagram

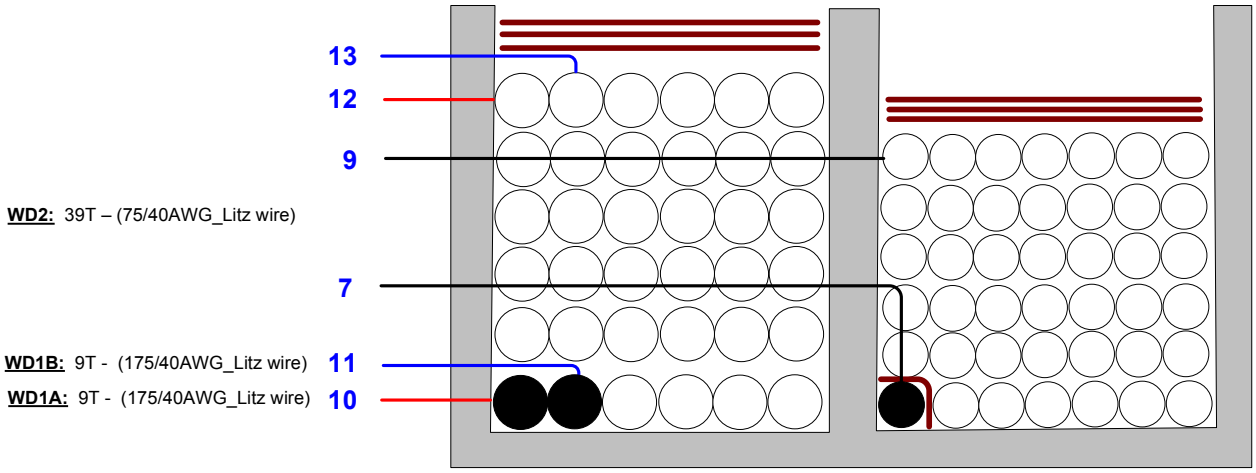
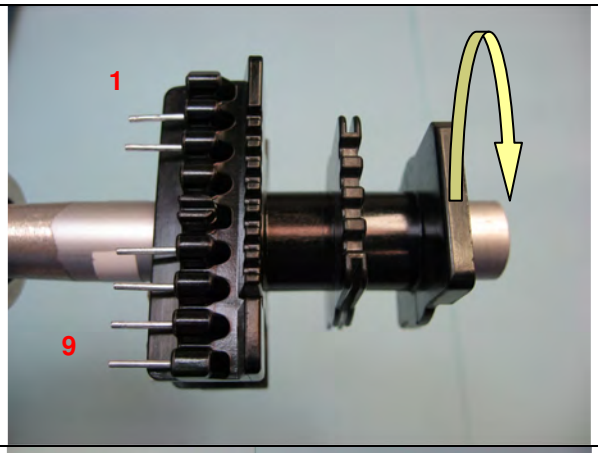
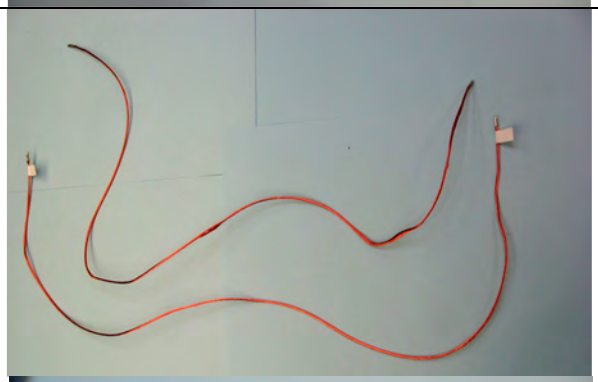
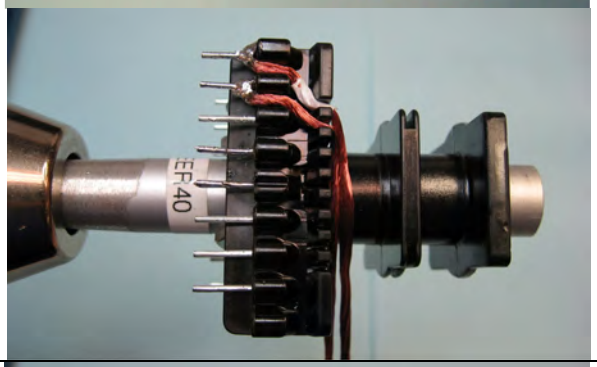
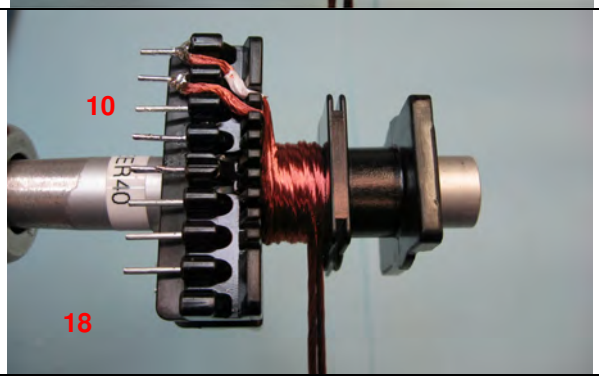


Figure 8 – LLC Transformer Winding Diagram.

7.1.5 Winding Instructions

General note	For the purpose of these instructions, Bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1A and 1B	For WD1A and WD1B use two ~60 cm lengths of Litz wire (item [5]). Mark start and finish of one strand using a tape flag or other means. This strand will be used for WD 1A. Route start and finish leads as shown in illustrations. Start flagged wire strand at pin 10, start unflagged strand at pin 11. Wind 9 simultaneous bifilar turns of Litz wire (item [5]) from left to right, then from right to left, and continue with tight tension about 4 layers. Finish flagged wire at pin12 and unflagged wire at pin 13. Use 2 layers of tape (item [3]) for finish wrap.
WD2	Starting at pin 7, shield start lead where it enters bobbin with 2cm piece of tape (item [3]) at side of bobbin, then wind 39 turns of Litz wire (item [4]) on bobbin from left to right, then from right to left, and continue with tight tension in 6 layers. Use 2 layers of tape (item [3]) for finish wrap. Route start and finish leads as shown in illustrations.
Assembly	Grind core halves for specified primary inductance, insert bobbin, and secure core halves with one turn of copper tape (item [6]) as shown. Make sure that start and finis of copper tape overlap. Solder at overlap, attach wire (item [8]) and connect this wire to pin 2. Use tape (item [7]) to secure core halves and insulate.

7.2 Transformer Illustrations

General note		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is counter-clockwise.
WD1A and 1B:	 	For WD1A and WD1B use two ~60 cm lengths of Litz wire (item [5]). Mark start and finish of one strand using a tape flag or other means. The marked strand will be used for WD 1A. Route start and finish leads as shown in illustrations. Start flagged wire strand at pin 10, start unflagged strand at pin 11.
WD1A and 1B: (Cont'd)		Wind 9 simultaneous bifilar turns of Litz wire (item [5]) from left to right, then from right to left, and continue with tight tension about 4 layers. Finish flagged wire at pin 12 and unflagged wire at pin 13. Use 2 layers of tape (item [3]) for finish wrap.

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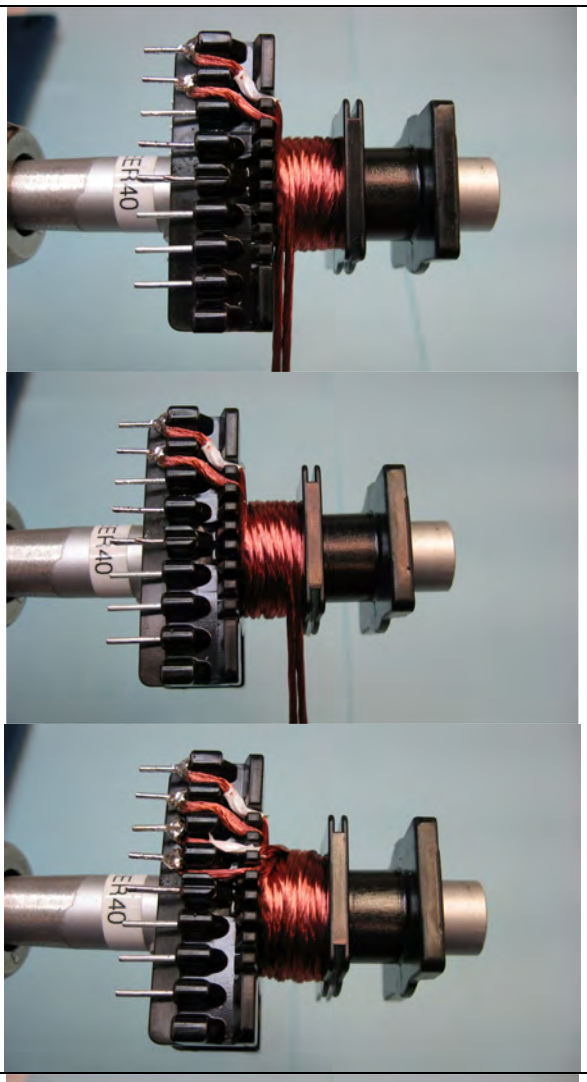
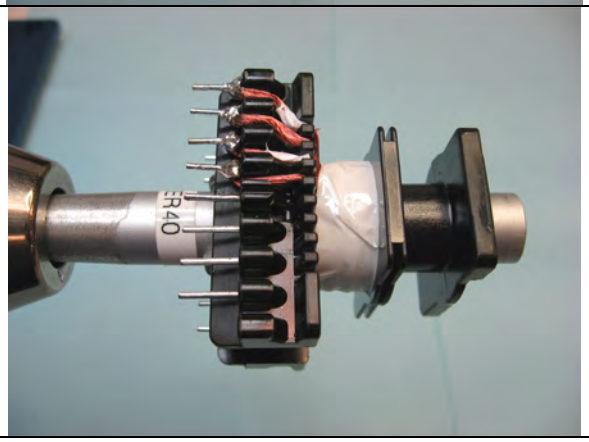
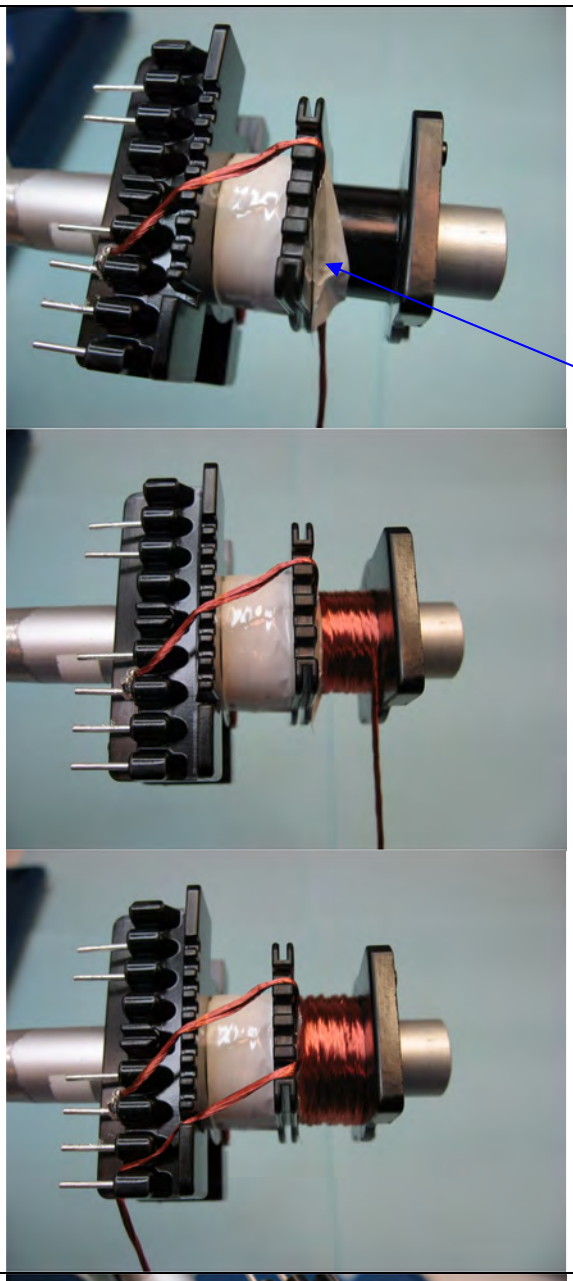
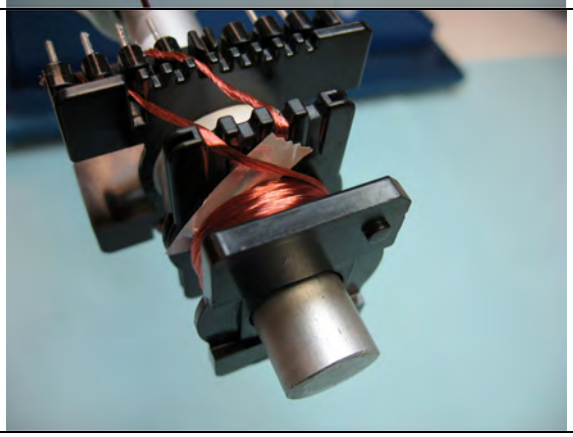
		
		Use 2 layers of tape (item [3]) for finish wrap.

WD2:		Starting at pin 7, shield start lead where it enters bobbin with 2cm piece of tape (item [3]) at side of bobbin, then wind 39 turns of Litz wire (item [4]) on bobbin from left to right, then from right to left, and continuing for 6 layers. Finish at Pin 9. Route start and finish leads as shown in illustration.
WD2: **(Cont'd)**		Use 2 layers of tape (item [3]) for finish wrap. Route start and finish leads as shown in illustrations.

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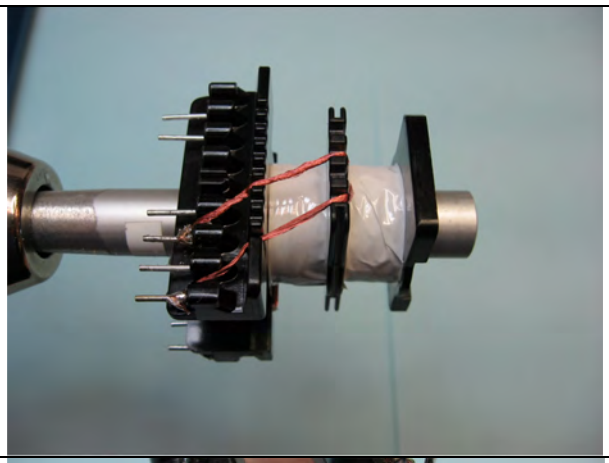
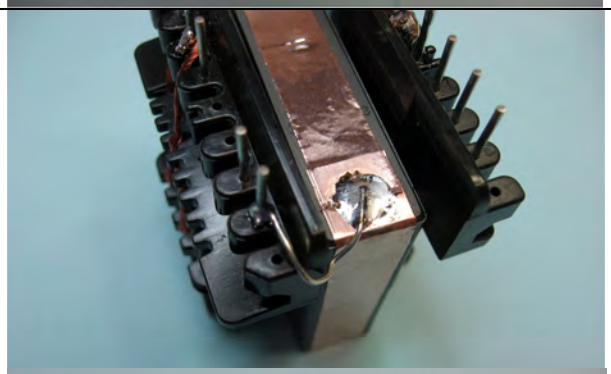
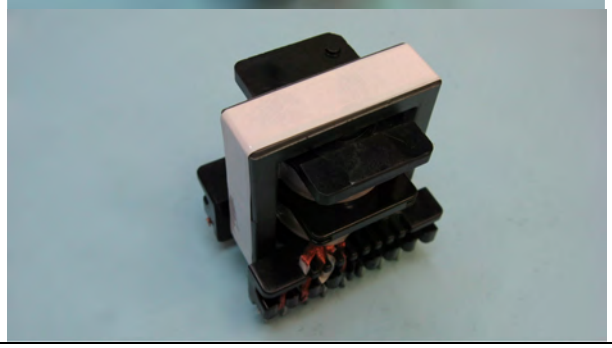
		
Assembly	 	Grind core halves for specified primary inductance, insert bobbin, and secure cores with one turn of copper Tape (item [6]). Overlap start and finish of copper tape. Solder at overlap, attach wire (item [8]) and connect this wire to pin 2. Use tape (item [7]) to secure core halves and insulate.

7.3 PFC Choke (L4) Specification

7.3.1 Electrical Diagram

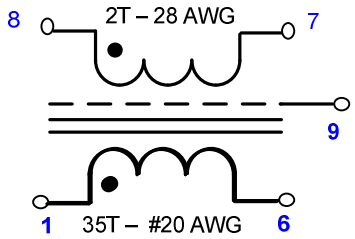


Figure 9 – PFC Choke Schematic.

7.3.2 Electrical Specification

Inductance: Pins 1-6, 100 kHz, 0.4 V - 580 µH ± 10%

7.3.3 Materials

Item	Description
[1]	Ferrite core pair, PQ32/20, TDK PC44PQ32/20Z-12 or equivalent, gap for A_L of 473 nH/T^2.
[2]	Bobbin, PQ32/20, 12 pin, TDK CPH-E41/12-1S-12PD-Z or equivalent.
[3]	Magnet Wire: #20AWG, solderable double coated.
[4]	Magnet Wire: #28AWG, solderable double coated.
[5]	Tape Polyester Film, 3M 1350F-1 or equivalent, 7.5 mm wide.
[6]	Tape Polyester Film, 3M 1350F-1 or equivalent, 10 mm wide.
[7]	Tape, Copper Foil, 3M 1125 or equivalent, 6.5 mm wide.
[8]	Wire, tinned bus, #24 AWG.
[9]	Transformer Varnish, Dolph BC-389 or equivalent (must be baking vs. air-dry varnish).

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7.3.4 Build Diagram

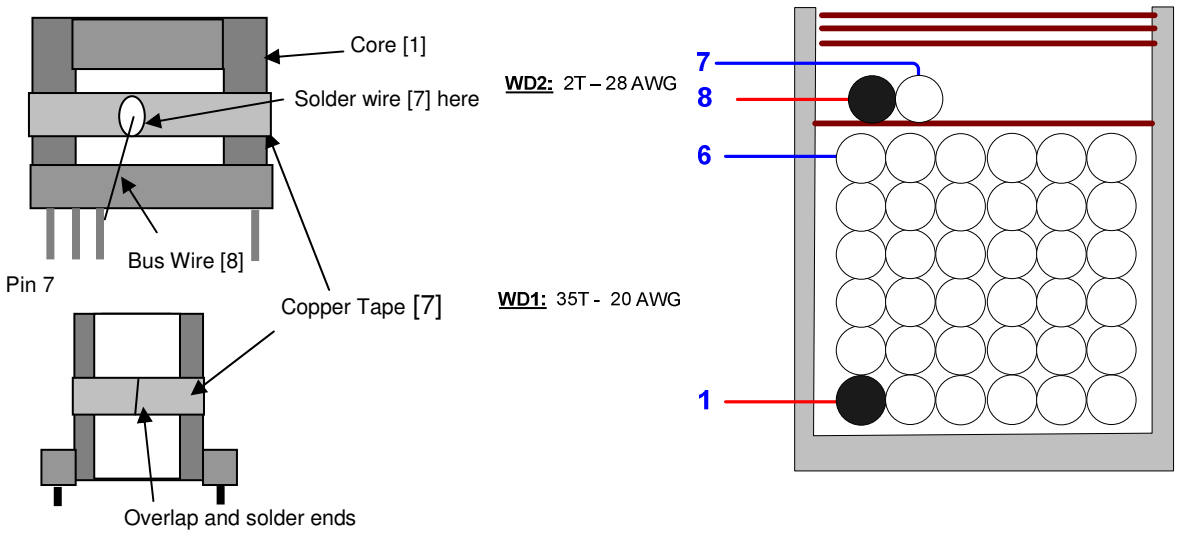

Figure 10 – PFC Choke Build Diagram.

7.3.5 Winding Instructions

Bobbin Preparation	Pull pins 2, 3, 10, and 11 on bobbin [2].
Main Winding	Starting on pin 1, wind 35 turns of wire [3] on bobbin [2]. Finish on pin 6.
Insulation	Use 1 layer of tape [5] for insulation.
Bias Winding	Starting on pin 8, wind 2 turns of wire [4], finishing on pin 7.
Finish Wrap	Use 3 layers of tape [5] for finish wrap.
Core Assembly	Assemble bobbin and core halves. Secure core with two wraps of tape (Item 5).
Shield	Apply 1 turn of copper tape (Item [7]) as shown in Figure 1, centered in bobbin window. Overlap start and finish ends as shown in Figure 1, and solder to form a shorted turn. Take 3 cm of hook-up wire [7], solder 1 end of wire to copper foil as shown in Figure 1. Terminate other end on pin 9 of bobbin.
Shield Insulation	Apply 3 turns of tape (item [6]) to insulate copper shield.
Varnish	Dip varnish finished assembly.

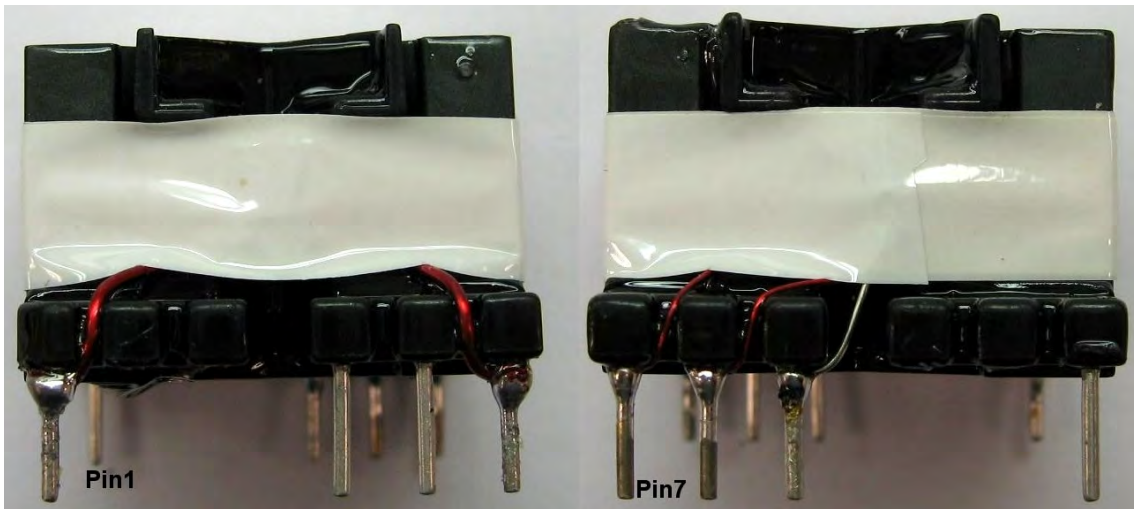

Figure 11 – Finished PFC Choke, Front and Back View.

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8 LLC Transformer Design Spreadsheet

ACDC_PLC810_031209; Rev.1.4; Copyright Power Integrations 2008	INPUTS	INFO	OUTPUTS	UNITS	ACDC_PLC810_031209_Rev1-4.xls; PLC810 Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vacmin			140	V	Minimum AC input voltage
Vacmax			265	V	Maximum AC input voltage
Iacinmax			1.19	A	Maximum input AC rms current at Vacmin
Vbulk			385.00	V	Nominal PFC output voltage
Vbulkmax			411.95	V	Peak PFC OVP voltage (typical is 7% above Vbulk)
Vbulkmin	300.00		300.00	V	Minimum bulk capacitor voltage at the specified holdup time. Typical value is between 250 - 320 VDC. Max holdup time is at 250 V
fL			50.00	Hz	AC Line input frequency
Holdup time	18.00		18.00	ms	Bulk capacitor hold up time
CIN_MIN			98.28	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbulkmin to change bulk cap value
bulk ripple			8.16	V	Bulk capacitor peak to peak voltage (low freq ripple)
Vrippeak			389.08	V	Bulk cap peak value of ripple voltage
IAC			1.19	A	AC input rms current at VACMIN
IAC_PEAK			1.68	A	Peak AC input current at full load and VACMIN
Enter LLC (secondary) outputs					The spreadsheet assumes AC stacking of the secondaries
Vo1	48.00			V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
Io1	3.13			A	Main output maximum current
Vd1	0.90		0.90	V	Forward voltage of diode in main output
Po1			150.24	W	Output Power from first LLC output
Vo2	0.00			V	Second Output Voltage
Io2	0.00			A	Second output current
Vd2	0.00		0.00	V	Forward voltage of diode used in second output
Po2			0.00	W	Output Power from second LLC output
Enter stand-by (auxiliary) outputs					
Vo3	12.00			V	Auxiliary Output 1 Voltage
Io3	0.05			A	Auxiliary Output 1 maximum current
Vo4				V	Auxiliary Output 2 Voltage
Io4				A	Auxiliary Output 2 maximum current
Efficiciency and Loss Allocation					
P_LLC			150.24	W	Specified LLC output power
P_AUX			0.60	W	Auxiliary output power
P_PFC			158.95	W	PFC output power
P_TOTAL			150.84	W	Total output power (Includes Output power from LLC stage and auxiliary stage)
LLC_n_estimated	0.95		0.95		Efficiency of LLC stage
AUX_n_estimated			0.75		Efficiency of auxiliary output
PFC_n_estimated	0.96		0.96		Minimum efficiency of PFC front end stage
PIN			166.44	W	AC input power

Overall efficiency		0.91		Minimum system efficiency
Ploss_PFC		7.49	W	PFC stage power loss
Ploss_LLC		7.91	W	LLC stage power loss
Ploss_AUX		0.20	W	Auxiliary power loss
Ploss_TOTAL		15.60	W	Total power loss
Enter PFC Design Parameters				
f_nominal_desired		100.00	kHz	Desired full load switching frequency. Recommended value 66 kHz to 132 kHz
Krp	0.98	0.98		PFC choke ripple current factor. Actual Krp tends to increase at higher current when using iron powder/Sendust cores, due to drop in inductance at higher current
Diode bridge Vf		0.70	V	Forward voltage drop of diode bridge
Rdson	0.22	0.22	ohms	PFC MOSFET Rdson - use high temp value from datasheet
Coss		18.18	pF	PFC MOSFET high voltage Coss from datasheet
tON		20.00	ns	MOSFET turnon current rise time. Check actual value
Qrr		26.49	nC	Average Qrr of boost diode over AC sinusoid
PFC CHOKE Parameters				
Lpfc		583.79	uH	PFC choke inductance
ILpk		3.33	A	PFC choke peak current at VACMIN
AL	470.00		nH/t^2	nH per turn^2 (from magnetics datasheet). Note - This value decreases by as much as 15% if a belly-band is added to reduce EMI
n		35.24	turns	PFC choke number of turns
MLT	5.00		cm	Mean length per turn
AWG_Choke	20			PFC choke wire gauge
Equivalent Choke Metric Wire gauge		0.80	mm	Equivalent diameter of wire in metric units
Wire length		1.76	m	Length of wire used on PFC choke
Strands	3			Number of wires
DCR		21.21	m-ohms	DC resistance of wire at 25 C
DCR at 85 C		26.72	m-ohms	DC resistance of wire at 85 C
Irms_CHOKE		1.36	A	PFC choke rms current
DCR Cu loss		0.05	W	PFC choke DC Copper loss for reference at 85 C
ACR_PFC_Choke		53.45	m-ohms	Measure or calculate; add 26% to measured value to get 85 C value
HF Irms		0.58	A	RMS current of switching component
HF Cu loss		0.02	W	Copper loss due to switching component at 85 C
tot Cu loss		0.07	W	Total copper loss at 85 C
LM	10.00		cm	Magnetic path length of core used
Hpk		14.74	Oe	Peak MMF in Oersteds, calculated at low line
Hpk_SI		1174	A/m	Peak MMF in A/m, calculated at low line
PFC FET, Diode and Output Parameters				
Isense_R		0.16	ohms	Maximum value of PFC current sense resistor
Sense resistor power dissipation		0.30	W	PFC sense resistor power dissipation at Vacmin
Irms_FET		1.11	A	PFC MOSFET RMS current measured at VACMIN
Conduction loss		0.27	W	PFC MOSFET conduction loss

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Trrloss		0.89	W	PFC MOSFET loss due to diode Trr
Cossloss		0.15	W	MOSFET Coss loss
Crossover loss		0.01	W	MOSFET crossover turnon loss
Total PFC loss		1.17	W	MOSPFC FET total loss
Diode bridge Ploss		1.51	W	Diode bridge estimated loss
PFC Diode RMS current		0.65	A	Approximate PFC Diode RMS current at nominal AC input voltage (VACMIN) (includes 100/120 Hz component)
Bulk capacitor RMS current		0.72	A	Approximate Bulk Capacitor RMS current at nominal AC input voltage (VACMIN) (includes 100/120 Hz component and LLC input current)

LLC TRANSFORMER CALCULATIONS

Po		153.06	W	Output from LLC converter including diode loss
Vo		48.90	V	Output at transformer windings (includes diode drop)
Ae	2.10		cm^2	Transformer core cross-sectional area
Lpar	704.00	704.00	uH	Parallel inductance. (Lpar = Lopen - Lser for integrated transformer; Lpar = Lmag for non-integrated transformer)
Lser	116.00	116.00	uH	Leakage inductance of integrated transformer; Leakage + external inductor for non-integrated transformer
Lopen		820.00	uH	Primary open circuit inductance for integrated transformer
C	18.00	18.00	nF	Series resonant capacitor
fnominal_desired		100.00	kHz	Desired full load switching frequency. Recommended value 66 kHz to 132 kHz
fnominal_actual		87.0	kHz	Expected frequency at nominal input voltage (VBULK) and full load
IRMS_LLC_Primary		0.94	A	Primary winding RMS current at full load and nominal input voltage (VBULK)
IRMS_LLC_Q1		0.67	A	RMS current through upper MOSFET in LLC half bridge
VMIN		295.1	V	Minimum Voltage on Bulk Capacitor at minimum switching frequency
f_AT_VMIN		49.00	kHz	Frequency at minimum Bulk capacitor voltage
fpar		45	kHz	Parallel resonant frequency (defined by Lpar + Lser and C)
fser		110	kHz	Series resonant frequency (defined by series inductance Lser and C)
fmin		55	kHz	Min frequency, at VBULK _MIN and full load. Set PLC810 minimum frequency to this value. Operation below this frequency results in loss of ZVS
NP_1		39		Primary winding number of turns
NS_1	9.00	9		Secondary winding number of turns
n_RATIO	4.30	4.30		Transformer turns ratio. Adjust this value so that fnominal_actual is close to fnominal_desired
Bpkfmin		1186	Gauss	First Quadrant peak flux excursion at minimum frequency.
BAC		1487	Gauss	AC peak to peak flux density (calculated at fnominal_actual, VBULK at full load)
LLC sense resistor	0.22	0.22	ohms	LLC current sense resistor
Pdiss_LLC_senseR		0.20	W	Power dissipation in LLC sense resistor

PRIMARY

Primary gauge	40.00		AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge		0.08	mm	Equivalent diameter of wire in metric units

Primary litz strands	75.00			Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Primary parallel wires	1.00			Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Primary		49.72	m-ohm/m	Resistivity in milli-ohms per meter
Transformer primary MLT	5.00		cm	Mean length per turn
Primary turns		38.70		Number of primary turns
Primary DCR 25 C		96.21	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C		128.92	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current	1.50		A	Measured RMS current through the primary winding
ACR_Trf_Primary		206.27	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss		0.46	W	Total primary winding copper loss at 85 C
Separate Series Inductor (For non-integrated transformer only)				Ignore this section if using integrated magnetics
Lsep		116.00	uH	Desired inductance from separate inductor
Ae_Ind	0.53		cm^2	Inductor core cross-sectional area
Inductor turns	15.00	15		Number of primary turns
BP_fnom		2086	Gauss	AC flux for core loss calculations (at fnom and full load)
BP_fmin		2629	Gauss	Peak flux density, calculated at minimum frequency fmin
Inductor gauge	40.00		AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge		0.08	mm	Equivalent diameter of wire in metric units
Inductor litz strands	125.00			Number of strands used in Litz wire
Inductor parallel wires	1.00			Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind		29.83	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT	7.00		cm	Mean length per turn
Inductor DCR 25 C		31.32	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C		41.97	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor		67.16	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss		0.15	W	Total primary winding copper loss at 85 C
Winding 1 (Vo1)				Note - Power loss calculations are for each winding half of secondary
Sec 1 Wire gauge	40		AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge		0.08	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	175			Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Parallel wires sec 1	1			Number of parallel individual wires to make up Litz wire
Resistivity_25 C_sec1		21.31	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT	5.00		cm	Mean length per turn
Sec 1 Turns		9.00		Secondary winding turns (each half)
DCR_25C_Sec1		9.59	m-ohm	Estimated resistance at 25 C (for reference)
DCR_100C_Sec1		12.85	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Sec 1 RMS current		4.92	A	RMS current through Output 1 winding,

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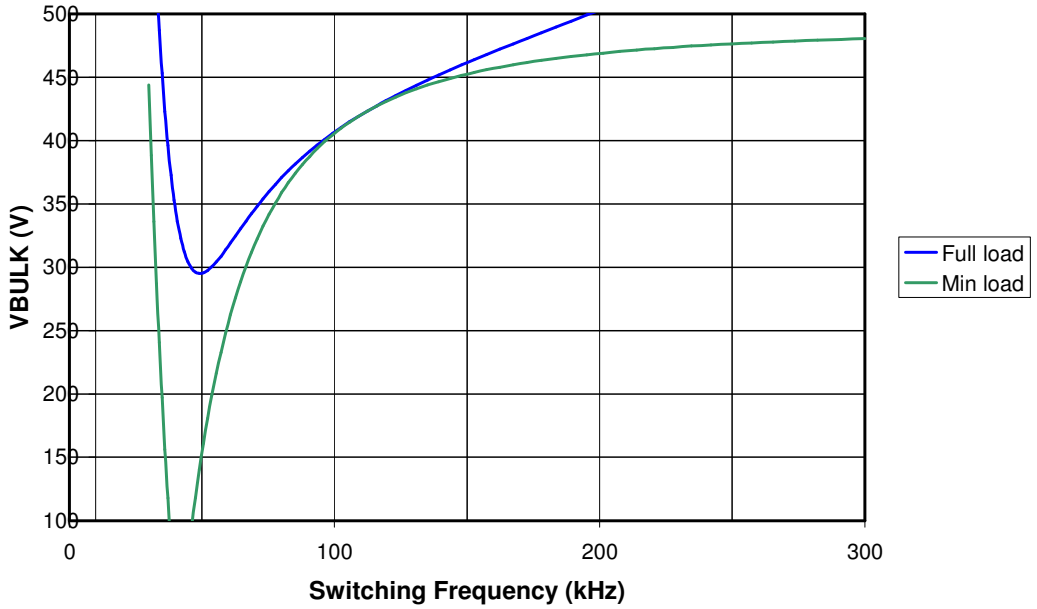
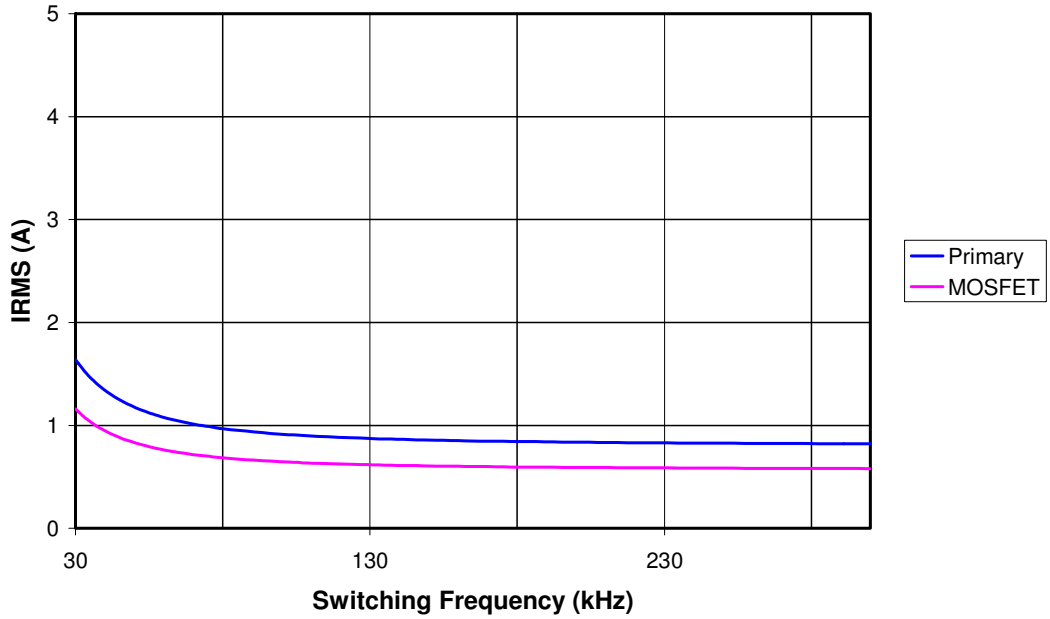
				assuming half sinusoidal waveshape
DCR_Ploss_Sec1		0.25	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec1		20.56	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1		1.00	W	Estimated AC copper loss (both secondary halves)
Total secondary winding Copper Losses		1.25	W	Total (AC + DC) winding copper loss for both secondary halves
Winding 2 (Vo2)				Note - Power loss calculations are for each winding half of secondary
Sec 2 Wire gauge	40		AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge		0.08	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	175			Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Parallel wires sec 2	1			Number of parallel individual wires to make up Litz wire
Resistivity_25 C_sec2		21.31	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary 2 MLT			cm	Mean length per turn
Sec 2 Turns	0.00			Secondary winding turns (each half)
DCR_25C_Sec2		0.00	m-ohm	Estimated resistance at 25 C (for reference)
DCR_100C_Sec2		0.00	m-ohm	Estimated resistance at 100 C for half secondary (approximately 33% higher than at 25 C)
Sec 2 RMS current		4.92	Arms	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
DCR_Ploss_Sec1		0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2		0.00	m-ohm	Actual measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2		0.00	W	Estimated AC copper loss (both secondary halves)
Total secondary winding Copper Losses		0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Total Copper loss calculation				Does not include fringing flux loss from gap
Primary copper loss (from Primary section)		0.46	W	Total primary winding copper loss at 85 C
Secondary copper Loss		1.25	W	Total copper loss in secondary winding
Transformer copper loss		1.71	W	Total copper loss in transformer (primary + secondary)
TURNS CALCULATOR				This is to help you choose the secondary turns - not connected to any other part of spreadsheet
V1		48.00	V	Target Output Voltage Vo1
V1d1		0.90	V	Diode drop voltage for Vo1
N1	4.00			Total number of turns for Vo1
V2			V	Expected outputV
V2d2			V	Diode drop voltage for Vo2
N2	2.00			Total number of turns for Vo2

Compared to the above spreadsheet, actual operating frequency is considerably higher than the expected operating frequency of 90 kHz shown. This is due to the effective turns ratio of the transformer, which results in an operating turns ratio lower than the ratio of primary turns to secondary turns (N_P/N_S). The graphs shown below were generated by adjusting the turns ratio in the spreadsheet until the expected operating frequency shown in the spreadsheet was identical to the actual operating frequency of the unit under test.

VBULK vs Switching Frequency



Full Load Primary and MOSFET RMS Currents



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9 Performance Data

All measurements were taken at room temperature and 60 Hz input frequency unless otherwise specified, Output voltage measurements were taken at the output connectors.

9.1 LLC Stage Efficiency

To make this measurement, the LLC stage was powered separately by connecting an external 385 VDC supply across bulk capacitor C9, and a 15 V source was applied between the collector of regulator transistor Q27 and controller ground.

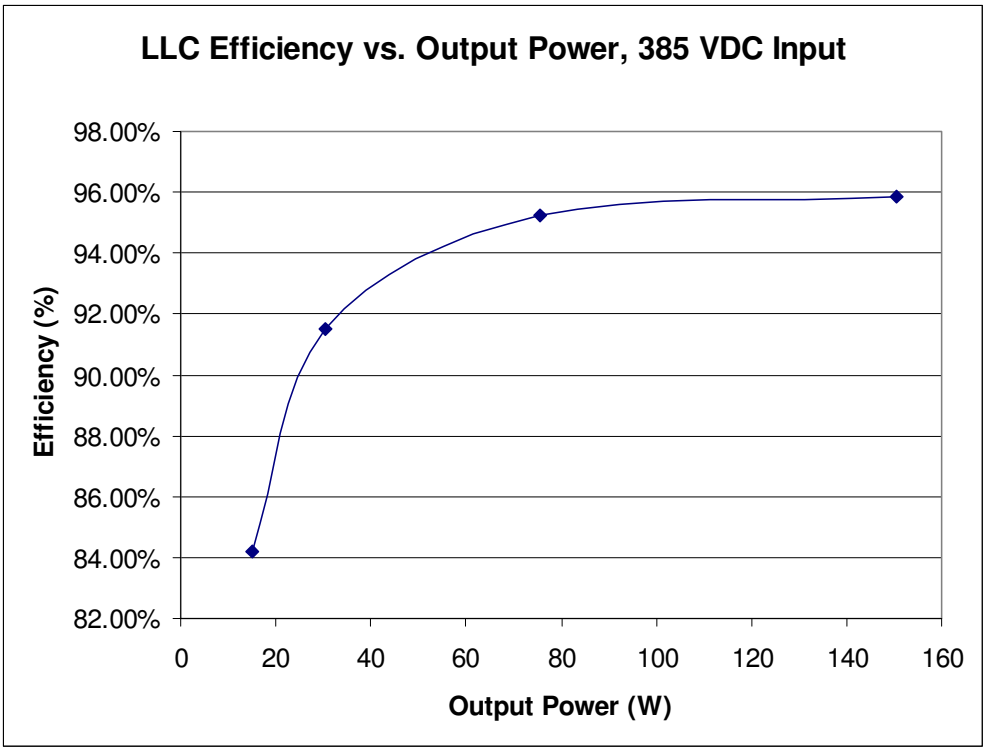

Figure 12 – LLC Stage Efficiency vs. Load, 385 VDC Input.

9.2 Total Efficiency

Figures below show the total supply efficiency (PFC and LLC stages). AC input was supplied using a 60 Hz sine wave source.

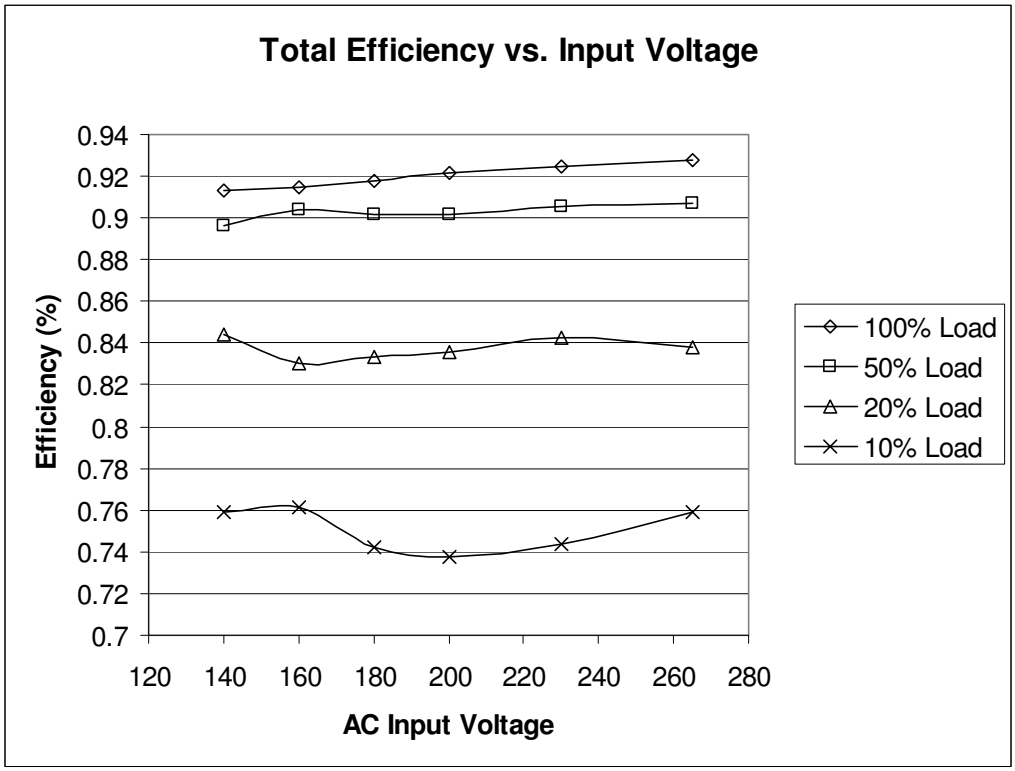

Figure 13 – Total Efficiency vs. Output Power.

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9.3 THD and Power Factor

THD and Power factor measurements were made using a 60 Hz sine wave AC source.

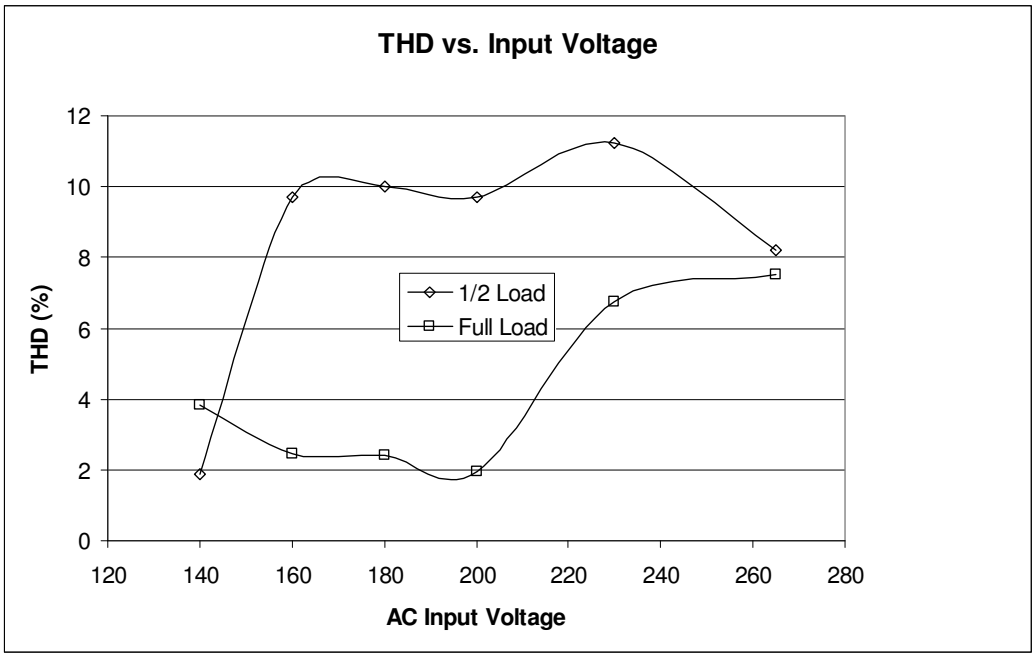

Figure 14 – Input Current THD vs. Input Voltage, 50% and 100% Load.

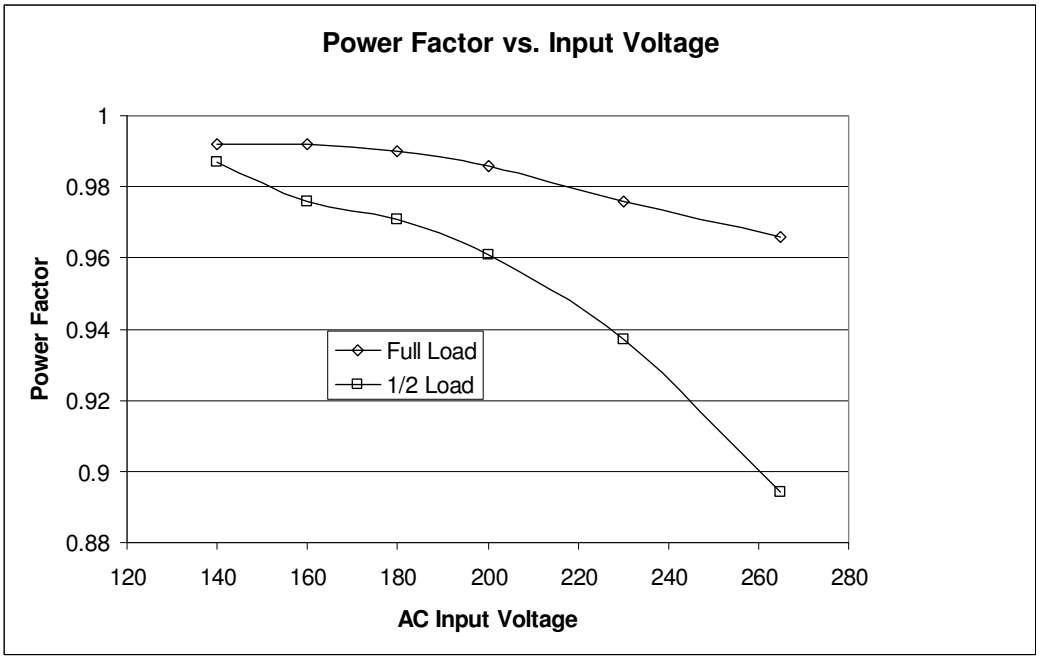

Figure 15 – Power Factor vs. Input Voltage, 50% and 100% Load.

9.4 Output Regulation

The PFC regulates the LLC and standby supply input voltage under normal conditions so the outputs will not be affected by the AC input voltage. Variations due to temperature and component tolerances are not represented. The 48 V output varies by less than 1% over a load range of 2% to 100% load.

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10 Waveforms

All waveforms are measured at room temperature using a 60 Hz sine wave supply unless otherwise indicated.

10.1 Input Voltage and Current

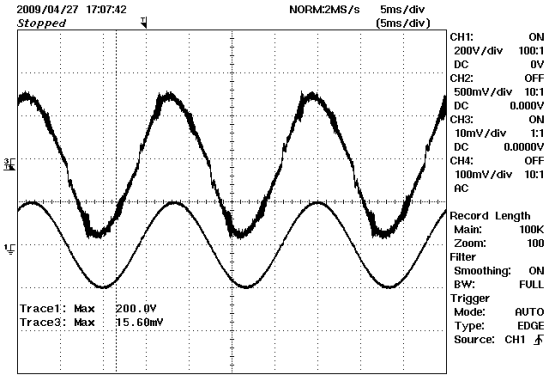

Figure 16 – 140 VAC, 150 W Load.
Top Trace: Input Current, 1 A / div.
Bottom trace: Input Voltage, 200 V, 5 ms / div.

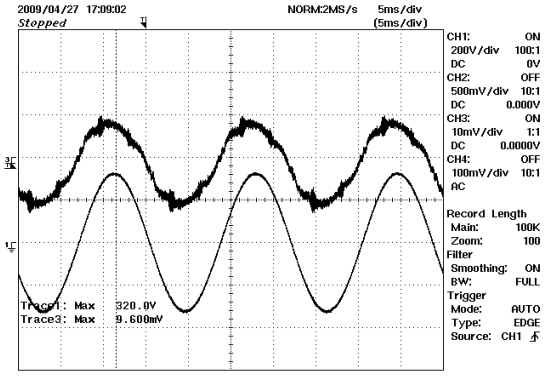

Figure 17 – 230 VAC, 150 W Load.
Top Trace: Input Current, 1 A / div.
Bottom trace: Input Voltage, 200 V, 5 ms / div.

10.2 LLC Primary Voltage and Current

The LLC stage current was measured by cutting the PC board trace in series with the T1 primary and adding a current sensing loop that measures the LLC transformer (T1) primary current. The primary voltage waveform was measured at the hot side of ferrite bead L6.

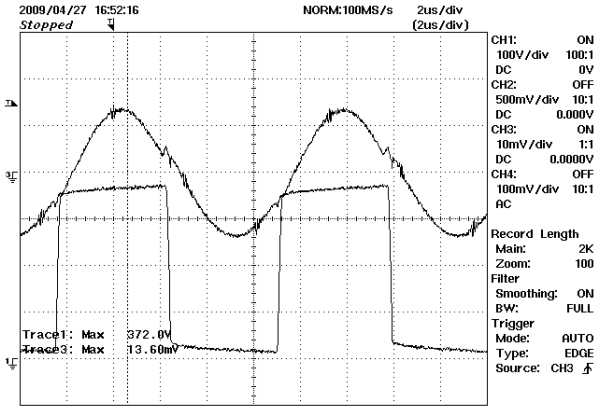

Figure 18 – LLC Stage Primary Voltage and Current.
Top Trace: Current, 1 A / div.
Bottom Trace: Voltage, 100 V, 2 µs / div.

10.3 PFC Switch Voltage and Current - Normal Operation

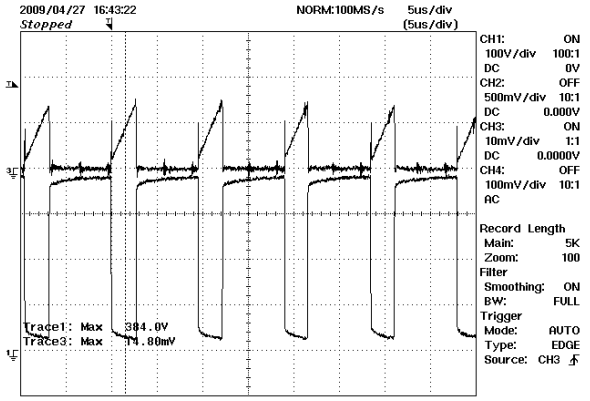

Figure 19 – 140 VAC Input, 100% Load.
Top Trace: Q2 Drain Current, 1 A / div, 5 µs / div
Bottom Trace: Drain Voltage, 100 V, 5 µs/div.

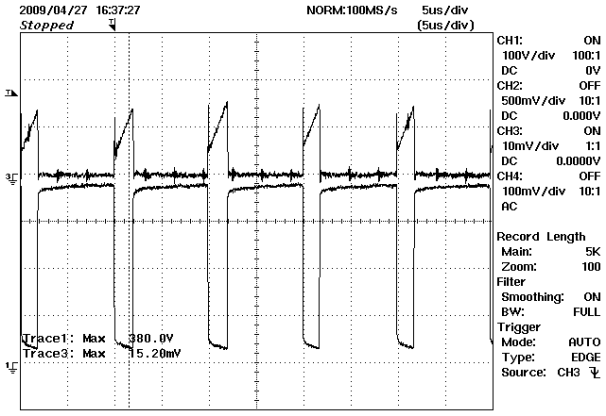

Figure 20 – 230 VAC Input, 100% Load.
Top Trace: Q2 Drain Current, 1 A / div, 5 µs / div
Bottom Trace: Drain Voltage, 100 V, 5 µs / div.

10.4 AC Input Current and PFC Output Voltage During Start-up

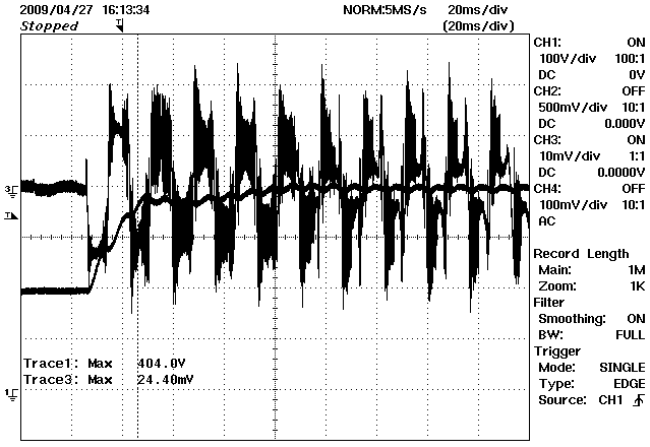

Figure 21 – Full Load, 140 VAC.
Top Trace: AC Input Current, 2 A / div.
Bottom Trace: PFC Voltage, 100 V, 20 ms / div.

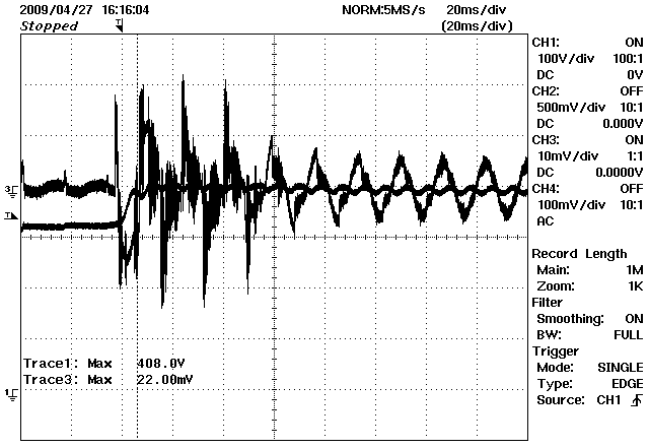

Figure 22 – Full Load, 230 VAC.
Top Trace: AC Input Current, 2 A / div.
Bottom Trace: PFC Voltage, 100 V, 20 ms / div.

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10.5 LLC Start-up

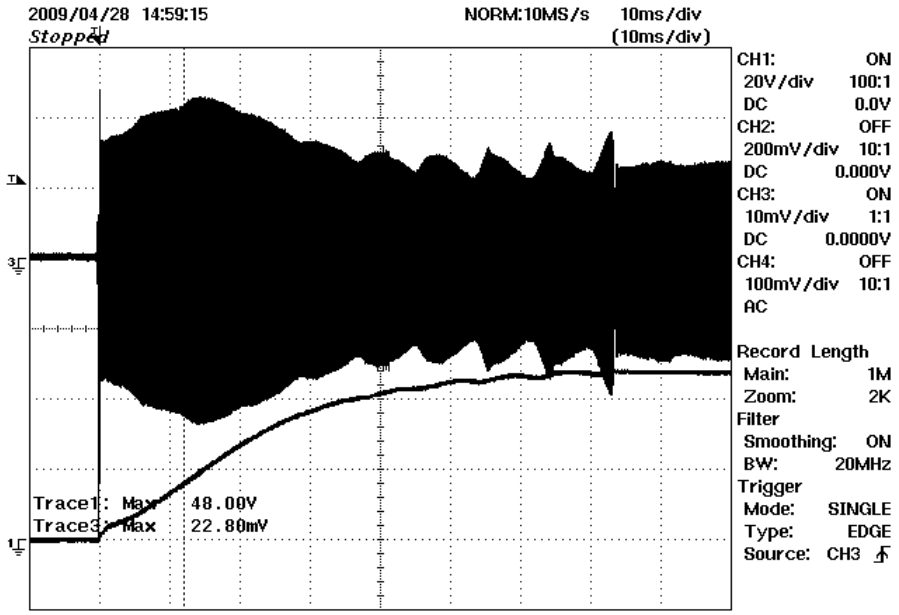

Figure 23 – LLC Start-up. 230 VAC, 100% Load.
Top Trace: LLC Primary Current, 1 A / div.
Bottom Trace: Output Voltage, 20 V, 10 ms / div.

10.6 LLC Output Short Circuit

The figure below shows the effect of an output short circuit on the LLC primary current. A mercury displacement relay was used to short the output to get a fast, bounce-free connection.

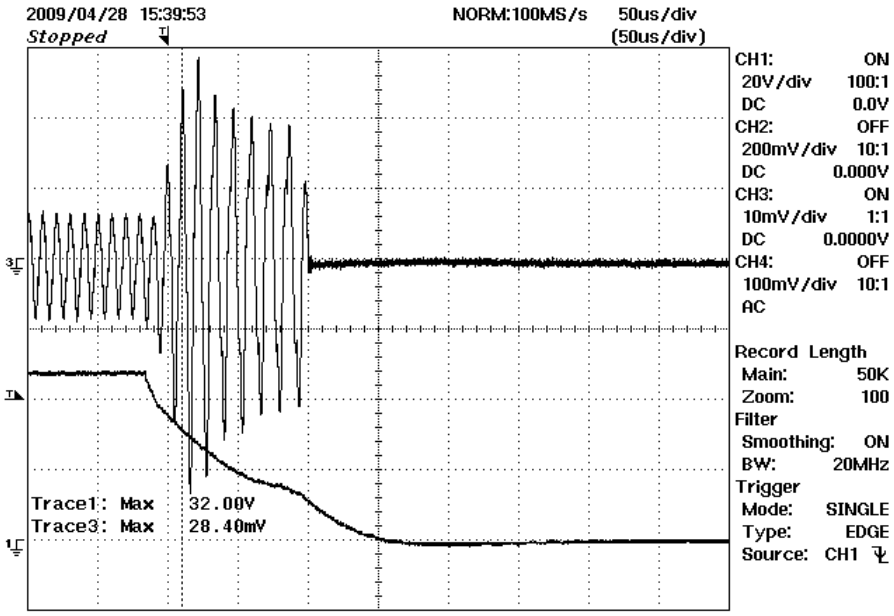

Figure 24 – Output Short Circuit Test, 230 VAC.
Top Trace: LLC Primary Current, 2 A / div.
Bottom Trace: 48 V Output, 20 V, 50 µs / div.

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10.7 Output Voltage During Start-up

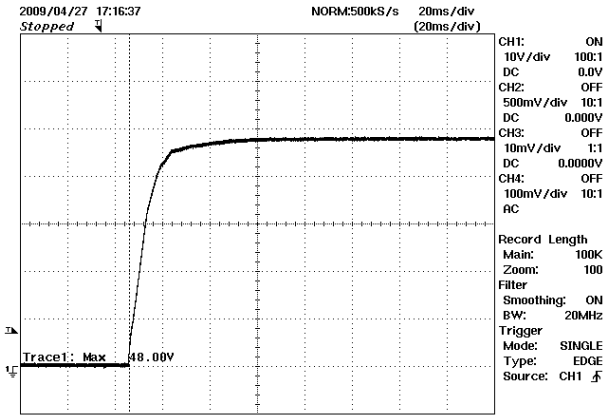

Figure 25 – 48 V Output at Start-up.
140 VAC Input, Full Load. 10 V, 20 ms/ div.

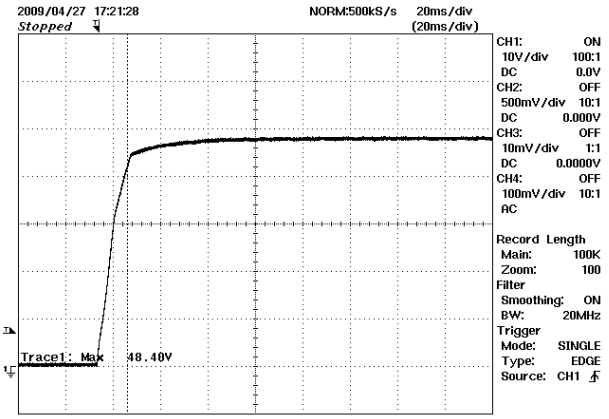

Figure 26 – 48 V Output at Start-up.
230 VAC Input, Full Load. 10 V, 20 ms / div.

10.8 Output Ripple Measurements

10.8.1 Ripple Measurement Technique

For DC output ripple measurements, use a modified oscilloscope test probe to reduce spurious signals. Details of the probe modification are provided in figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 µF / 50 V ceramic capacitor and 1.0 µF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

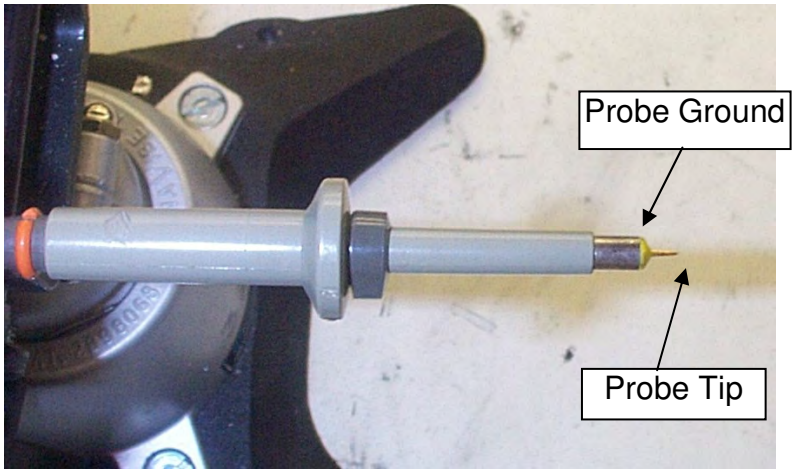

Figure 27 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

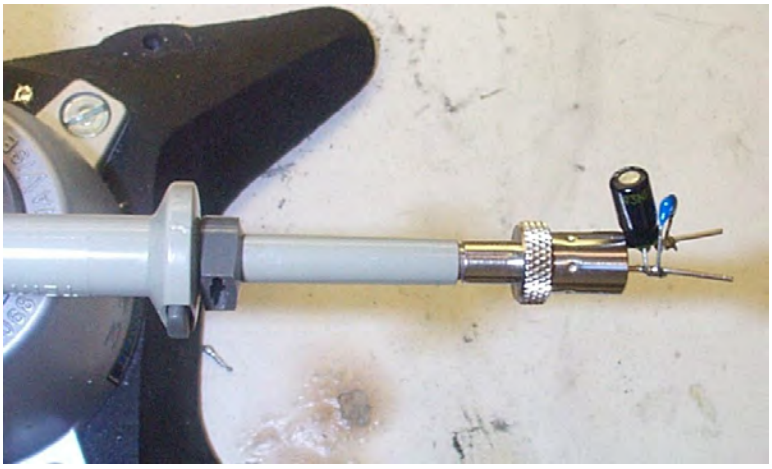

Figure 28 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

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10.8.2 Full Load Output Ripple Results

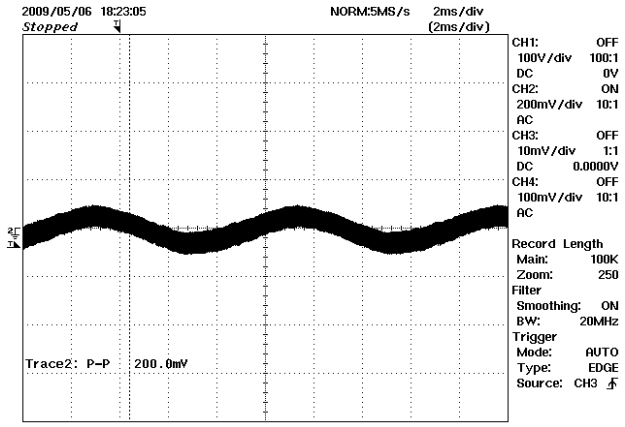

Figure 29 – 48 V Output Ripple, 200 mV, 2 ms / div.

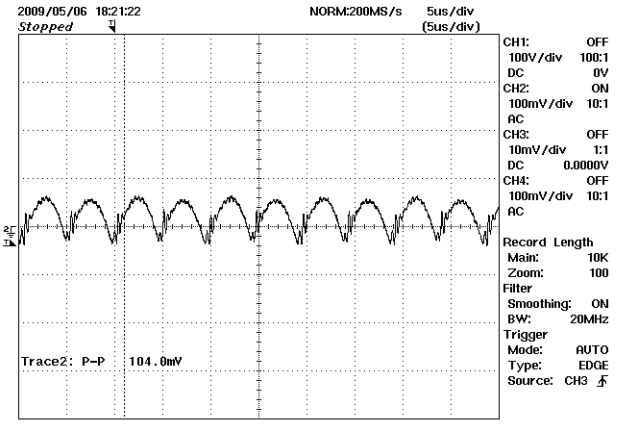

Figure 30 – 48 V Output Ripple, 100 mV, 5 µs / div.

10.8.3 Output Load Step Response

The figures below show transient response with a 75%-100%-75% load step for the 48 V output. The oscilloscope was triggered using the rising edge of the load step, and averaging was used to cancel out ripple components asynchronous to the load step in order to better ascertain the load step response.

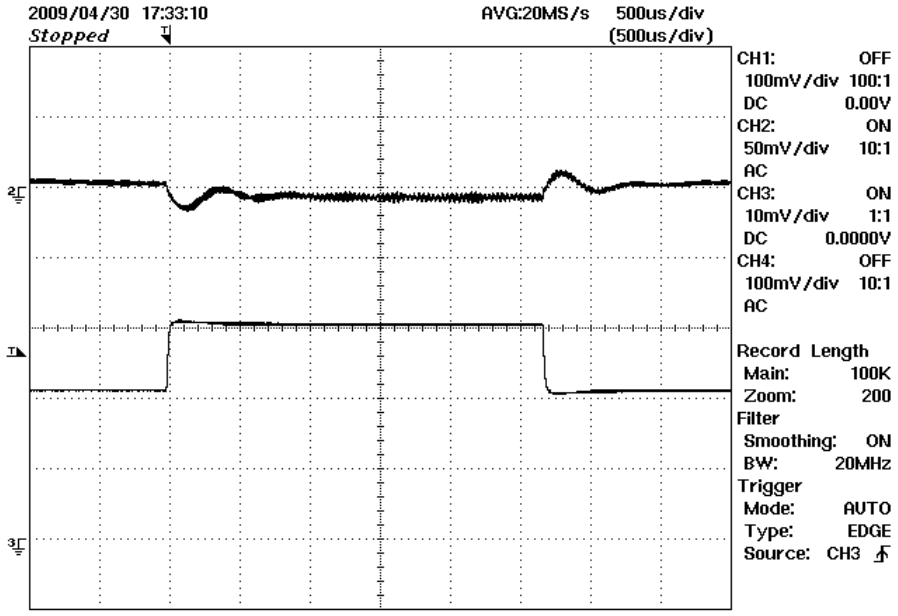

Figure 31 – Output Transient Response 3.13 A – 2.3 A – 3.13 A Load Step.
Top Trace: 48 V Transient Response, 50 mV / div.
Bottom Trace: Output Load Step, 1 A, 500 µs / div.

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11 Temperature Profiles

The board was operated at room temperature in a vertical orientation as shown below. For each test condition the unit was allowed to thermally stabilize (>1 hr) before measurements were made. Infrared measurements were correlated to thermocouples attached using copper tape.

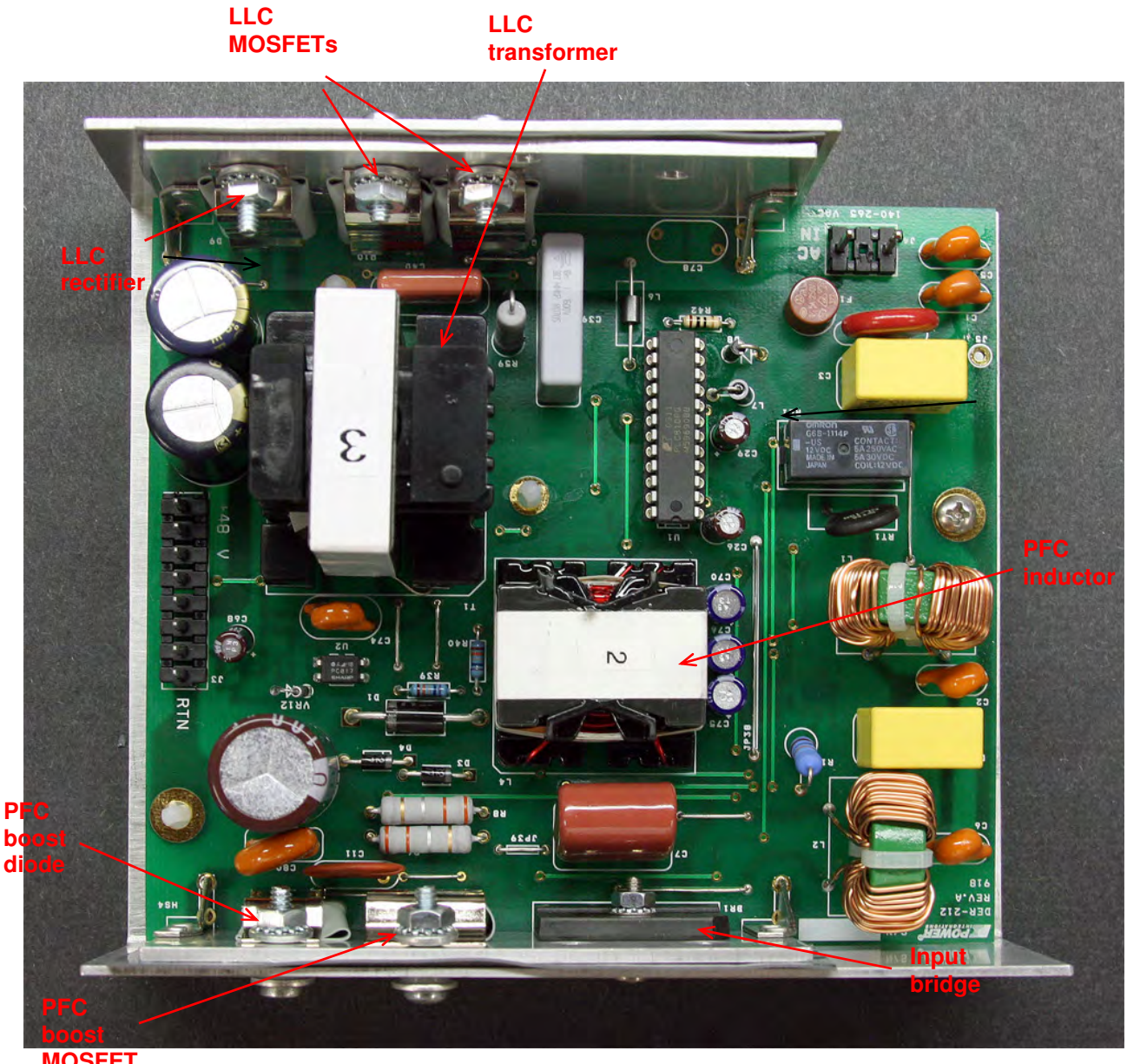

Figure 32 – Photograph of Board Orientation Used for Thermal Testing.

11.1 Thermal Results Summary

11.1.1 Testing Conditions

The goal of this design is to maintain the temperature of components below 100 °C at rated ambient and 100% load (150 W), low line (140 VAC, 60 Hz).

By extrapolating the data below from 21 °C to 60 °C this design meets these requirements.

Measurement data is presented below. The unit was allowed to thermally stabilize (>1 hours in all cases) before gathering data. Semiconductor plastic and magnetics temperatures were correlated via thermocouples attached with copper tape.

	140 VAC, 60 Hz	**230 VAC, 60 Hz**
Output Power (W)	150.2	150.2
Input Power (W)	164.5	162.6
Efficiency (%)	91.3	92.37
Output Loading 48 V (A)	3.13	3.13
Temperatures (°C)		
Ambient	21	21
LLC rectifier plastic package (D9)	47	48
LLC Upper MOSFET (Q10) plastic package	42	43
LLC Lower MOSFET (Q11) plastic package	44	45
PFC diode plastic package (D2)	44	41
PFC MOSFET plastic package (Q2)	42	39
Bridge rectifier plastic package (BR1)	49	43
LLC transformer (T2) surface	47	49
PFC inductor (L4) surface	40	43

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11.2 140 VAC, 60 Hz, 150 W_{OUT}

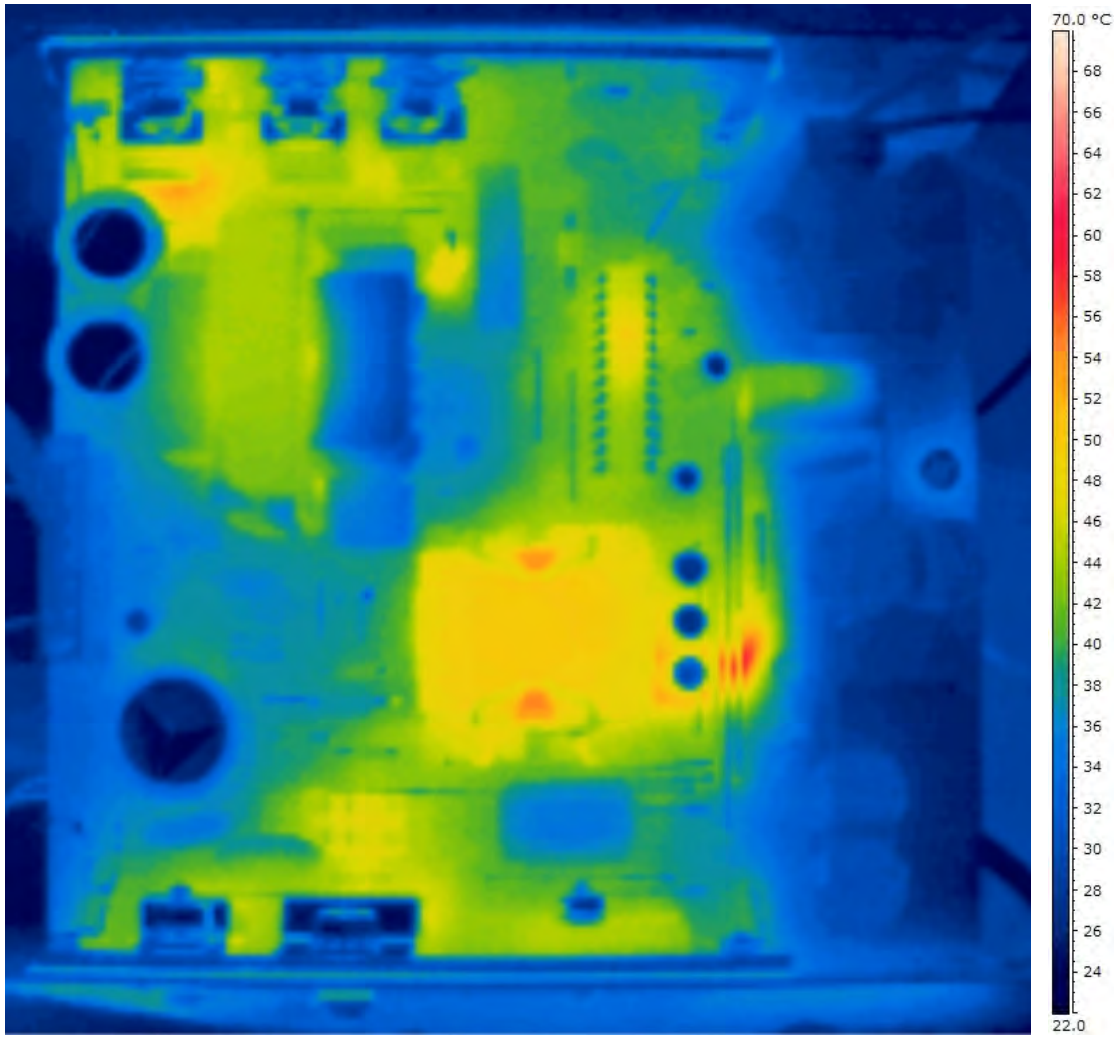

Figure 33 – Thermal Profile. Room Temperature, 140 VAC, 60 Hz, 150 W Load (1 hr)

11.3 230 VAC, 60 Hz, 150 W_{OUT}

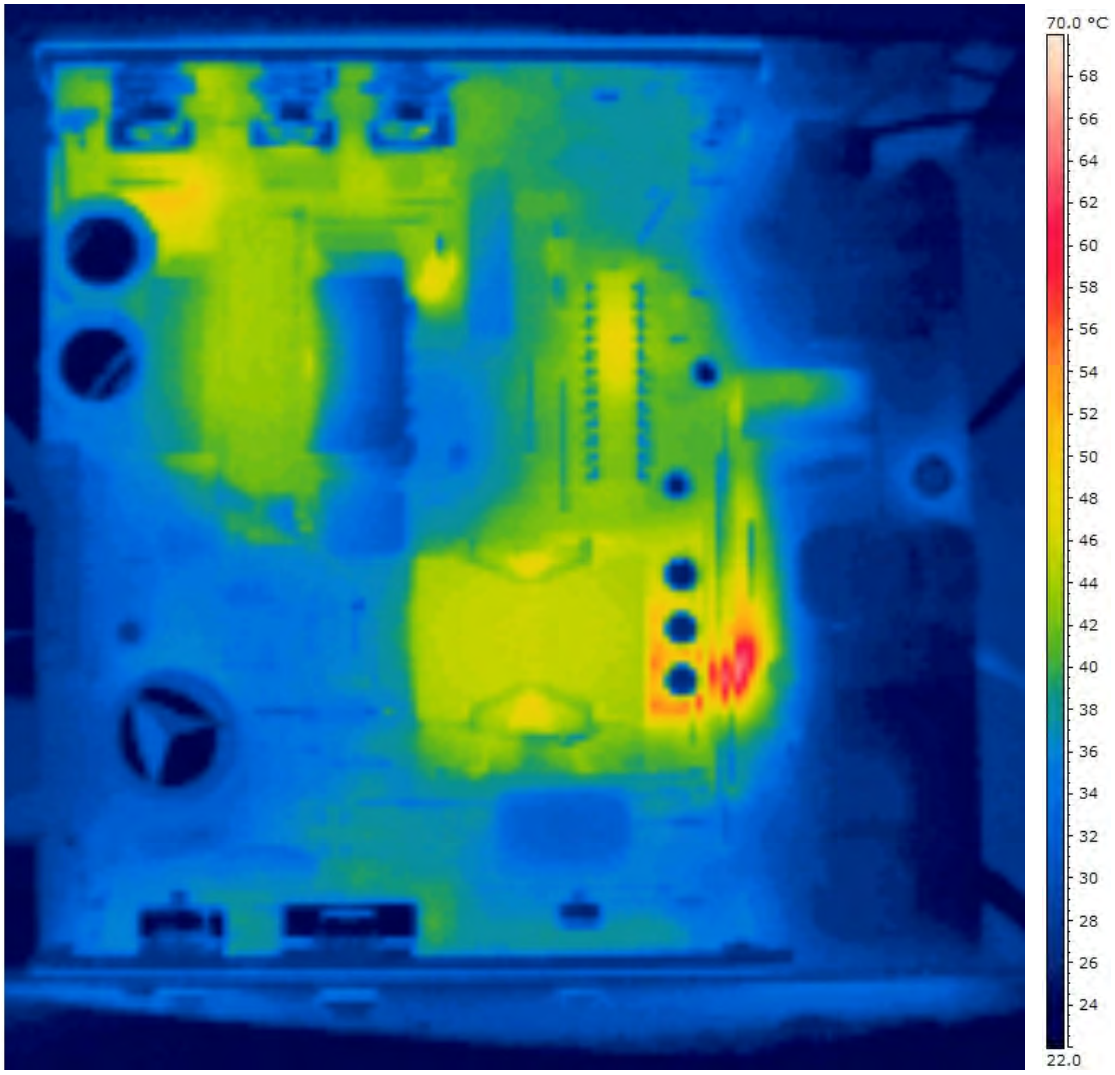

Figure 34 – Thermal Profile. Room Temperature, 230 VAC, 60 Hz, 150 W Load (1 hr)

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12 LLC Gain-Phase

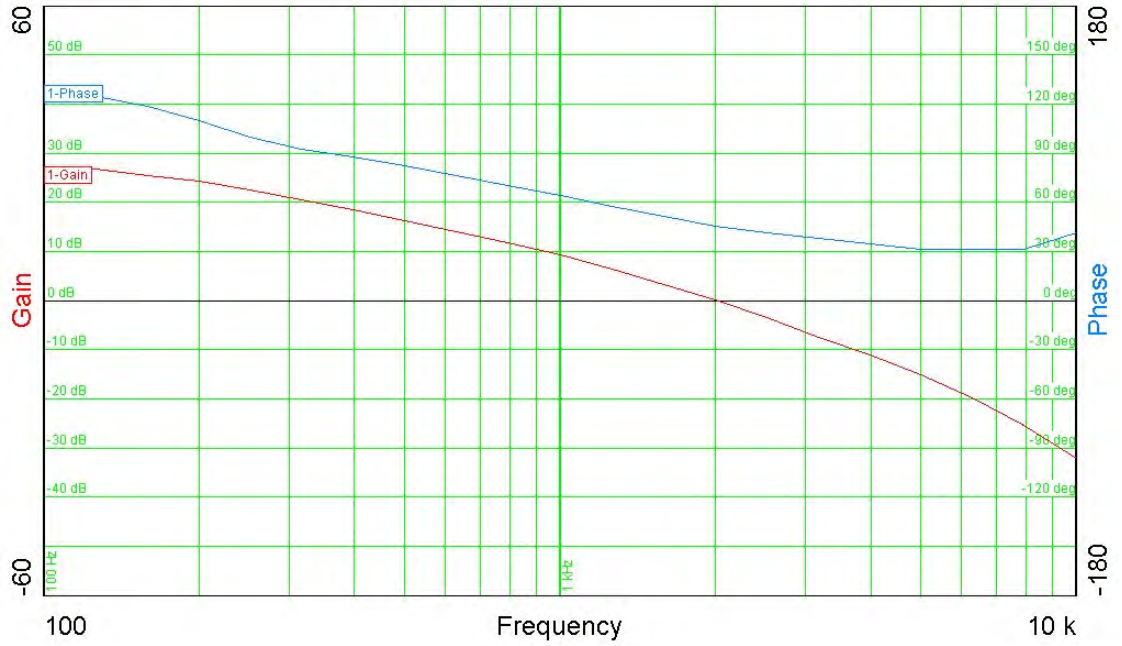

Figure 35 – LLC Converter Gain-Phase, 100% Load Crossover Frequency – 2 kHz, Phase Margin - 45°.

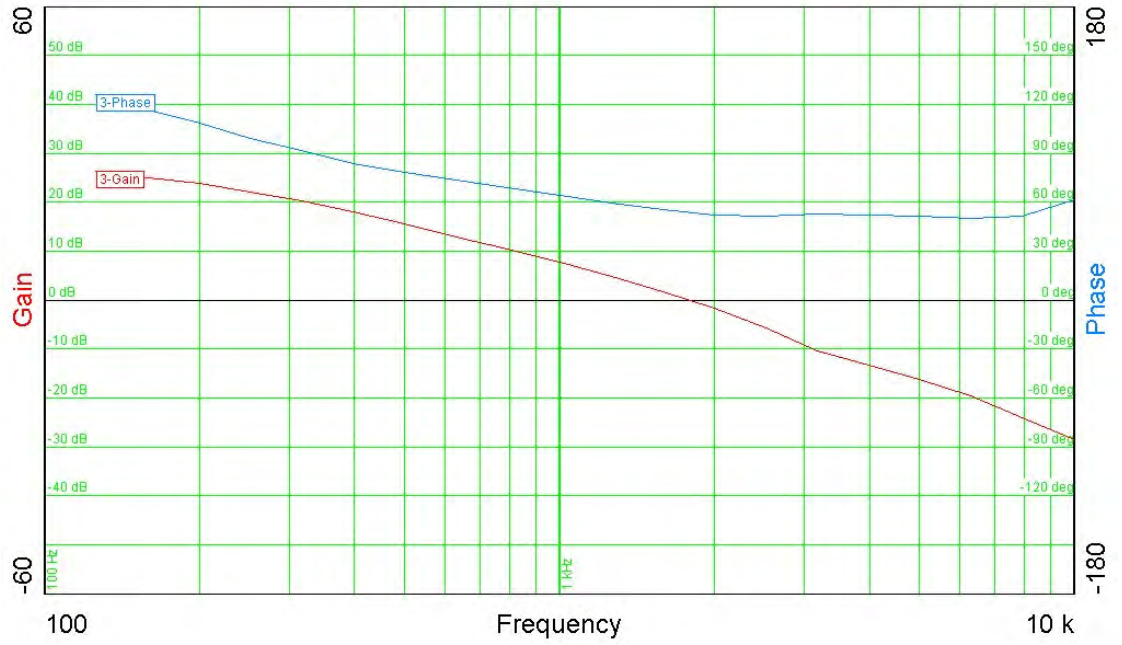

Figure 36 – LLC Converter Gain-Phase, 50% Load. Crossover Frequency ~1.8 kHz, Phase Margin - ~55°.

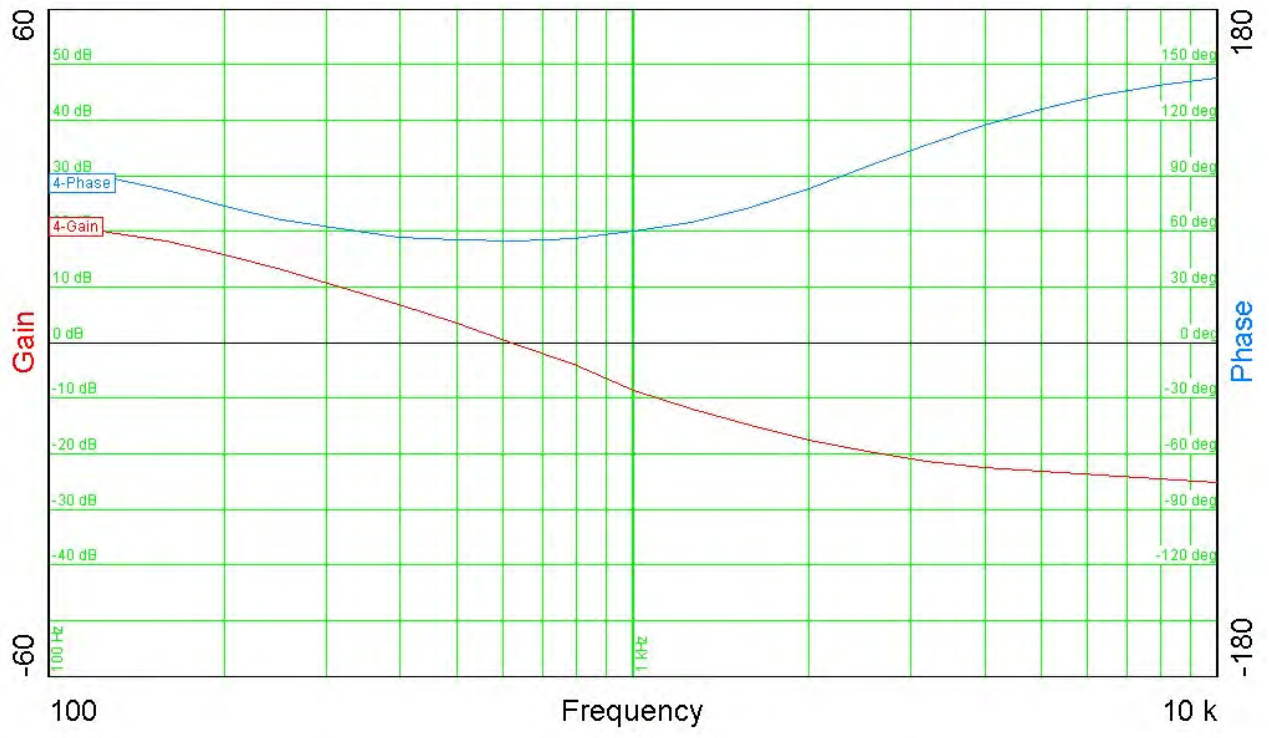

Figure 37 – LLC Converter Gain-Phase, 10% Load. Gain Crossover – 600 Hz, Phase Margin - ~55°.

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13 Conducted EMI

Conducted EMI tests were performed with a 16 Ω resistive load on the 48 V main output. The unit was placed on a metallic ground plane, which in turn was hard wired to the AC cord ground. The resistive load was connected to the ground plane with a pair of 2.2 nF capacitors (one at the positive feed, and one at the return) to simulate the capacitive coupling of LED modules to a grounded street light casing. The peak shown at `90 MHz is actually 10 dB lower than shown in the graph, as the EMI receiver changes scale at 80 MHz.

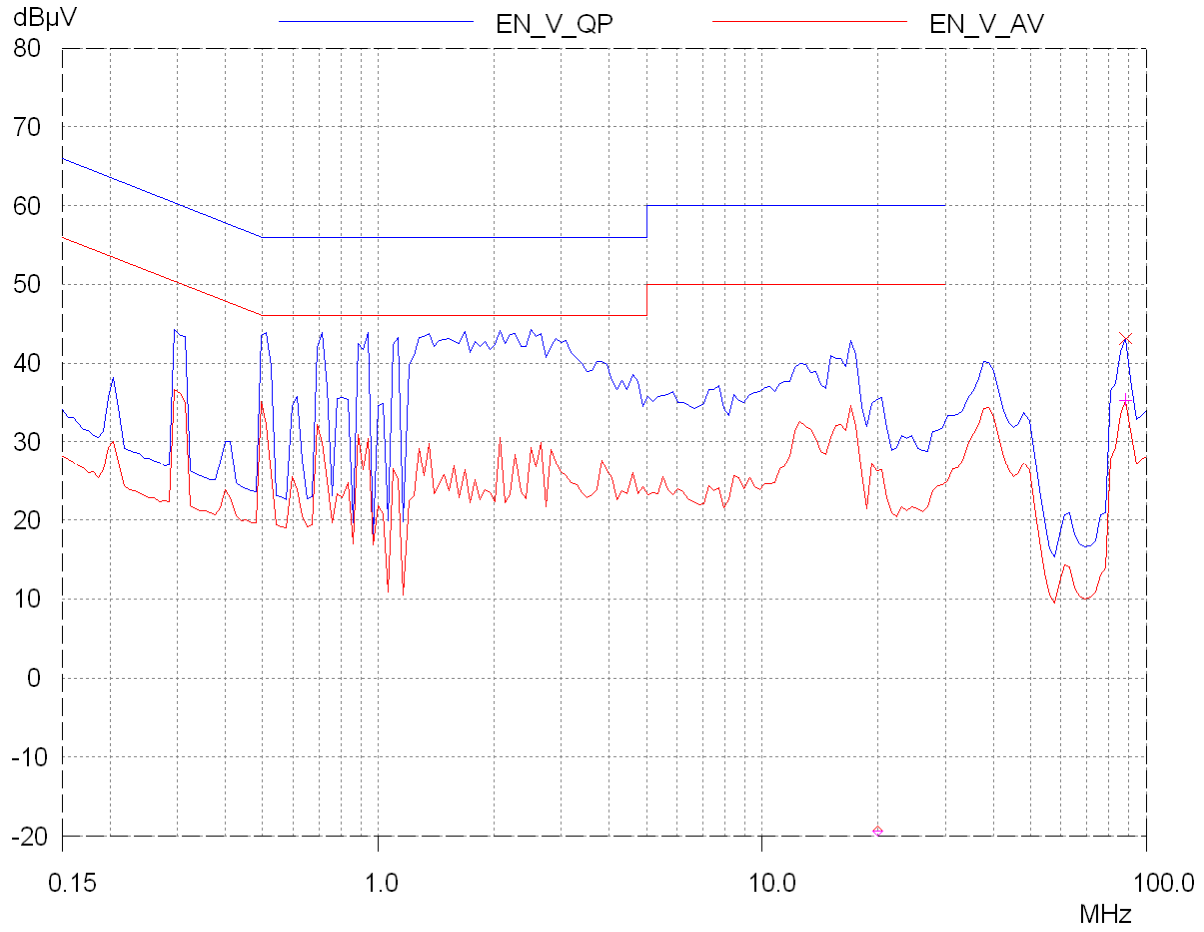

Figure 38 – Conducted EMI, 230 VAC.

14 Line Surge

Differential input line 1.2/50 µs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event. During testing no output interruption was seen.

Surge Level (kV)	Generator Impedance (Ω)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+1 kV	2	230	L to N	90	Pass
-1 kV	2	230	L to N	270	Pass
+2 kV	12	230	L, N to G	90	Pass
-2 kV	12	230	L, N to G	270	Pass

Notes: 1) A ground plane was placed under the PSU bracket and load resistors (load resistors are aluminum case units mounted on heat sinks). The resistive load was bypassed to the ground plane with (2) 2.2 nF capacitors (one at the +48 V input lead, one at return) to simulate the capacitance of LED arrays to a grounded street light case, but otherwise feft floating. The input AC safety ground wire was connected to the ground plane.

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15 Revision History

Date	Author	Revision	Description and changes	Reviewed
11-May-09	RH	1.0	Initial Release	
01-Jun-09		1.1	Revised PCB Images	

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