National Semiconductor

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# MM54HC113/MM74HC113
# Dual J-K Flip-Flops with Preset

## General Description

These high speed J-K Flip-Flops utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ inputs. PRESET is independent of the clock and accomplished by a low level on the input.

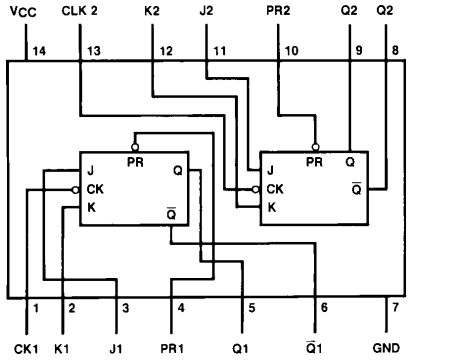
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 $\mu$A maximum
- Low quiescent current: 40 $\mu$A (74HC Series)
- High output drive: 10 LS-TTL loads

## Connection Diagram and Truth Table

**Dual-In-Line Package**

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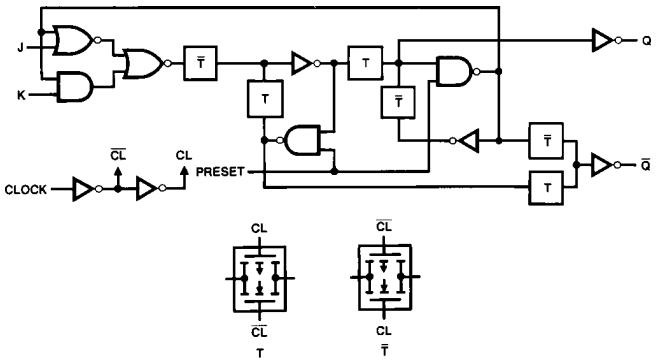
**Top View**

**Order Number MM54HC113 or MM74HC113**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLK | J | K | O | $\overline{Q}$ |
| L | X | X | X | H | L |
| H | ↓ | L | L | Q0 | $\overline{Q}$0 |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | Q0 | $\overline{Q}$0 |

## Logic Diagram

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**(1 of 2)**

RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±25 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temp. ($T_L$) (Soldering 10 seconds) | 260°C |

## Operating Conditions

| | | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | | 0 | $V_{CC}$ | V |
| Operating Temp. Range ($T_A$) | | | | |
| MM74HC | | −40 | +85 | °C |
| MM54HC | | −55 | +125 | °C |
| Input Rise or Fall Times ($t_r$, $t_f$) | $V_{CC}$ = 2.0V | | 1000 | ns |
| | $V_{CC}$ = 4.5V | | 500 | ns |
| | $V_{CC}$ = 6.0V | | 400 | ns |

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | 74HC $T_A$ = −40 to 85°C | 54HC $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum High Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\|I_{OUT}\| \le 20\ \mu A$ | 2.0V | 2.0 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\|I_{OUT}\| \le 4.0$ mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 | V |
| | | $\|I_{OUT}\| \le 5.2$ mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 | V |
| $V_{OL}$ | Maximum Low Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\|I_{OUT}\| \le 20\ \mu A$ | 2.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $\|I_{OUT}\| \le 4.0$ mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| | | $\|I_{OUT}\| \le 5.2$ mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 | V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0 μA | 6.0V | | 4.0 | 40 | 80 | μA |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**$V_{IL}$ limits are currently tested at 20% of $V_{CC}$. The above $V_{IL}$ specification (30% of $V_{CC}$) will be implemented no later than Q1, CY'89.

## AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | | 50 | 30 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ | | 16 | 21 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Preset to Q or $\overline{Q}$ | | 23 | 28 | ns |
| $t_{REM}$ | Minimum Removal Time, Preset to Clock | | 10 | 20 | ns |
| $t_s$ | Minimum Setup Time, J or K to Clock | | 14 | 20 | ns |
| $t_H$ | Minimum Hold Time, J or K from Clock | | −3 | 0 | ns |
| $t_W$ | Minimum Pulse Width, Preset, Clear or Clock | | 10 | 16 | ns |

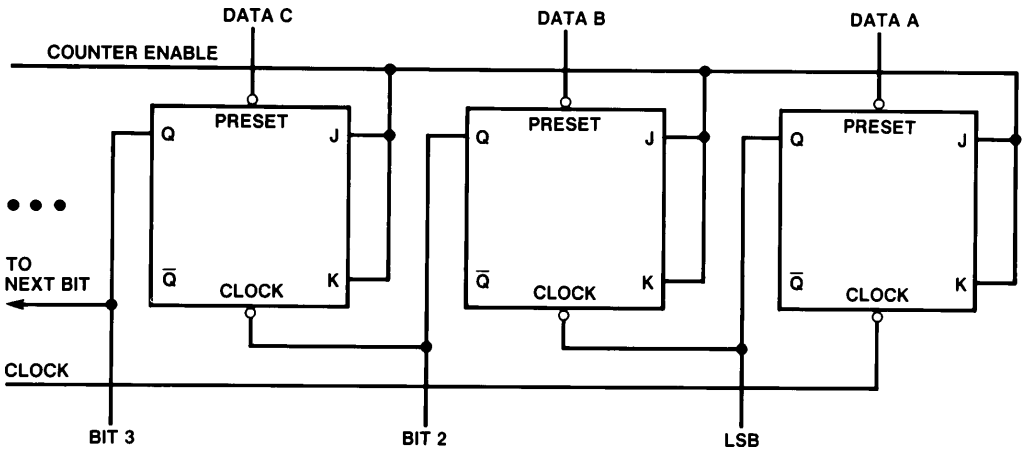
## AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A=25°C$ | 74HC $T_A=-40$ to 85°C | 54HC $T_A=-55$ to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $f_{MAX}$ | Maximum Operating Frequency | | 2.0V | 9 | 5 | 4 | 3 | MHz |
| | | | 4.5V | 45 | 27 | 21 | 18 | MHz |
| | | | 6.0V | 53 | 31 | 24 | 20 | MHz |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ | | 2.0V | 100 | 125 | 160 | 183 | ns |
| | | | 4.5V | 20 | 25 | 32 | 37 | ns |
| | | | 6.0V | 17 | 33 | 27 | 32 | ns |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay, Preset to Q or $\overline{Q}$ | | 2.0V | 137 | 165 | 206 | 239 | ns |
| | | | 4.5V | 27 | 33 | 41 | 47 | ns |
| | | | 6.0V | 23 | 28 | 35 | 40 | ns |
| $t_{REM}$ | Minimum Removal Time Preset to Clock | | 2.0V | 55 | 100 | 125 | 150 | ns |
| | | | 4.5V | 11 | 20 | 25 | 30 | ns |
| | | | 6.0V | 9 | 17 | 21 | 25 | ns |
| $t_s$ | Minimum Setup Time J or K to Clock | | 2.0V | 77 | 100 | 125 | 150 | ns |
| | | | 4.5V | 15 | 20 | 25 | 30 | ns |
| | | | 6.0V | 13 | 17 | 21 | 25 | ns |
| $t_H$ | Minimum Hold Time J or K from Clock | | 2.0V | −3 | 0 | 0 | 0 | ns |
| | | | 4.5V | −3 | 0 | 0 | 0 | ns |
| | | | 6.0V | −3 | 0 | 0 | 0 | ns |
| $t_W$ | Minimum Pulse Width, Preset, Clear or Clock | | 2.0V | 55 | 80 | 100 | 120 | ns |
| | | | 4.5V | 11 | 16 | 20 | 24 | ns |
| | | | 6.0V | 9 | 14 | 18 | 20 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Time | | 2.0V | | 1000 | 1000 | 1000 | ns |
| | | | 4.5V | | 500 | 500 | 500 | ns |
| | | | 6.0V | | 400 | 400 | 400 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | (per flip-flop) | | 80 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

## Typical Applications

**N Bit Presettable Binary Ripple Counter with Enable**

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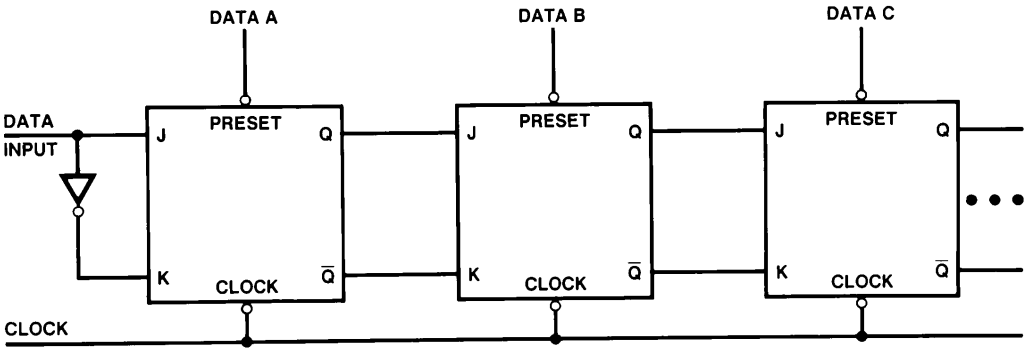
**N Bit Parallel Load/Serial Load Shift Register**

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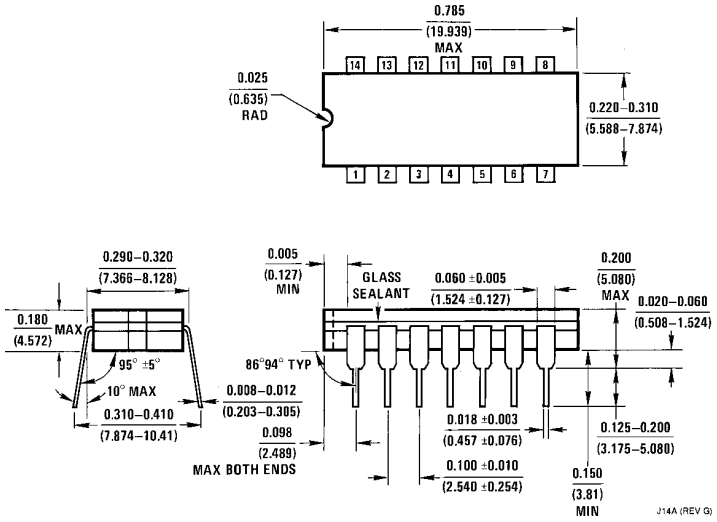
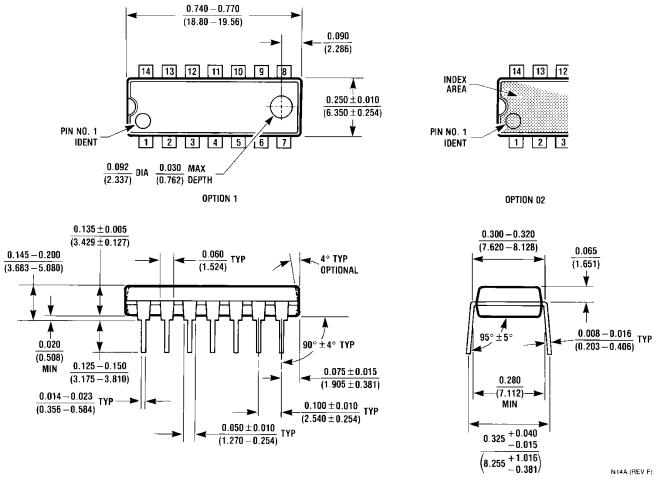
## Physical Dimensions inches (millimeters)




**Order Number MM54HC113J or MM74HC113J**
**NS Package J14A**

## Physical Dimensions inches (millimeters) (Continued)




**Order Number MM74HC113N**
**NS Package N14A**

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