National Semiconductor

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MM54HC149/MM74HC149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. Only one request output can be low at a time. The output that is low is dependent on the highest priority request that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RIn}$ is active.

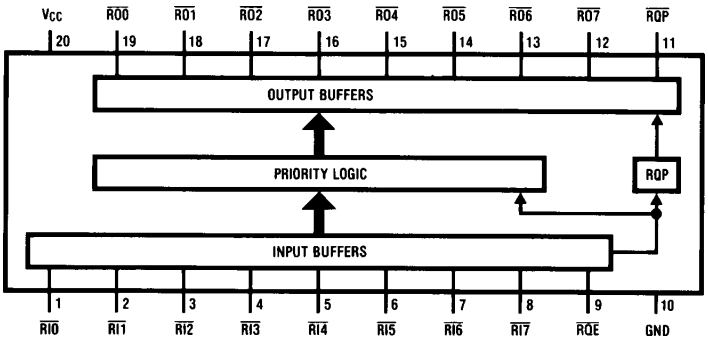
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- Propagation delay: 15 ns typical
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA max (74HC Series)
- Wide input noise immunity

Connection Diagram

Dual-In-Line Package



TL/F/5312–1

Top View

Order Number MM54HC149 or MM74HC149

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns (Note 6)

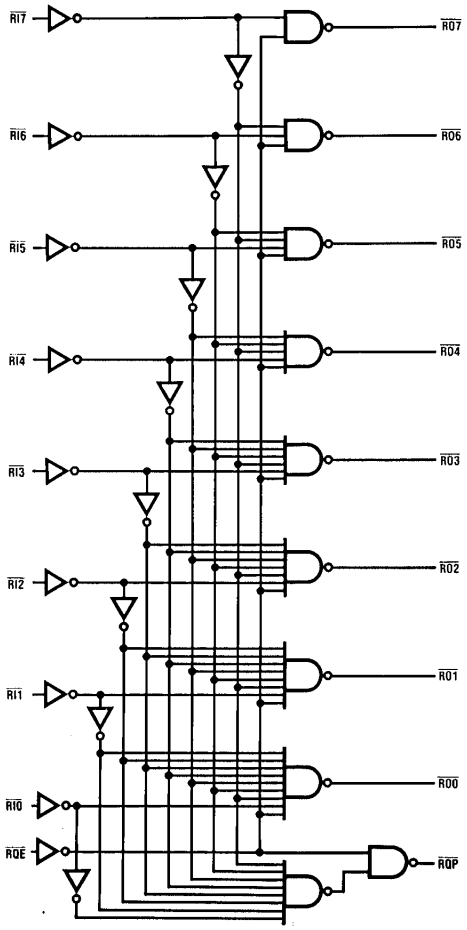
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Input To Any Output		20	33	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input To Any Output		2.0V 4.5V 6.0V	73 25 21	205 41 35	255 51 43	310 62 53	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			50				pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Simplified Logic Diagram



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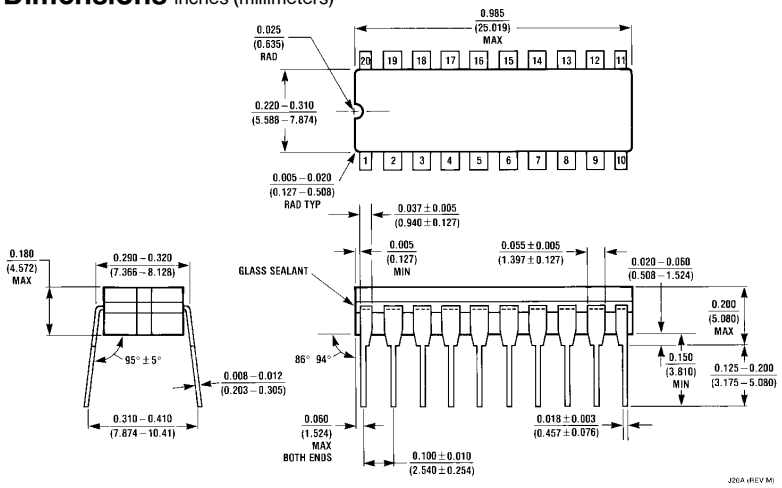
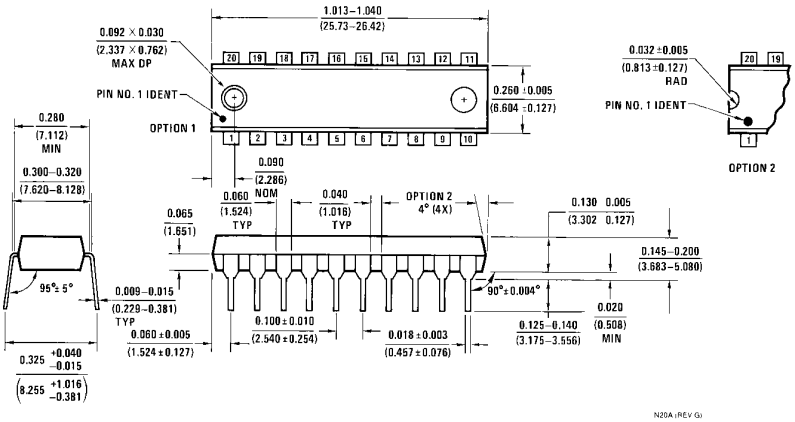
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC149J or MM74HC149J
NS Package J20A



Molded Dual-In-Line Package (N)
Order Number MM74HC149N
NS Package N20A

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