

## MM54HC166/MM74HC166 8-Bit Parallel In/Serial Out Shift Registers

### General Description

The MM54HC166/MM74HC166 high speed 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These Parallel-In or Serial-In, Serial-Out shift registers feature gated CLOCK inputs and an overriding CLEAR input. The load mode is established by the SHIFT/LOAD input. When high, this input enables the SERIAL INPUT and couples the eight flip-flops for serial shifting with each clock pulse. When low, the PARALLEL INPUTS are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the CLOCK pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or CLOCK INHIBIT function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be

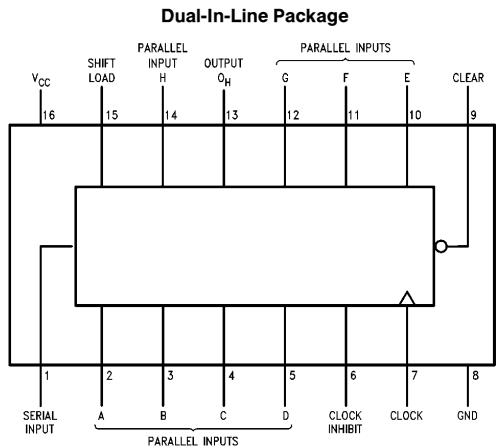
stopped on command with the other clock input. The CLOCK INHIBIT input should be changed to the high level only while the clock input is high. A direct CLEAR input overrides all other inputs, including the CLOCK, and sets all flip-flops to zero.

The 54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and Ground.

### Features

- Typical propagation delay:
- Wide operating supply voltage range: 2V–6V
- Low input current:  $<1 \mu A$
- Low quiescent supply current: 80  $\mu A$  maximum (74HC Series)
- Fanout of 10 LS-TTL loads

### Connection Diagram



Order Number MM54HC166 or MM74HC166

### Function Table

Clear	Inputs					Internal Outputs		Output $Q_H$
	Shift/Load	Clock Inhibit	Clock	Serial	Parallel A...H	$Q_A$	$Q_B$	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	$Q_{An}$	$Q_{Gn}$
H	H	L	↑	L	X	L	$Q_{An}$	$Q_{Gn}$
H	X	H	↑	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$

H = High Level (steady state), L = Low Level (steady state)  
 X = Don't Care (any input, including transitions)  
 ↑ = Transition from low to high level  
 a...h = The level of steady-state input at inputs A through H, respectively  
 $Q_{A0}, Q_{B0}, Q_{H0}$  = The level of  $Q_A, Q_B, Q_H$ , respectively, before the indicated steady-state input conditions were established  
 $Q_{An}, Q_{Gn}$  = The level of  $Q_A, Q_G$ , respectively, before the most recent ↑ transition of the clock

## Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5V to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	$\pm 20$ mA
DC Output Current, per Pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per Pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ ) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

## Operating Conditions

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

## DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40^\circ C$ to $+85^\circ C$	54HC $T_A = -55^\circ C$ to $+125^\circ C$		
$V_{IH}$	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND $V_{CC} = 2V-6V$	6.0V	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$ $V_{CC} = 2V-6V$	6.0V	8.0	80	160	$\mu A$	

**Note 1:** Absolute Maximum ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power dissipation temperature derating—plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V  $\pm$  10%, the worst-case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V, respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst-case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

**AC Electrical Characteristics**  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  unless otherwise noted

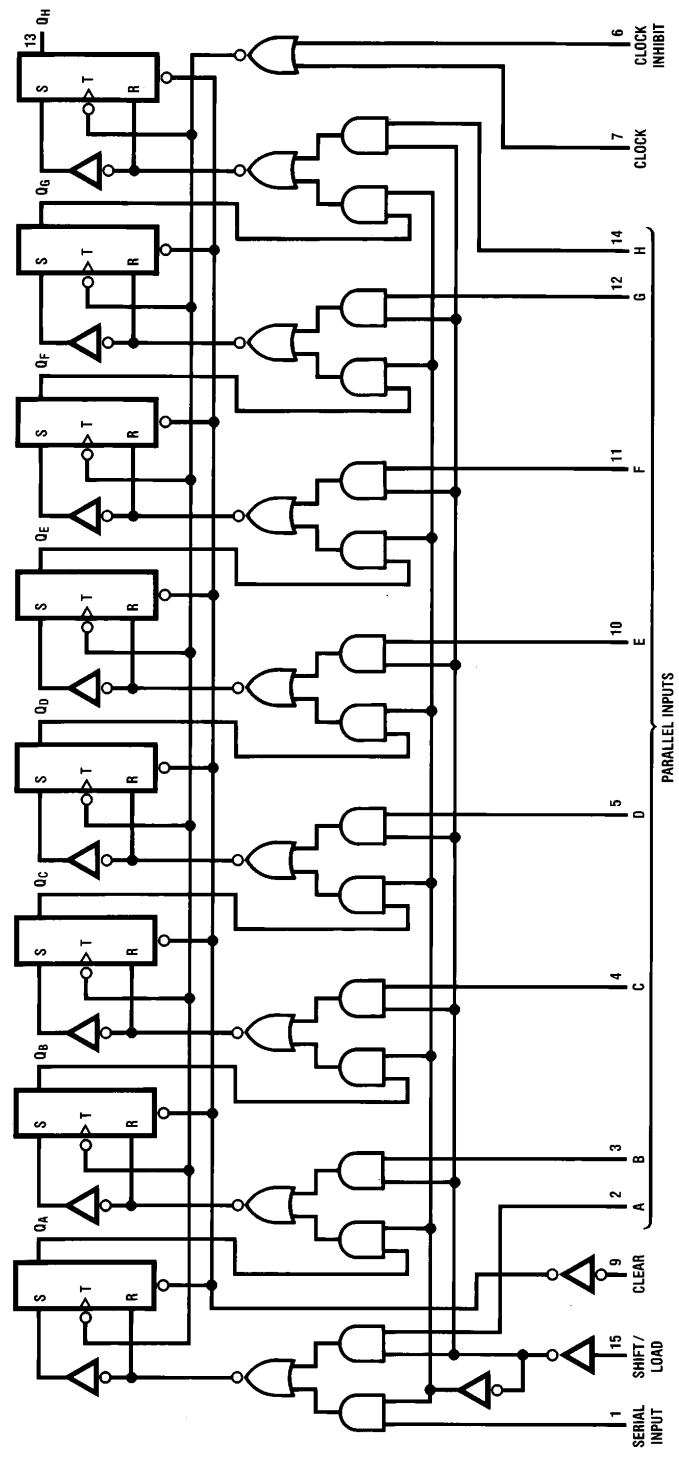
Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = 25°C		74HC	54HC	Units
			Typ		T <sub>A</sub> = -40°C to +85°C	T <sub>A</sub> = -55°C to +125°C	
f <sub>MAX</sub>	Maximum Operating Frequency	2.0V		6	5	4.2	MHz MHz MHz
		4.5V		31	25	21	
		6.0V		36	29	25	
t <sub>PHL</sub> / t <sub>PLH</sub>	Maximum Propagation Delay Clock to Q <sub>H</sub>	2.0V	14	140	175	210	ns ns ns
		4.5V		28	35	42	
		6.0V		24	30	36	
t <sub>PHL</sub> / t <sub>PLH</sub>	Maximum Propagation Delay Clear to Q <sub>H</sub>	2.0V	11	130	165	195	ns ns ns
		4.5V		26	35	39	
		6.0V		22	30	33	
t <sub>su</sub>	Minimum Setup Time Shift/Load to Clock	2.0V		80	100	120	ns ns ns
		4.5V		16	20	24	
		6.0V		14	18	20	
t <sub>su</sub>	Minimum Setup Time Data before Clock	2.0V		80	100	120	ns ns ns
		4.5V		16	20	24	
		6.0V		14	18	20	
t <sub>REM</sub>	Minimum Removal Time Clear to Clock	2.0V		0	0	0	ns ns ns
		4.5V		0	0	0	
		6.0V		0	0	0	
t <sub>h</sub>	Maximum Hold Time Data after Clock	2.0V		0	0	0	ns ns ns
		4.5V		0	0	0	
		6.0V		0	0	0	
t <sub>r</sub> , t <sub>f</sub>	Maximum Output Rise and Fall Time	2.0V	7	75	95	110	ns ns ns
		4.5V		15	19	22	
		6.0V		13	16	19	
t <sub>w</sub>	Minimum Pulse Width Clock or Clear	2.0V		80	100	120	ns ns ns
		4.5V		16	20	24	
		6.0V		14	16	20	
C <sub>pd</sub>	Power Dissipation Capacitance (Note 5)	(per package)		100			pF
C <sub>in</sub>	Maximum Input Capacitance		5	10	10	10	pF

**AC Electrical Characteristics**  $V_{CC} = 5V$ ,  $C_L = 15 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $t_r = t_f = 6 \text{ ns}$  unless otherwise noted

Symbol	Parameter	Typical	Guaranteed Limits	Units
f <sub>MAX</sub>	Maximum Operating Frequency		31	MHz
t <sub>PHL</sub> / t <sub>PLH</sub>	Maximum Propagation Delay Clock to Q <sub>H</sub>		16	ns
t <sub>PHL</sub> / t <sub>PLH</sub>	Maximum Propagation Delay Clear to Q <sub>H</sub>		12	ns
t <sub>su</sub>	Minimum Setup Time Shift/Load High to Clock		16	ns
t <sub>su</sub>	Minimum Setup Time Data before Clock		16	ns
t <sub>REM</sub>	Minimum Removal Time Clear to Clock		0	ns
t <sub>h</sub>	Maximum Hold Time Data after Clock		0	ns
t <sub>w</sub>	Minimum Pulse Width Clock or Clear		16	ns

**Note 5:** C<sub>pd</sub> determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

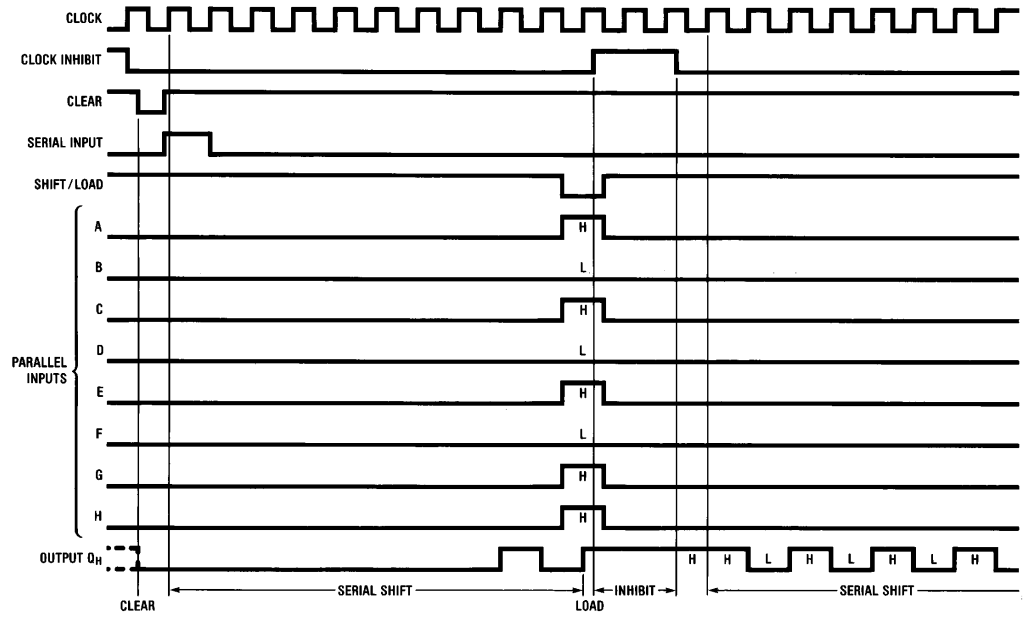
# Logic Diagram



TL/F 5770-2

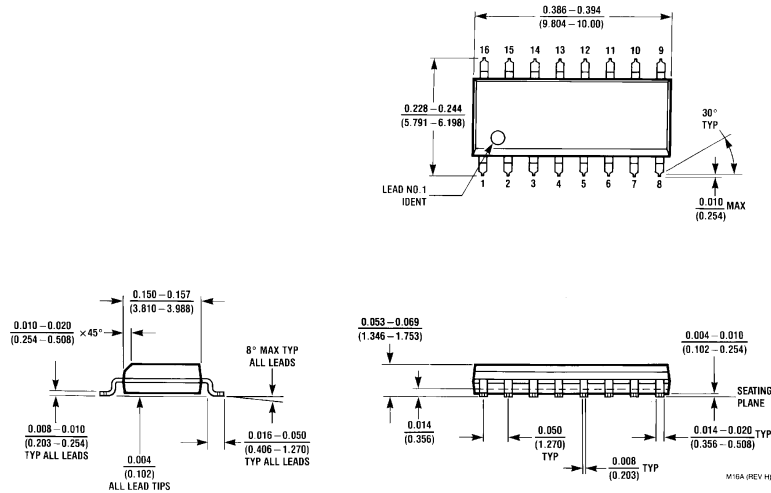
# Logic Diagram

## Typical Clear, Shift, Load, Inhibit and Shift Sequences

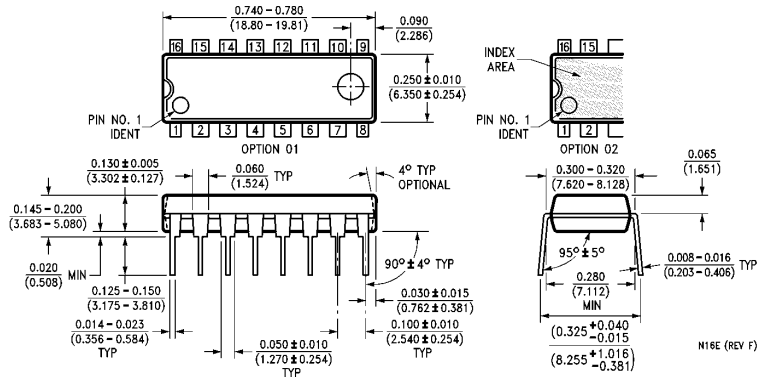


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**Physical Dimensions** inches (millimeters)



Order Number MM54HC166 or MM74HC166  
NS Package Number M16A



Order Number MM54HC166 or MM74HC166  
NS Package Number N16E

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