National Semiconductor

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MM54HC181/MM74HC181
Arithmetic Logic Units/Function Generators

General Description

These arithmetic logic units (ALU)/function generators utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM54HC181/MM74HC181 are arithmetic logic unit (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the MM54HC182 or MM74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading HC182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the MM54HC182/MM74HC182.

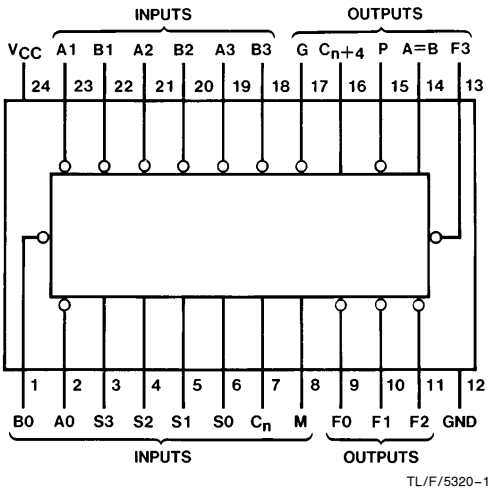
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Full look-ahead for high-speed operations on long words
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand a one position magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



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Top View

Order Number MM54HC181 or MM74HC181

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

RRD-B30M105/Printed in U. S. A.

General Description (Continued)

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to produce A—B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The MM54HC181/MM74HC181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table 1)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A ≤ B	A ≥ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≥ B	A ≤ B

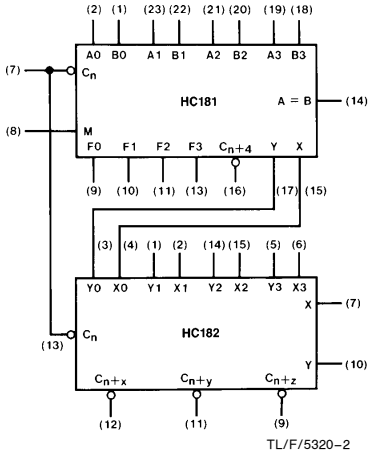

FIGURE 1

Table I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)

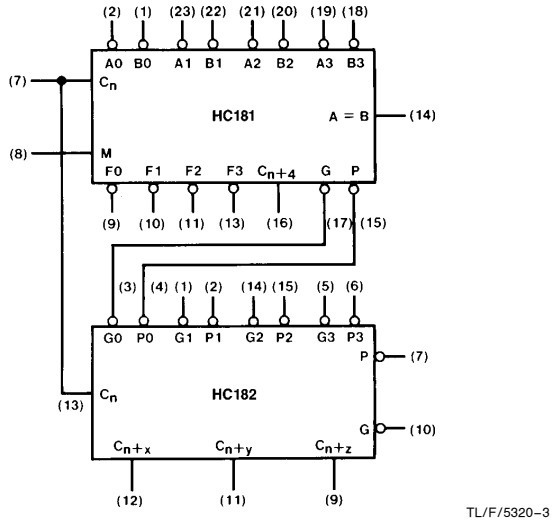

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FIGURE 2

Table II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A + B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$ Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage (any output except A = B)	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
I_{LKG}	Maximum Leakage Open Drain Output Current (A = B Output)	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}	6.0V		0.5	5.0	10	μA
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25°C, C_L = 15\ pF, t_r = t_f = 6\ ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = V_{CC} S1 = S0 = 0V ($\overline{\text{Sum}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff.}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff.}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	27	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	24	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	19	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	25	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	25	37	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		2.0V		125	155	190	ns
			4.5V		25	31	38	ns
			6.0V		22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	110	250	325	375	ns
			4.5V	35	50	63	75	ns
			6.0V	30	43	53	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V		250	325	375	ns
			4.5V		50	63	75	ns
			6.0V		43	53	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ mode)	2.0V	65	150	190	225	ns
			4.5V	22	32	40	48	ns
			6.0V	14	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC}, S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	70	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	12	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 ($\overline{\text{Diff}}$ mode)	2.0V	65	165	210	250	ns
			4.5V	23	33	42	50	ns
			6.0V	16	29	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	80	220	275	330	ns
			4.5V	30	44	55	66	ns
			6.0V	25	37	47	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	75	195	244	293	ns
			4.5V	27	39	49	60	ns
			6.0V	24	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	70	180	225	270	ns
			4.5V	26	36	45	54	ns
			6.0V	21	31	39	47	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V		160	200	290	ns
			4.5V		32	40	48	ns
			6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	2.0V	180	200	250	300	ns
			4.5V	30	40	50	60	ns
			6.0V	23	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	180	200	250	300	ns
			4.5V	30	40	50	60	ns
			6.0V	23	34	43	51	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			300				pF
C_{IN}	Maximum Input Capacitance			5	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Parameter Measurement Information

Logic Mode Test Table **Function Inputs: S1 = S2 = M = V_{CC}, S0 = S3 = 0 V**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase

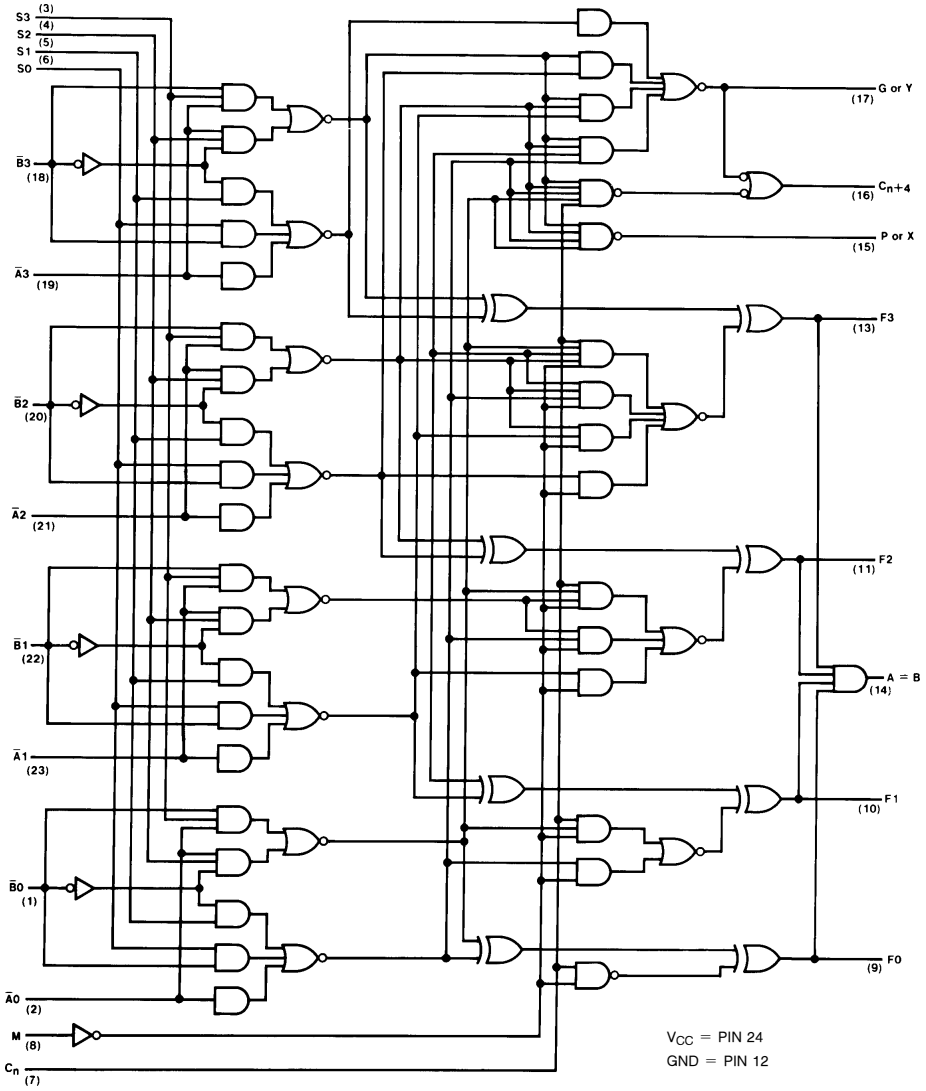
$\overline{SUM}$ Mode Test Table **Function Inputs: S0 = S3 = V_{CC}** **S1 = S2 = M = 0 V**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A	All B	Any F or $C_n + 4$	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	$C_n + 4$	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	$C_n + 4$	Out-of-Phase

$\overline{Diff}$ Mode Test Table **Function Inputs: S1 = S2 = V_{CC}, S0 = S3 = M = 0 V**

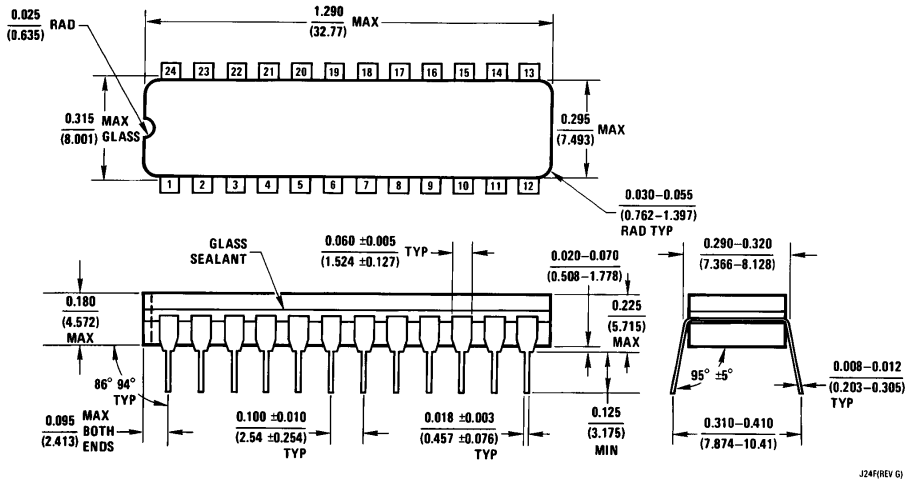
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A and B	None	$C_n + 4$ or any F	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A, B, C_n	$C_n + 4$	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A, B, C_n	$C_n + 4$	In-Phase

Logic Diagram



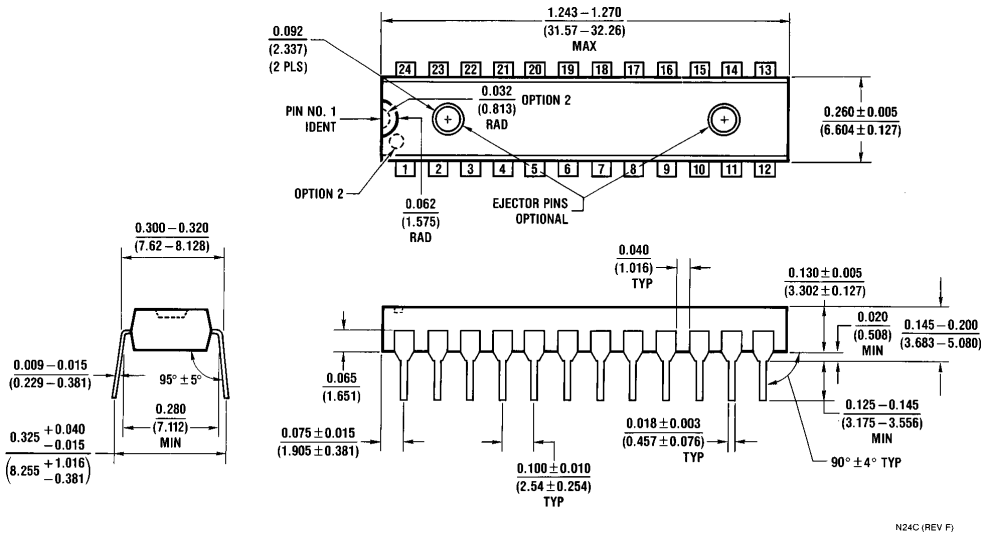
TL/F/5320–4

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC181J or MM74HC181J
NS Package Number J24F

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number MM74HC181N
NS Package Number N24C

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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