

MM54HC253/MM74HC253 Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

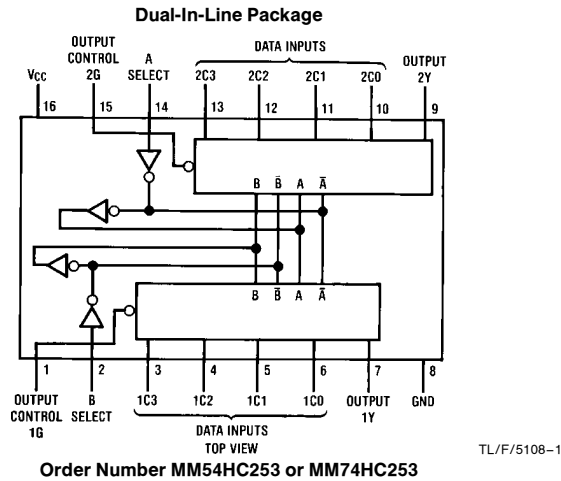
When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads

Connection Diagram



Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off).

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$		Units
				Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5		V	
			4.5V		3.15	3.15	3.15		V	
			6.0V		4.2	4.2	4.2		V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5		V	
			4.5V		1.35	1.35	1.35		V	
			6.0V		1.8	1.8	1.8		V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9		V	
			4.5V	4.5	4.4	4.4	4.4		V	
			6.0V	6.0	5.9	5.9	5.9		V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7		V	
			6.0V	5.7	5.48	5.34	5.2		V	
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1		V	
			4.5V	0	0.1	0.1	0.1		V	
			6.0V	0	0.1	0.1	0.1		V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 4.0$ mA $ I_{OUT} \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4		V	
			6.0V	0.2	0.26	0.33	0.4		V	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0		μA	
I_{OZ}	Maximum TRI-STATE Output Leakage Current	Strobe = V_{CC} $V_{OUT} = V_{CC}$ or GND	6.0V		± 0.5	± 5.0	± 10		μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160		μA	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}, C_L=15\text{ pF}$

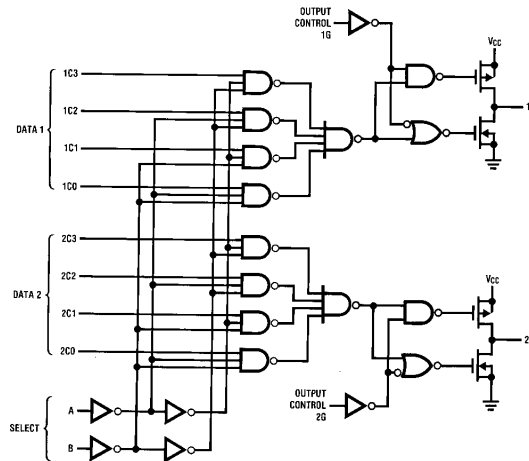
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		24	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		18	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	$R_L = 1\text{ k}\Omega$	13	18	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	$R_L = 1\text{ k}\Omega$	18	27	ns

AC Electrical Characteristics $C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

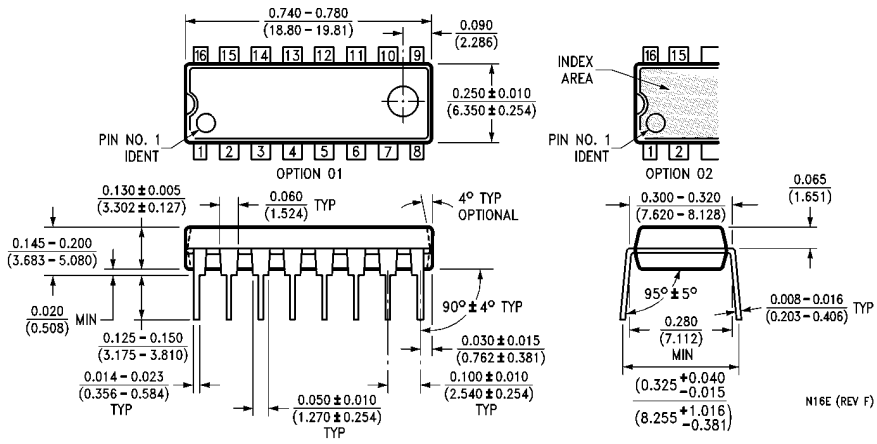
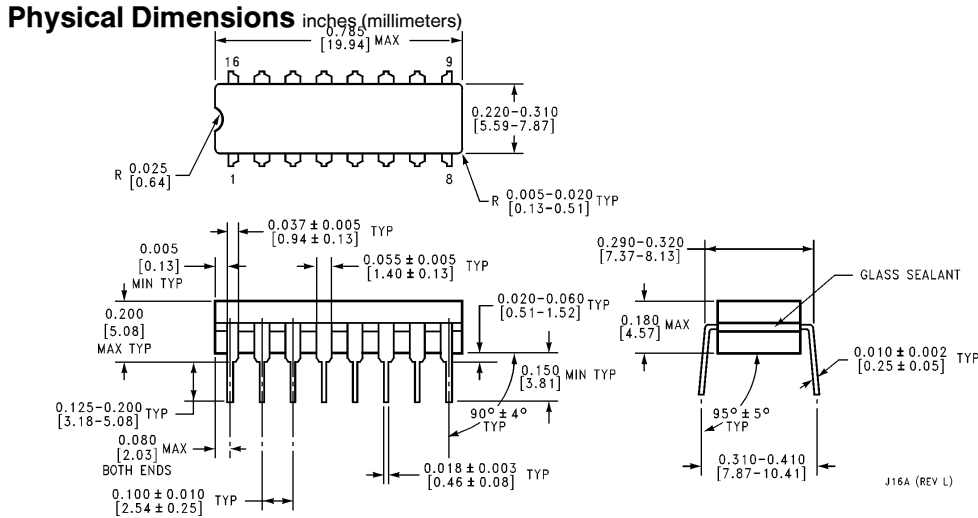
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^{\circ}C$		$T_A = -40\text{ to }85^{\circ}C$		$T_A = -55\text{ to }125^{\circ}C$		Units
				Typ	Guaranteed Limits					
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns		
			4.5V	29	35	44	53	ns		
			6.0V	24	30	38	45	ns		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	126	158	189	ns		
			4.5V	22	28	35	42	ns		
			6.0V	19	23	29	35	ns		
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1\text{ k}\Omega$	2.0V	63	90	113	135	ns		
			4.5V	14	20	25	30	ns		
			6.0V	12	17	21	26	ns		
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\text{ k}\Omega$	2.0V	90	135	169	203	ns		
			4.5V	20	30	38	45	ns		
			6.0V	17	25	31	38	ns		
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns		
			4.5V	8	15	19	22	ns		
			6.0V	7	13	16	19	ns		
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF		
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Outputs Enabled Outputs Disabled		90				pF		
				25				pF		

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram




TL/F/5108-2



LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

 <p>National Semiconductor Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: (800) 272-9959 Fax: (800) 737-7018</p>	<p>National Semiconductor Europe</p> <p>Fax: (+49) 0-180-530 85 86 Email: cnjwge@tevm2.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tel: (+49) 0-180-532 78 32 Français Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80</p>	<p>National Semiconductor Hong Kong Ltd. 19th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960</p>	<p>National Semiconductor Japan Ltd. Tel: 81-043-299-2309 Fax: 81-043-299-2408</p>
--	---	---	---

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.