National Semiconductor

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MM74HC594 8-Bit Shift Register with Output Registers

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clears are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

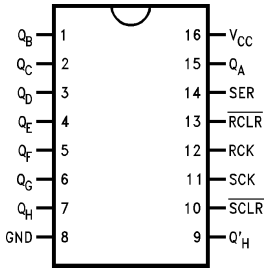
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TL/F/10915–1

Top View

Order Number MM74HC594
See NS Package Number N16E

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{RCLR}$	Function
X	X	X	L	Storage Register cleared
X	X	L	X	Shift Register cleared $Q'_H = 0$
X	↑	H	H	Shift Register clocked $Q_N = Q_{n-1}$, $Q_0 = SER$
↑	X	H	H	Contents of Shift Register transferred to output latches

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	-0.5 to $+7.0$V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to $+150$°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	$+85$	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC}=2.0$V		1000	ns
$V_{CC}=4.5$V		500	ns
$V_{CC}=6.0$V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25$°C		74HC $T_A=-40$ to 85°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
	Q'_H	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	V
	Q_A thru Q_H	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
	Q'_H	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	V
	Q_A thru Q_H	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		± 0.1	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0$ μA	6.0V		8.0	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

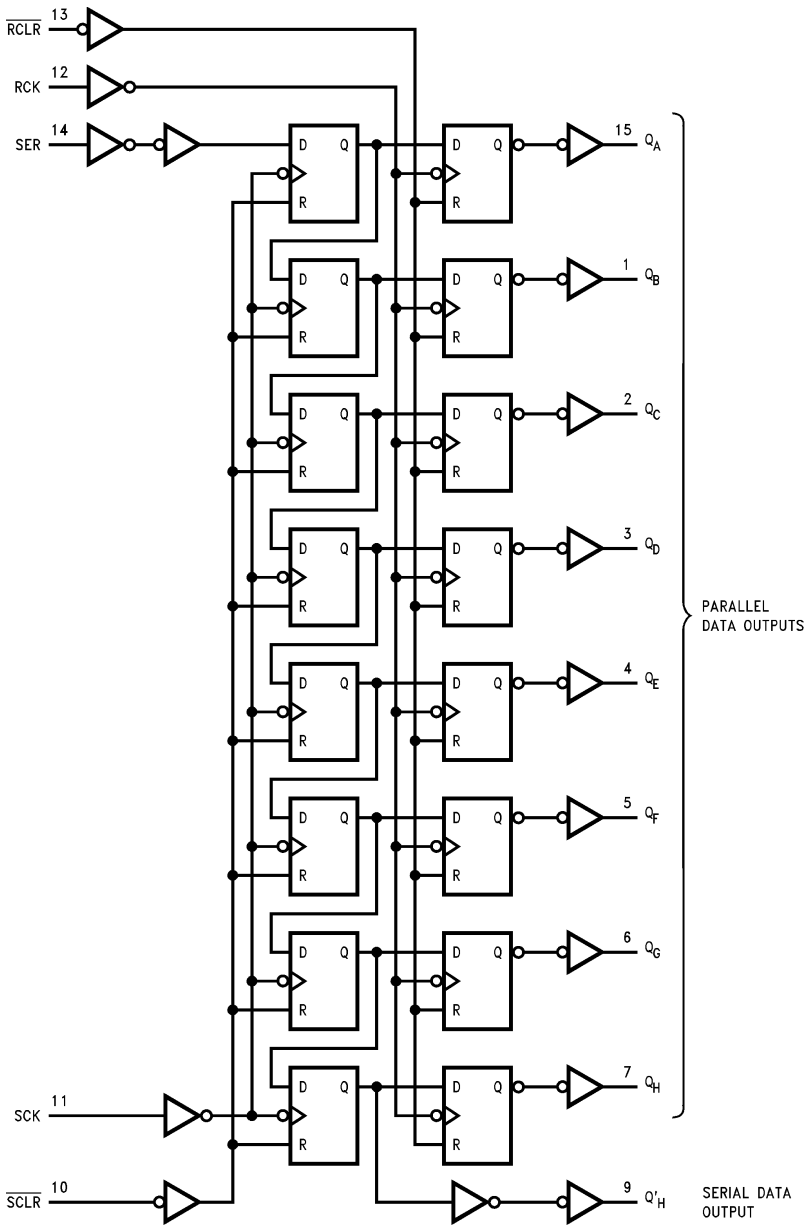
Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5$V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} and I_{CC}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	Units
				Typ	Guaranteed Limits	
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V 4.5V 6.0V		6 30 35	4.8 24 28	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q'_H	$C_L=50$ pF	2.0V 4.5V 6.0V		150 30 25	185 37 31	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L=50$ pF $C_L=150$ pF	2.0V 2.0V		150 200	185 250	ns ns
		$C_L=50$ pF $C_L=150$ pF	4.5V 4.5V		30 40	37 50	ns ns
		$C_L=50$ pF $C_L=150$ pF	6.0V 6.0V		25 34	31 43	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SCLR}$ to Q'_H		2.0V 4.5V 6.0V		150 30 25	185 37 31	ns ns ns
t_{PHL}	Maximum Propagation Delay from $\overline{RCLR}$ to Q_A thru Q_H	C_L = 50 pF	2.0V 4.5V 6.0V		125 25 21	155 31 26	ns ns ns
		C_L = 150 pF	2.0V 4.5V 6.0V		200 40 34	250 50 43	ns ns ns
t_S	$\overline{SCLR}$ Low to RCK		2.0V 4.5V 6.0V		50 10 9	63 13 11	ns ns ns
t_S	$\overline{RCLR}$ High to SCK		2.0V 4.5V 6.0V		5 5 5	5 5 5	ns ns ns
t_S	Minimum Setup Time from SER to SCK		2.0V 4.5V 6.0V		90 18 15	110 22 19	ns ns ns
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK		2.0V 4.5V 6.0V		20 10 10	20 10 10	ns ns ns
t_S	Minimum Setup Time from SCK to RCK		2.0V 4.5V 6.0V		90 18 15	110 22 19	ns ns ns
t_H	Minimum Hold Time SER to SCK		2.0V 4.5V 6.0V		5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$ or RCK or $\overline{RCLR}$		2.0V 4.5V 6.0V		100 20 17	125 25 21	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q_A–Q_H		2.0V 4.5V 6.0V		60 12 10	75 15 13	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q'_H		2.0V 4.5V 6.0V		75 15 13	95 19 16	ns ns ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G}=V_{CC}$ $\overline{G}=GND$		90 150			pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram (positive logic)



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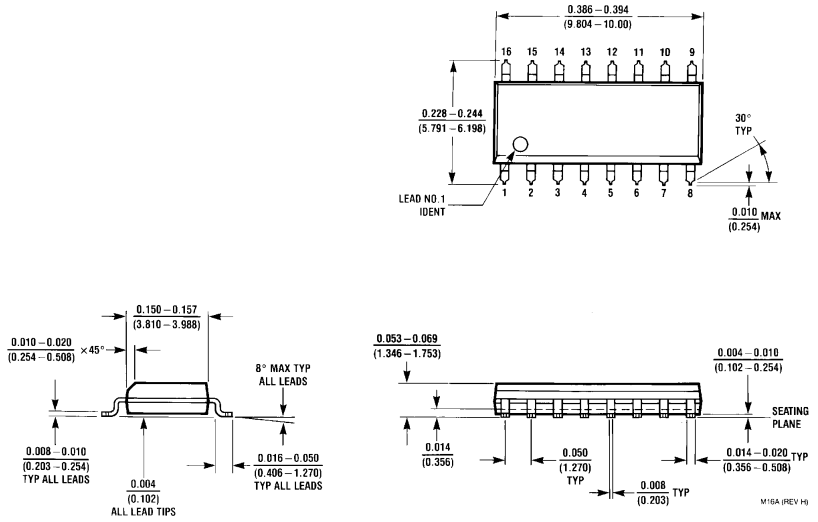
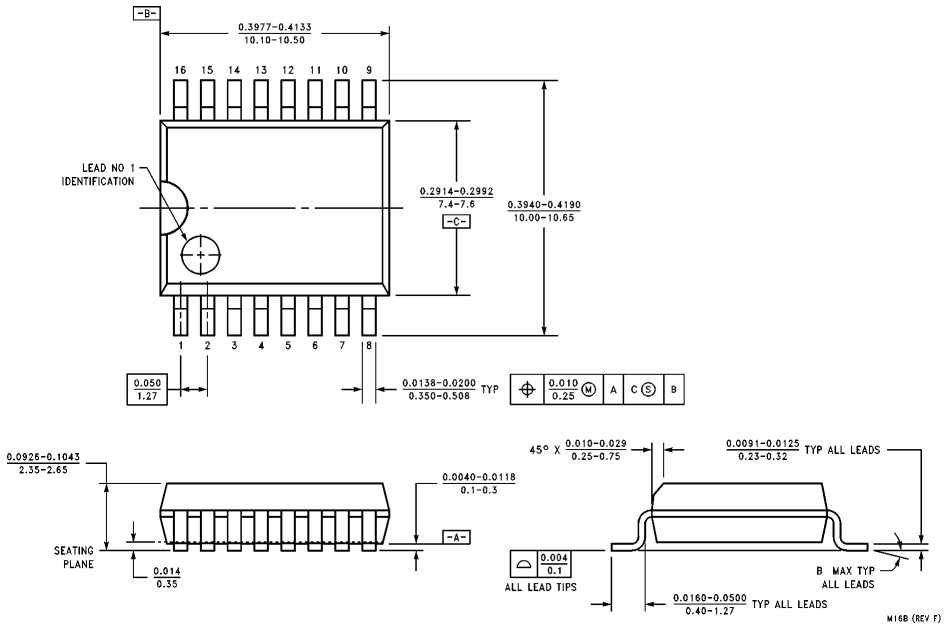
Physical Dimensions inches (millimeters)

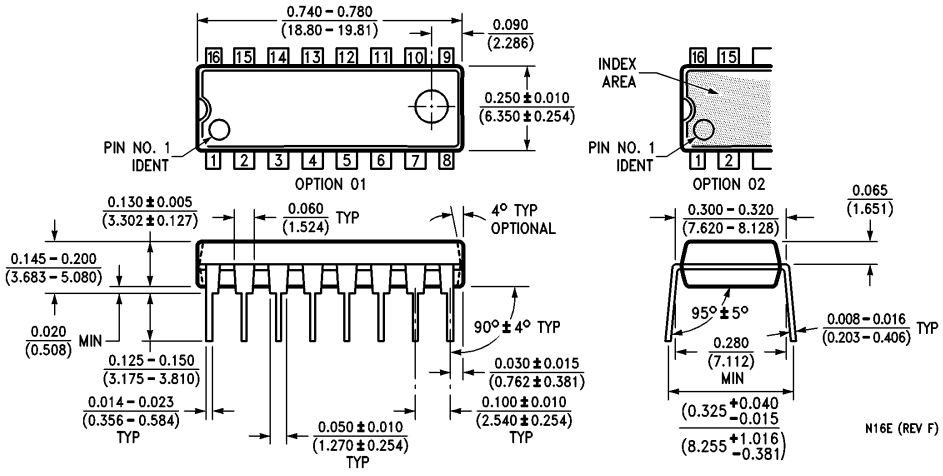


Order Number MM74HC594M
NS Package Number M16A



Order Number MM74HC594WM
NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)



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NS Package Number N16E

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408