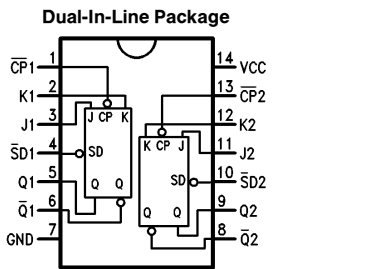


# 54LS113 Dual JK Edge-Triggered Flip-Flop

## General Description

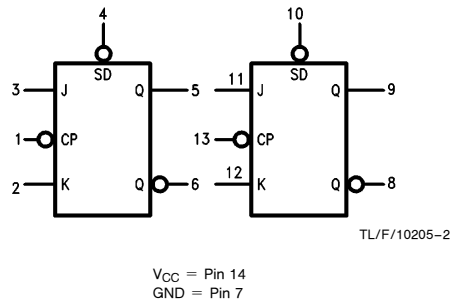
The 54LS113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

## Connection Diagram



Order Number 54LS113DMQB,  
54LS113FMQB or 54LS113LMQB  
See NS Package Number E20A, J14A or W14B

## Logic Symbol



## Truth Table

Inputs		Output
@ t <sub>n</sub>		@ t <sub>n</sub> + 1
J	K	Q
L	L	Q <sub>n</sub>
L	H	L
H	L	H
H	H	$\bar{Q}_n$

t<sub>n</sub> = Bit Time before Clock Pulse  
t<sub>n</sub> + 1 = Bit Time after Clock Pulse  
H = HIGH Voltage Level  
L = LOW Voltage Level

### Asynchronous Input:

Low input to  $\bar{S}_D$  sets Q to HIGH level  
Set is independent of clock

Pin Names	Description
J1, J2, K1, K2	Data Inputs
$\bar{C}P1, \bar{C}P2$	Clock Pulse Inputs (Active Falling Edge)
$\bar{S}D1, \bar{S}D2$	Direct Set Inputs (Active LOW)
Q1, Q2, $\bar{Q}1, \bar{Q}2$	Outputs

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
54LS	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual operation.

## Recommended Operating Conditions

Symbol	Parameter	54LS113			Units
		Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7	V
I <sub>OH</sub>	High Level Output Current			–0.4	mA
I <sub>OL</sub>	Low Level Output Current			4	mA
T <sub>A</sub>	Free Air Operating Temperature	–55		125	°C
t <sub>s</sub> (H)	Setup Time	20			ns
t <sub>s</sub> (L)	J <sub>n</sub> or K <sub>n</sub> to $\overline{CP}_n$	20			ns
t <sub>h</sub> (H)	Hold Time	0			ns
t <sub>h</sub> (L)	J <sub>n</sub> or K <sub>n</sub> to $\overline{CP}_n$	0			ns
t <sub>w</sub> (H)	$\overline{CP}_n$ Pulse Width	20			ns
t <sub>w</sub> (L)		15			ns
t <sub>w</sub> (L)	$\overline{SD}_n$ Pulse Width LOW	15			ns

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	2.5			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min, V <sub>IL</sub> = Max			0.4	V
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 5.5V	J, K		0.1	mA
			SD		0.3	
			CP		0.4	
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V	J, K		20	μA
			SD		60	
			CP		80	
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.5V	J, K	–30	–400	μA
			CP, SD	–60	–800	
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	–20		–100	mA
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max (Note 3)			8	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

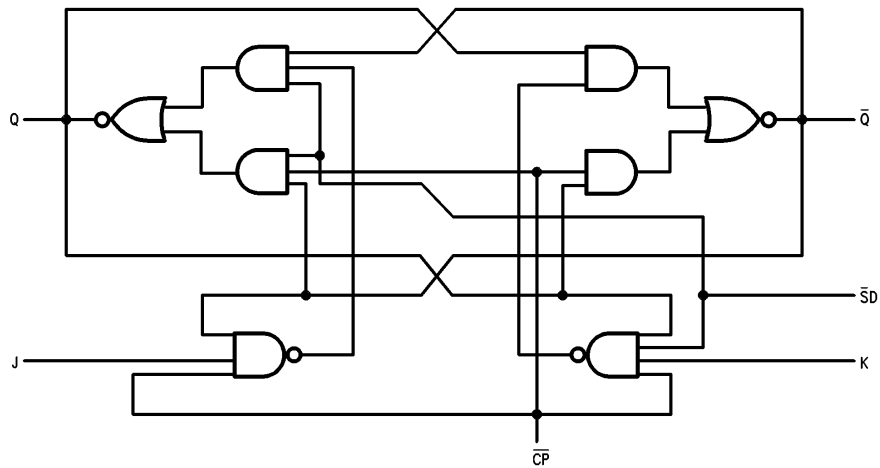
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I<sub>CC</sub> is measured with all outputs open and all inputs grounded.

**Switching Characteristics**  $V_{CC} = +5.0V, T_A = +25^\circ C$  (See Section 1 for test waveforms and output load)

Symbol	Parameter	54LS113		Units
		$C_L = 15 \text{ pF}$		
		Min	Max	
$f_{max}$	Maximum Clock Frequency	30		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CP}_n$ to $Q_n$ or $\overline{Q}_n$		16 24	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{SD}_n$ to $Q_n$ or $\overline{Q}_n$		16 24	ns

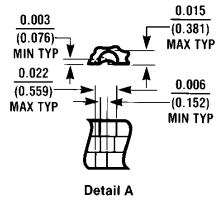
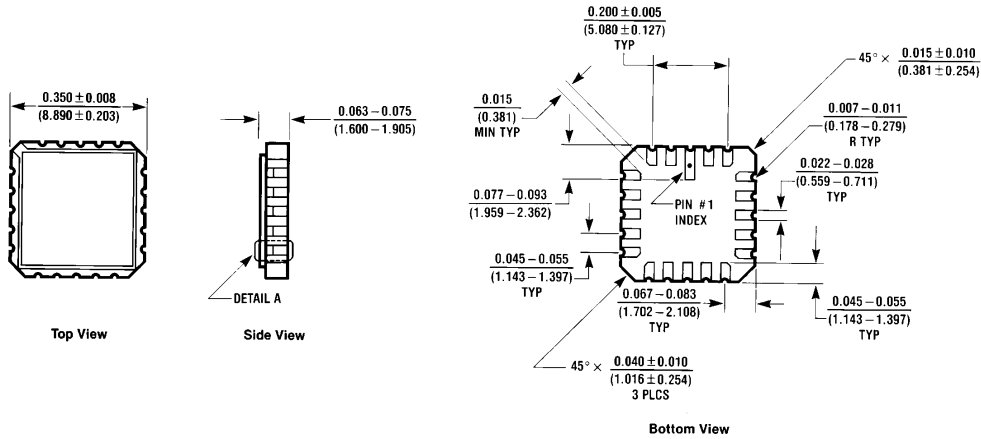
**Logic Diagram** (one half shown)



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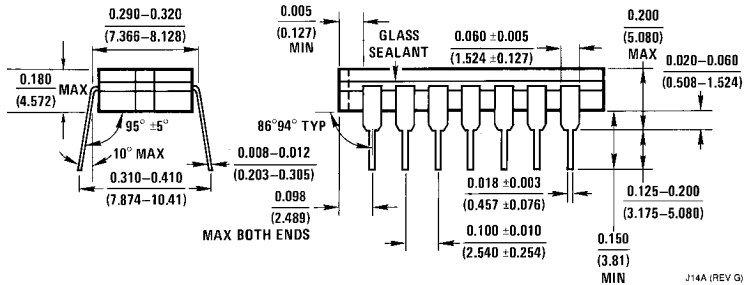
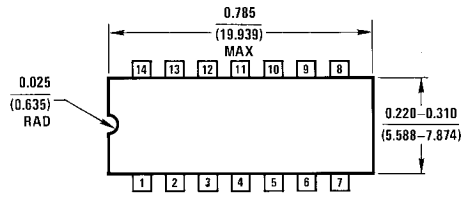


**Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)**  
**Order Number 54LS113LMQB**  
**NS Package Number E20A**

E20A (REV D)



**14-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54LS113DMQB**  
**NS Package Number J14A**

J14A (REV G)

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)**  
**Order Number 54LS113FMQB**  
**NS Package Number W14B**

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