

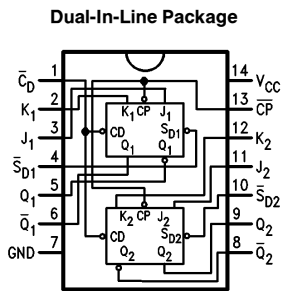
# 54LS114 Dual JK Negative Edge-Triggered Flip-Flop with Common Clocks and Clears

## General Description

The 'LS114 features individual J, K and set inputs and common clock and common clear inputs. When the clock goes HIGH the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change

when the Clock Pulse is HIGH and the bistable will perform according to the truth table as long as the minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

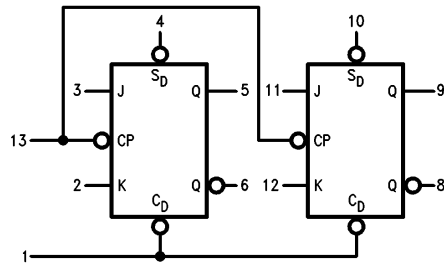
## Connection Diagram



TL/F/10176-1

**Order Number 54LS114DMQB,  
54LS114FMQB or 54LS114LMQB  
See NS Package Number E20A, J14A or W14B**

## Logic Symbol



TL/F/10176-2

VCC = Pin 14  
GND = Pin 7

Pin Names	Description
J1, J2, K1, K2	Data Inputs
CP	Clock Pulse Input (Active Falling Edge)
CD-bar	Direct Clear Input (Active LOW)
SD1-bar, SD2-bar	Direct Set Inputs (Active LOW)
Q1, Q2, Q1-bar, Q2-bar	Outputs

**54LS114 Dual JK Negative Edge-Triggered Flip-Flop  
with Common Clocks and Clears**

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	54LS114			Units
		Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	V
V <sub>IH</sub>	High Level Input Voltage	2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7	V
I <sub>OH</sub>	High Level Output Current			–0.4	mA
I <sub>OL</sub>	Low Level Output Current			4	mA
T <sub>A</sub>	Free Air Operating Temperature	–55		125	°C
t <sub>s</sub> (H)	Setup Time	20			ns
t <sub>s</sub> (L)	Jn or Kn to $\overline{CP}$	20			ns
t <sub>h</sub> (H)	Hold Time	0			ns
t <sub>h</sub> (L)	Jn or Kn to $\overline{CP}$	0			ns
t <sub>w</sub> (H)	$\overline{CP}$ Pulse Width	20			ns
t <sub>w</sub> (L)		15			ns
t <sub>w</sub>	$\overline{CD}$ or $\overline{SDn}$ Pulse Width	15			ns

## Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = –18 mA			–1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	2.5			V
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min			0.4	V
					0.5	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 10V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			0.1	mA
					0.3	mA
					0.6	mA
					0.8	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V; Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			20	μA
					60	μA
					120	μA
					160	μA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

## Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$I_{IL}$	Low Level Input Current	$V_{CC} = \text{Max}$ , $V_I = 0.4V$ Jn, Kn Inputs SD1, SD2 Inputs CD Input CP Input			-0.4 -0.8 -1.6 -1.44	mA mA mA mA
$I_{OS}$	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 2)	-20		-100	mA
$I_{CC}$	Supply Current	$V_{CC} = \text{Max}$ , $V_{CP} = 0V$			8.0	mA

**Note 1:** All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$ .

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics

$V_{CC} = +5.0V$ ,  $T_A = +25^\circ\text{C}$  (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$R_L = 2k$ , $C_L = 15\text{ pF}$		Units
		Min	Max	
$f_{\text{max}}$	Maximum Count Frequency	30		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CP}$ to Q or $\overline{Q}$		16 24	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay CD or $\overline{SDn}$ to Q or $\overline{Q}$		16 24	ns

## Truth Table

Inputs		Output
@ $t_n$		@ $t_{n+1}$
J	K	Q
L	L	$Q_n$
L	H	L
H	L	H
H	H	$\overline{Q_n}$

Asynchronous Inputs:

LOW input to  $\overline{SD}$  sets Q to HIGH level

LOW input to  $\overline{CD}$  sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on  $\overline{CD}$  and  $\overline{SD}$

makes both Q and  $\overline{Q}$  HIGH

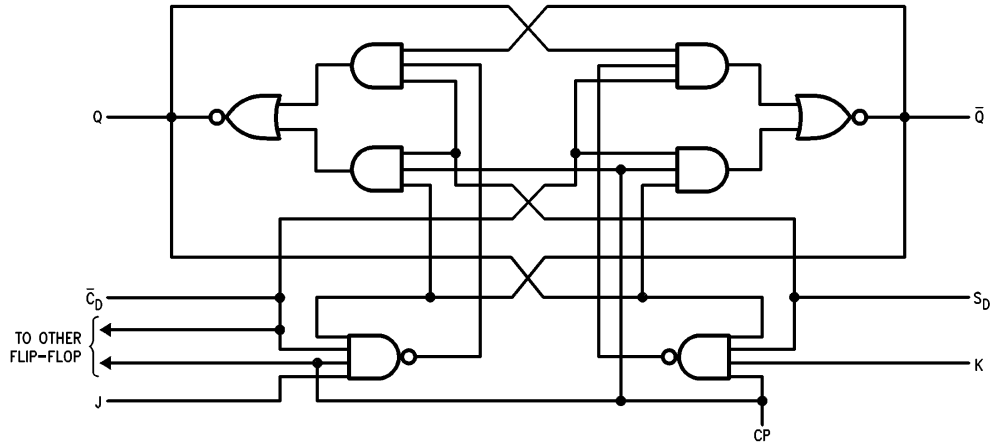
H = HIGH Voltage Level

L = LOW Voltage Level

$t_n$  = Bit time before clock pulse.

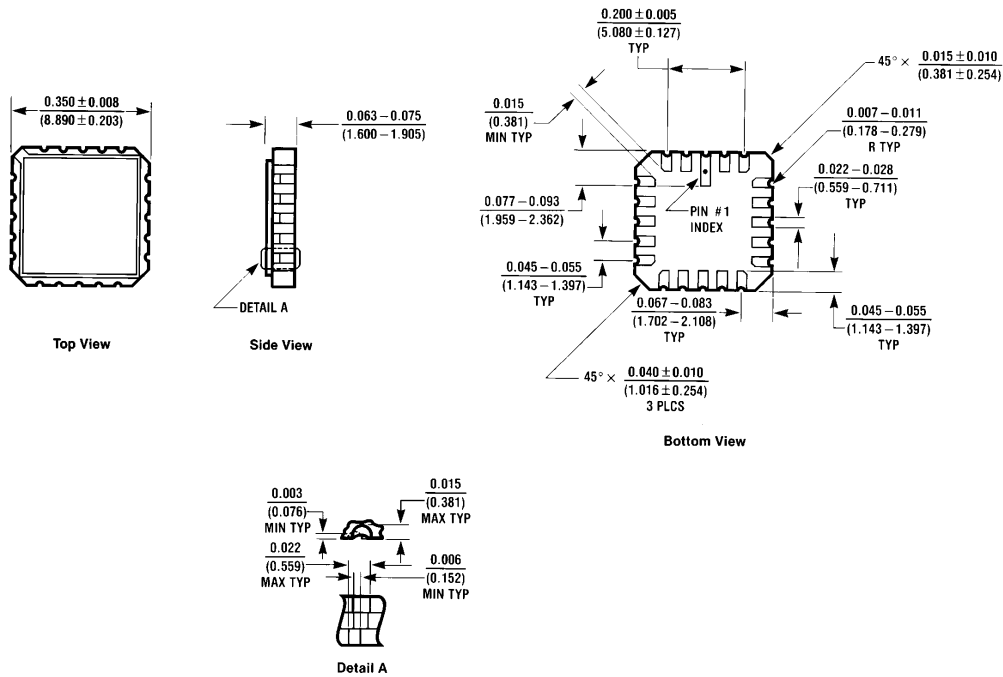
$t_{n+1}$  = Bit time after clock pulse.

**Logic Diagram** (one half shown)



TL/F/10176-3

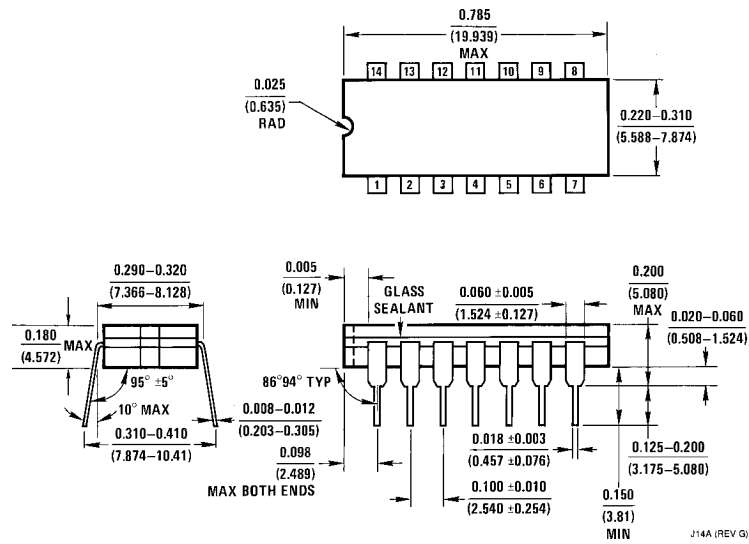
**Physical Dimensions** inches (millimeters)



E20A (REV D)

**Ceramic Leadless Chip Carrier (E)**  
**Order Number 54LS114LMQB**  
**NS Package Number E20A**

**Physical Dimensions** inches (millimeters) (Continued)

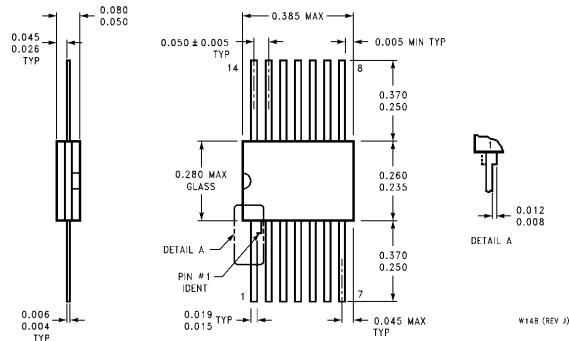


**14-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54LS114DMQB**  
**NS Package Number J14A**

J14A (REV G)

**54LS114 Dual JK Negative Edge-Triggered Flip-Flop  
with Common Clocks and Clears**

**Physical Dimensions** inches (millimeters) (Continued)



**14-Lead Ceramic Flat Package (W)  
Order Number 54LS114FMQB  
NS Package Number W14B**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
1111 West Bardin Road  
Arlington, TX 76017  
Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018

**National Semiconductor Europe**  
Fax: (+49) 0-180-530 85 86  
Email: cnjwge@tevm2.nsc.com  
Deutsch Tel: (+49) 0-180-530 85 85  
English Tel: (+49) 0-180-532 78 32  
Français Tel: (+49) 0-180-532 93 58  
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**  
19th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**  
Tel: 81-043-299-2309  
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.