

## 54LS379/DM74LS379 Quad Parallel Register with Enable

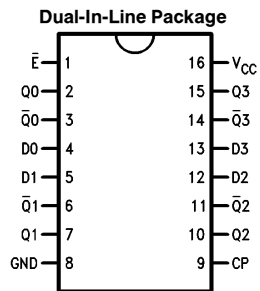
### General Description

The LS379 is a 4-bit register with buffered common Enable. This device is similar to the LS175 but features the common Enable rather than common Master Reset.

### Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs

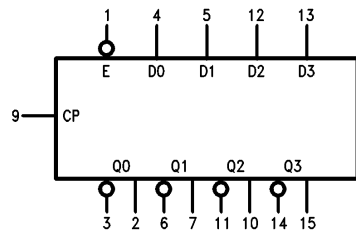
### Connection Diagram



TL/F/10186-1

Order Number 54LS379DMQB, 54LS379FMQB,  
54LS379LMQB, DM74LS379M or DM74LS379N  
See NS Package Number E20A,  
J16A, M16A, N16E or W16A

### Logic Symbol



TL/F/10186-2

$V_{CC}$  = Pin 16  
GND = Pin 8

Pin Names	Description
$\bar{E}$	Enable Input (Active LOW)
D0-D3	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0-Q3	Flip-Flop Outputs
$\bar{Q}0-\bar{Q}3$	Complement Outputs

## Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameter	54LS379			DM74LS379			Units
		Min	Nom	Max	Min	Nom	Max	
V <sub>CC</sub>	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High Level Input Voltage	2			2			V
V <sub>IL</sub>	Low Level Input Voltage			0.7			0.8	V
I <sub>OH</sub>	High Level Output Current			−0.4			−0.4	mA
I <sub>OL</sub>	Low Level Output Current			4			8	mA
T <sub>A</sub>	Free Air Operating Temperature	−55		125	0		70	°C
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW Dn to CP	20			20			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW Dn to CP	5			5			ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time HIGH or LOW E̅ to CP	25			25			ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time HIGH or LOW E̅ to CP	5			5			ns
t <sub>w</sub> (L)	CP Pulse Width LOW	17			17			ns

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = Min, I <sub>I</sub> = −18 mA			−1.5	V
V <sub>OH</sub>	High Level Output Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max, V <sub>IL</sub> = Max	54LS	2.5		V
			DM74	2.7		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>CC</sub> Min, I <sub>OL</sub> = Max, V <sub>IH</sub> = Min	54LS		0.4	V
			DM74		0.5	
			DM74		0.4	
I <sub>I</sub>	Input Current @ Max Input Voltage	V <sub>CC</sub> = Max, V <sub>I</sub> = 10V			0.1	mA
I <sub>IH</sub>	High Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 2.7V			20	μA
I <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = Max, V <sub>I</sub> = 0.4V			−0.4	mA
I <sub>OS</sub>	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 2)	54LS	−20	−100	mA
			DM74	−20	−100	
I <sub>CC</sub>	Supply Current	V <sub>CC</sub> = Max			18	mA

Note 1: All typicals are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

## Switching Characteristics




$V_{CC} = +5.0V$ ,  $T_A = +25^\circ C$  (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\text{ k}\Omega$ , $C_L = 15\text{ pF}$		Units
		Min	Max	
$f_{max}$	Maximum Clock Frequency	30		MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CP to Qn		27	ns

## Functional Description

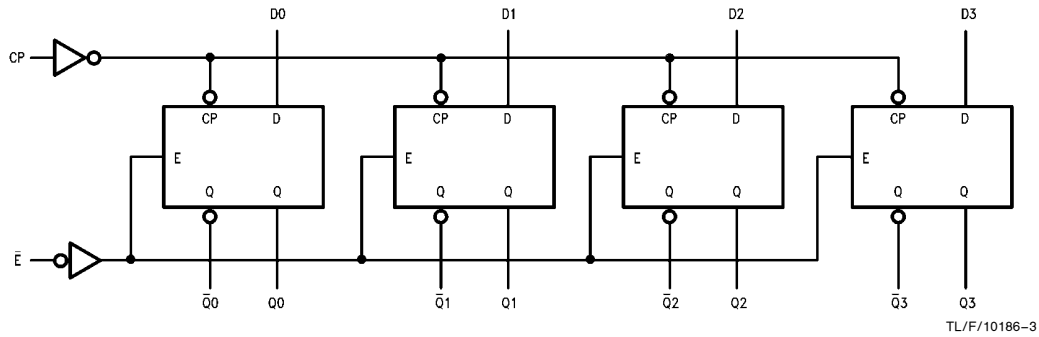
The LS379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and  $\bar{Q}$  outputs. The Clock (CP) and Enable ( $\bar{E}$ ) inputs are common to all flip-flops. When the  $\bar{E}$  input is HIGH, the register will retain the present data independent of the CP input. The Dn and  $\bar{E}$  inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

## Truth Table

Inputs			Outputs	
$\bar{E}$	CP	Dn	Qn	$\bar{Q}n$
H		X	No Change	No Change
L		H	H	L
L		L	L	H

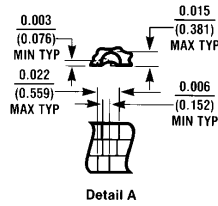
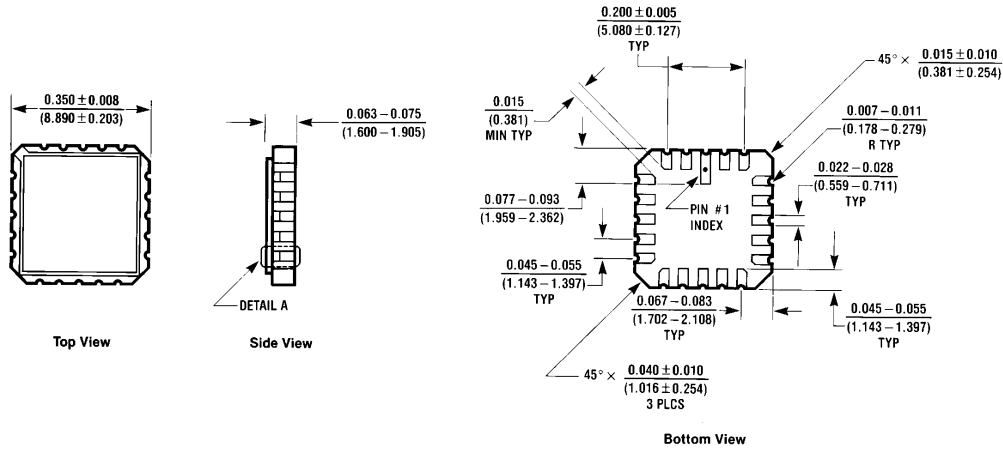
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## Logic Diagram



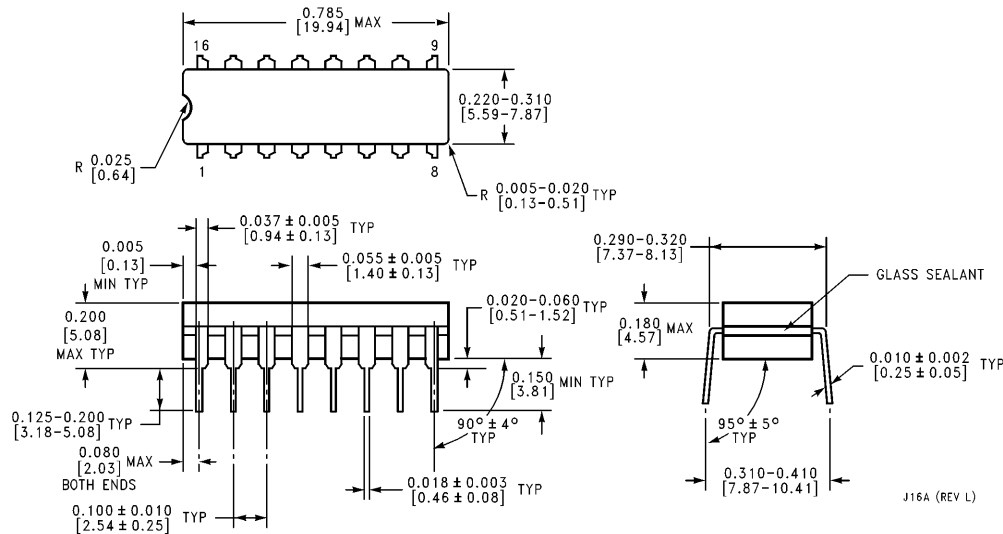
TL/F/10186-3

**Physical Dimensions** inches (millimeters)



**Ceramic Leadless Chip Carrier Package (E)**  
**Order Number 54LS379LMQB**  
**NS Package Number E20A**

E20A (REV D)



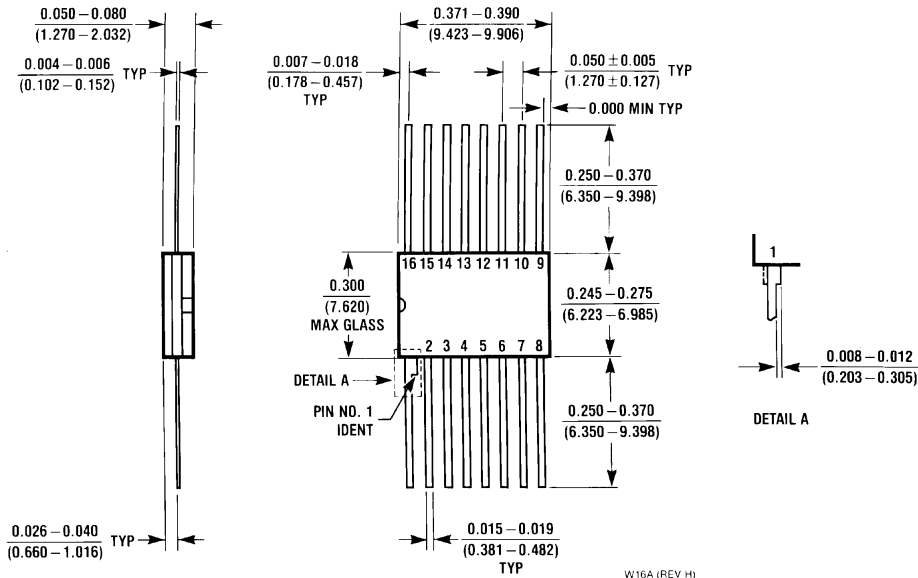
**16-Lead Ceramic Dual-In-Line Package (J)**  
**Order Number 54LS379DMQB**  
**NS Package Number J16A**

J16A (REV L)



**54LS379/DM74LS379 Quad Parallel Register with Enable**

**Physical Dimensions** inches (millimeters)



**16-Lead Ceramic Flat Package (W)**  
**Order Number 54LS379FMQB**  
**NS Package Number W16A**

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