三路模拟视频延迟线

概述

EL9115是三路模拟延迟线，可为3个信号提供斜率补偿。对由典型的CAT-5电缆（每对电线对有不同的电长度）引入的斜率，EL9115可提供非常好的补偿。

EL9115 可在每个通道上设置以 2ns 为步长增加，直到 62ns 的总延迟。

订购信息

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL9115IL	20-Pin QFN (5mm x 5mm)	-	MDP0046
EL9115IL-T7	20-Pin QFN (5mm x 5mm)	7"	MDP0046
EL9115IL-T13	20-Pin QFN (5mm x 5mm)	13"	MDP0046
EL9115ILZ (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	-	MDP0046
EL9115ILZ-T7 (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	7"	MDP0046
EL9115ILZ-T13 (See Note)	20-Pin QFN (5mm x 5mm) (Pb-Free)	13"	MDP0046

注：Intersil无铅产品采用特殊的无铅材料制成，模塑料／晶片的附属材料和100%无光泽锡盘引脚符合RoHS标准，兼容SnPb和无铅低温焊接操作。Intersil无铅产品在无铅峰值回流温度中属于MSL级别分类，完全满足和超过IPC/GEDEC JSTD-020的无铅要求。

特点

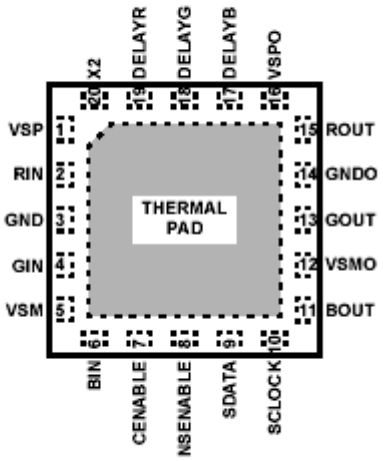
- 62ns 的总延迟
- 步长为 2ns 的延迟增量
- 工作电源为±5V
- 高达 100MHz 的带宽
- 低功耗
- 20 引脚 QFN（5mm×5mm）封装
- 无铅(符合 RoHS 标准)

应用

- RGB 信号斜率（延时）控制
- 模拟信号传播调整

管脚引出线图

EL9115
[20-PIN QFN (5mm x 5mm)]
TOP VIEW



EXPOSED DIEPLATE SHOULD BE CONNECTED TO -5V

极限参数

电源电压（V_S^+到V_S^-）……12V
最大输出电流…… ±60mA
储存温度范围…… -65℃到+150℃
工作结点温度……+135℃
工作环境温度……-40℃到+85℃

注意：强度超出所列的极限参数可能导致器件的永久性损坏。这些仅仅是极限参数，并不意味着在极限条件下或在任何其它超出推荐工作条件所示参数的情况下器件能有效工作。

重要提示：所有具有最小/最大值的参数都是有保证的。典型值仅作为信息提供。除非另有说明，所有的测试都在规定的温度下进行，且为脉冲测试，因此：$T_J=T_C=T_A$。

直流电电气指标

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V+	Positive Supply Range		+4.5		+5.5	V
V-	Negative Supply Range		-4.5		-5.5	V
G_0	Gain Zero Delay	X2 = 5V, 150Ω load	1.81	1.89	2.04	
G_m	Gain Mid Delay		1.66	1.84	2.04	
G_f	Gain Full Delay		1.52	1.79	2.04	
DG_m0	Difference in Gain, 0 - Mid		-7.5	-2.5	2.5	%
DG_f0	Difference in Gain, 0 - Full		-13.5	-6.0	2.5	%
DG_fm	Difference in Gain, Mid - Full		-10.0	-2.6	4.0	%
V_{IN}	Input Voltage Range	Gain falls to 90% of nominal	-0.7		1.3	V
V_{OUT}	Output Voltage Range	X2 = +5V into 150Ω load	-5		1.6	V
I_B	Input Bias Current			1	5	µA
R_{IN}	Input Resistance			10		MΩ
V_{OS_0}	Output Offset 0 Delay	X2 = +5V, 75 + 75Ω load	-200	-150	60	mV
V_{OS_M}	Output Offset full Delay		-200	-140	60	mV
V_{OS_F}	Output Offset mid Delay		-200	-130	60	mV
Z_{OUT}	Output Impedance	Chip enable = +5V	4.54	4.81	5.09	Ω
		Chip enable = 0V		1		MΩ
PSR+	Rejection of Positive Supply	X2 = +5V into 75 + 75Ω load		-38.8		dB
PSR-	Rejection of Negative Supply	X2 = +5V into 75 + 75Ω load		-52.98		dB
I_{SP}	Supply Current (Note 1)	Chip enable = +5V current on V_{SP}	75	87	115	mA
I_{SM}	Supply Current (Note 1)	Chip enable = +5V current in V_{SM}	-10.5	-8.64	-7	mA
I_{SMO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SMO}	-13	-11.66	-10	mA
I_{SPO}	Supply Current (Note 1)	Chip enable = +5V current in V_{SPO}	10	11.86	15.5	
$I_{SP\ \Delta}$	Supply Current (Note 1)	Increase in I_{SP}/I_{SM} for unit step in delay		0.9		mA
$I_{SP\ OFF}$	Supply Current (Note 1)	Chip enable = 0V current in V_{SP}		1.63		mA
I_O	Output Drive Current	10Ω load, 0.5V drive, X2 = 5V	30			mA
I_{CP}	Charge Pump Current			50		µA
L_{HI}	Logic High	Switch high threshold		1.25	1.6	V
L_{LO}	Logic Low	Switch low threshold	0.8	1.15		V

注：1. 所有的供电电流在延迟 R=0ns,G=mid delay,B=full delay 下测得。

交流电电气指标

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3 dB Bandwidth					
BW 0.1dB	0.1dB Bandwidth					
SR	Slew Rate					
T_R - T_F	Transient Response Time	20% - 80%, for all delays, 1V step, EL9115		2.5		ns
V_{OVER}	Voltage Overshoot	for any delay, response to 1V step input		5	10	%
Glitch	Switching Glitch	Time for o/p to settle after last s_clock edge		100		ns
THD	Total Harmonic Distortion	$1V_{PP}$ 10MHz sinewave, offset by +0.2V at mid delay setting		-50	-40	dB
X_T	Hostile Crosstalk	Stimulate G, measure R/B at 1MHz		-78		dB
V_N	Output Noise	Gain X2, measured at 75Ω load with		2.5		mV rms
d_T	Delay Increment		1.75	2	2.25	ns
T_{MAX}	Maximum Delay		55	62	70	ns
D_{ELDT}	Delay Diff Between Channels			1.6		%
t_{PD}	Propagation Delay	Measured input to output	8.5	9.8	11	ns
T_{MAX}	Max s_clock Frequency	Maximum programming clock speed			10	MHz
T_en_ck	Minimum Separation Between Serial Enable and Clock	Check enable low edge can occur after T_en_ck of previous (ignored) clock and up to before T_en_ck of next (wanted) clock		10		ns

引脚描述

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VSP	+5V for delay circuitry and input amp
2	RIN	Red channel input, ref GND
3	GND	0V for delay circuitry and input amp
4	GIN	Green channel input, ref GND
5	VSM	-5V for input amp
6	BIN	Blue channel input, ref GND
7	CENABLE	Chip enable logical +5V enables chip
8	NSENABLE	$\overline{\text{ENABLE}}$ for serial input; enable on low
9	SDATA	Data into registers; logic threshold 1.2V
10	SCLOCK	Clock to enter data; logical; data written on negative edge
11	BOUT	Blue channel output, ref GND_O
12	VSMO	-5V for output buffers
13	GOUT	Green channel output, ref GND_O
14	GNDO	0V reference for output buffers
15	ROUT	Red channel output, ref GND_O
16	VSPO	+5V for output buffers
17	TESTB	Blue channel phase detector output
18	TESTG	Green channel phase detector output
19	TESTR	Red channel phase detector output
20	X2	Sets gain to 2X if input high; X1 otherwise
Thermal Pad		Must be connected to V_{CC}

TABLE 1. SERIAL BUS DATA

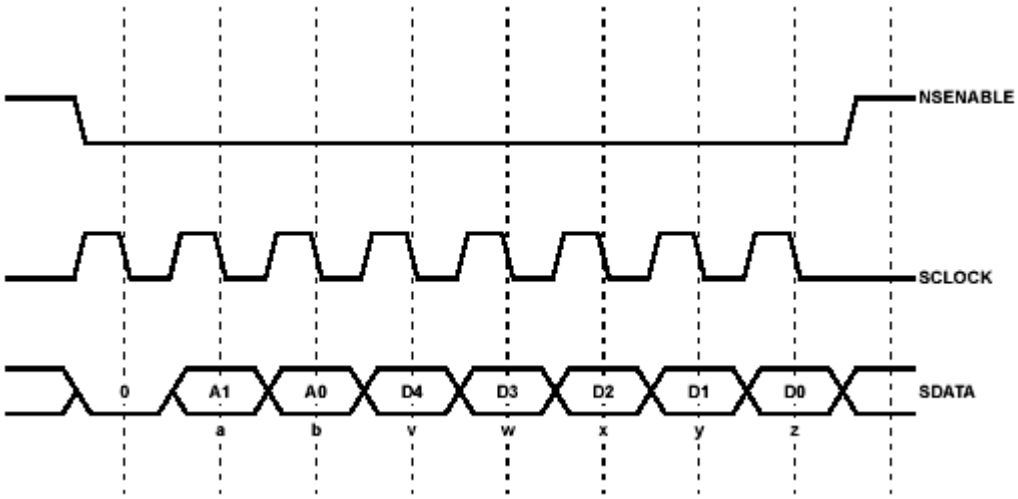
vwxyz	Delay
00000	0
00001	2
00010	4
00011	6
00100	8
00101	10
00110	12
00111	14
01000	16
01001	18
01010	20
01011	22
01100	24
01101	26
01110	28
01111	30
10000	32
10001	34
10010	36
10011	38
10100	40
10101	42
10110	44
10111	46
11000	48
11001	50
11010	52
11011	54
11100	56
11101	58
11110	60
11111	62

NOTES:

Delay register word = 0abvwxyz
Red register - ab = 01
Green register - ab = 10
Blue register - ab = 11
vwxyz selects delay

串行总线操作

NSEnable 脚变为低电平后，在第一个时钟下降沿从 DATA 读取输入数据。DATAT 应为 0 电平（写入寄存器），READ 无效。在随后的下降沿读取紧接着的两个数据位并译码，以填入寄存器，其中 Reg 01=R,02=G,03=B,00 作测试用。读取接下来的 5 个数据位送入寄存器。时钟应停止。NSEnable 变为高电平，数据传送结束。（如果时钟由 NSEnable 脚选通，则可连续工作）。上电时所有寄存器的初始值为 0。



声明：本资料仅供参考。如有不同之处，请以相应英文资料为准。