基于新型控制器FAN7535的高功率因数32W双管荧光灯电子镇流器

摘要：飞兆半导体公司推出的FAN7535单片IC，是一种集PFC控制器和镇流器控制器于一个芯片上的“二合一”器件，能为电子镇流器提供高于0.98的功率因数、低于10%的输入电流THD及预热和保护功能，控制参数可编程。文中介绍了FAN7535的结构和特点，给出了由其组成的32W×2荧光灯电子镇流器电路。

关键词：FAN7530；PFC；镇流器；预热；ZVS；参数可编程

1 前言

荧光灯电子镇流器如果只采用常规整流滤波电路而不带功率因数校正（PFC），由于桥式整流器输出端大容量（10~100μF/400V）电容器上的充放电电压比较平滑，整流二极管在交流（AC）市电电压每个半周期之内，只是在AC电压峰值附近才会导通。虽然桥式整流器输入端的AC电压是正弦波，但AC输入电流则为尖峰脉冲，发生严重畸变，将对电网造成污染，并且线路功率因数仅约0.5~0.6，造成电能的利用率很低。为此，IEC1000-3-2、EN61000-3-2和我国国家标准GB17625.1-1998等对照明电器（尤其是25W以上）和输入电流谐波含量都有限制要求，例如2次谐波不大于2%（以电流基波为100%），3次谐波不大于0.3λ（λ为功率因数），5次谐波不大于10%等。如果25W以上的照明电器不符合标准规定要求，则不能进入市场尤其是国际市场。

欲使照明电器尤其是电子镇流器能符合规范要求，就必须采用PFC措施。以往带PFC的电子镇流器通常要使用两片IC，其中一块是PFC控制器，另一块是镇流器控制器。美国飞兆半导体推出的FAN7535，将PFC控制器和镇流器控制器集成到同一芯片上和同一封装内，从而可减少外部元件数量及印制电路板（PCB）尺寸，缩短设计周期。

2 FAN7535的结构与特点

2.1 FAN7535封装和引脚功能

FAN7535采用24引脚SOP封装，引脚排列如图1所示。在图1中，左半部分为PFC控制器，右半部分为镇流器控制器；⑦脚为接地端，为两个控制器公用。除了接地端外，每个控制器的有效引脚均为7个，功能如附表所示。

2.2 FAN7535内部电路

FAN7535芯片电路含有一个PFC控制器和一个镇流器控制与半桥驱动器。

2.2.1 PFC控制器电路

FAN7535的PFC控制器由零电流检测

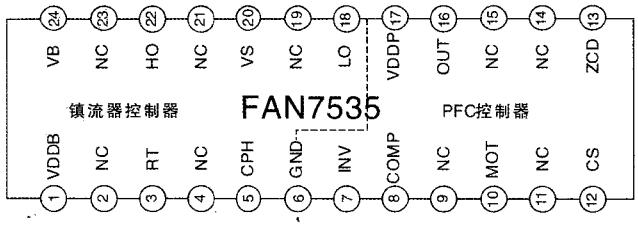

图1 FAN7535引脚排列

附表 FAN7535引脚功能

引脚号	名称	功能	引脚号	名称	功能
1	VDDB	镇流器部分电源电压端	12	CS	PFC过电流保护比较器输入端
2,4,9,11,14,15,19,21,23	NC	未连接端	13	ZCD	PFC零电流检测电路输入端
3	RT	振荡器频率设置电阻连接端	16	OUT	PFC驱动器输出端
5	CPH	预热时间设置电阻连接端	17	VDDP	PFC部分电源电压输入端
6	GND	PFC和镇流器部分接地端	18	LO	镇流器半桥低端驱动器输出端
7	INV	PFC误差放大器反相输入端	20	VS	镇流器部分高端浮置电源地
8	COMP	PFC误差放大器输出端	22	HO	镇流器半桥高端驱动器输出端
10	MOT	内部斜坡信号斜率设置端	24	VB	镇流器部分高端浮置电源

（ZCD）比较器、锯齿波产生器、过电流保护（OCP）比较器、误差放大器、过电压保护（OVP）比较器和输出驱动器等组成，如图2所示。

FAN7535⑫脚（VDDP）内置一个22V的齐纳二极管，启动门限是12V，欠压关闭门限为8.5V，启动电流为40μA，静态工作电流为1.5mA，驱动输出电流达+500mA/-800mA，适用功率达300W以上。

图2所示的PFC控制器不含乘法器，⑩脚内部电路起乘法器的作用，该脚外部电阻设定最大导通电压和导通时间。与带乘法器的传统PFC控制器比较，有更低的AC输入电流总谐波失真（THD）。

2.2.2 镇流器控制器与半桥驱动器

FAN7535的镇流器控制与半桥驱动器电路如图3所示。该电路与飞兆半导体的FAN7711是等效的，其①脚（VDDB）内置一个15.2V的齐纳钳位二极管，①脚上的启动门限是13.4V，启动电流为150μA，动态工作电源电流为3.2mA，驱动器输出电流达+350mA/-650mA。

FAN7535中的镇流器控制与驱动电路含有一个振荡器，灯丝预热时间由⑤脚上的外接电容来编程，预热频率和运行频率由IC③脚上的外接电阻设置。这部分电路还含有有源零电压开关（AZVS）控制单元，其作用是减小外部功率MOSFET的开关损耗。

3 基于FAN7535的32W双灯管电子镇流器电路

图4所示为采用FAN7535设计的32W×2荧光灯电子镇流器电路。为了便于理解，特将FAN7535的PFC控制器和镇流器控制器分开。

3.1 电路组成

图4所示电路由4部分组成，即：①C_1、C_2和C_3、C_4及LF_1组成输入EMI滤波器，RV_1为470V的压敏电阻，RT_1为NTC热敏电阻；②UR_1为桥式整流器；③FAN7535的PFC控制器、PFC开关VT_1、电感器L_1、二极管VD_2、输入电容C_3、输出电容C_9等，组成有源功率因数校正（APFC）升压变换器；④FAN7535的镇流器控制器及VT_2、VT_3及L_2、C_{56}和L_3、C_{58}组成的谐振输出级等，构成半桥式镇流器电路。

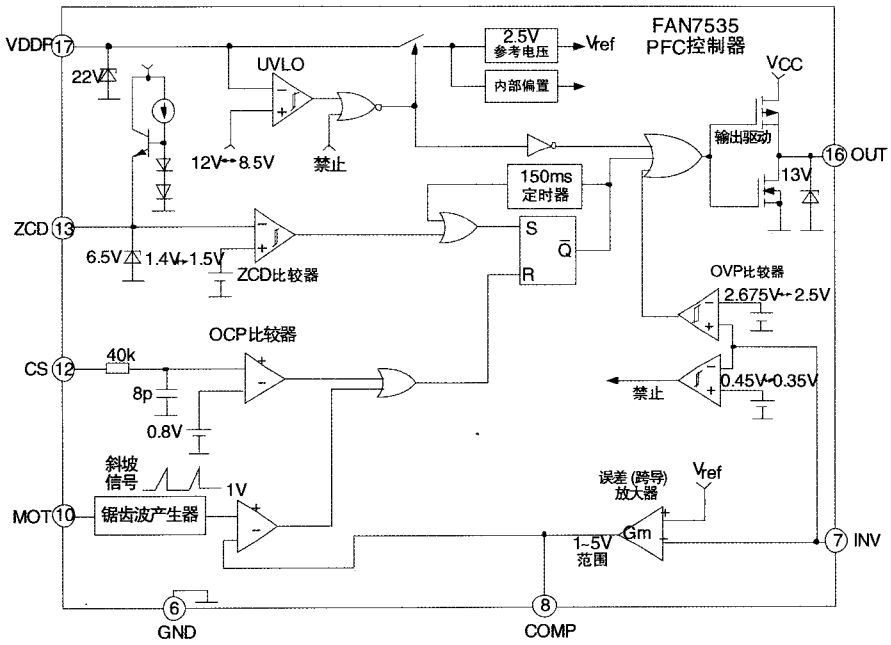

图2 FAN7535的PFC控制器电路框图

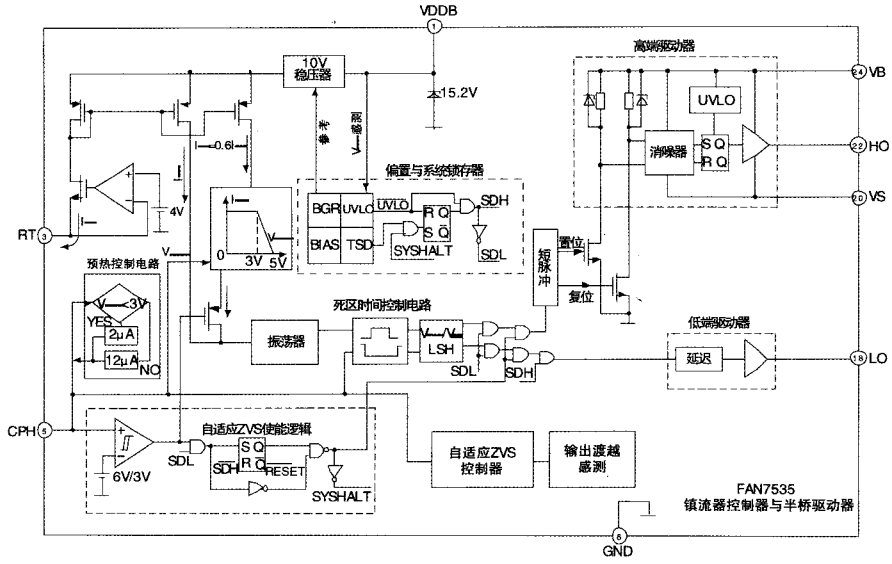

图3 FAN7535的镇流器控制与半桥驱动器电路框图

阻R_3对电容C_6充电。一旦IC（FAN7535）⑰脚上的电压超过12V的门限，IC⑰脚导通，IC中的PFC控制器启动，IC⑯脚上的输出驱动VT_1开始操作。当APFC升压变换器开始运行时，L_1的副绕组、R_4、C_{10}、二极管VD_3、稳压管VS_1（18V）、C_6组成的辅助电源则为IC⑰脚供电，因而启动电阻R_3上的功率损耗极小。

电阻分压器R_{10}/R_{11}用作感测PFC输出电压，以履行输出电压调节。R_{11}上的采样电压经IC⑰脚输入到内部误差放大器反相端，IC⑧脚上的R_8、C_7、C_8为误差放大器输出端上的补偿网络。IC⑦脚上的门限电平为2.5V，因此APFC升压变换器输出DC电压$V_{O\ (PFC)}$为

$$V_{O(PFC)}=2.5V\times(1+R_{10}/R_{11})=2.5V\times(1+2M/12.6k)\approx400V$$

无论AC输入电压在90V~264V范围内怎样变化，APFC输出电压总是稳定在400V上，这与开关电源的稳压原理是完全一样的。

3.2 电路工作原理

3.2.1 APFC升压变换器电路工作原理

接通交流（AC）电源，桥式整流器（UR_1）输出经二极管VD_1对PFC输出电容C_9充电，输入端上的热敏电阻（NTC）RT_1对充电时的浪涌电流起限制作用。C_9上的充电电压很快达到整流电压的峰值。由于充电电流不经过电感器L_1，所以在PFC电路开始操作前L_1中没有能量储存。

在通电后，整流电压同时通过PFC启动电

VT_1源极上串联的R_7，是电流传感电阻。只要IC⑫脚上的电压超过0.8V的门限，过电流保护（OCP）电路则使能，IC关闭其输出。

IC⑩脚上的电阻设置内部锯齿波的斜率和MOSFET（VT_1）的最大导通时间。L_1的副绕组还作为传感器使用，为IC⑬脚提供零电流检测（ZCD）信号，以保证L_1电流降为零时开始下一

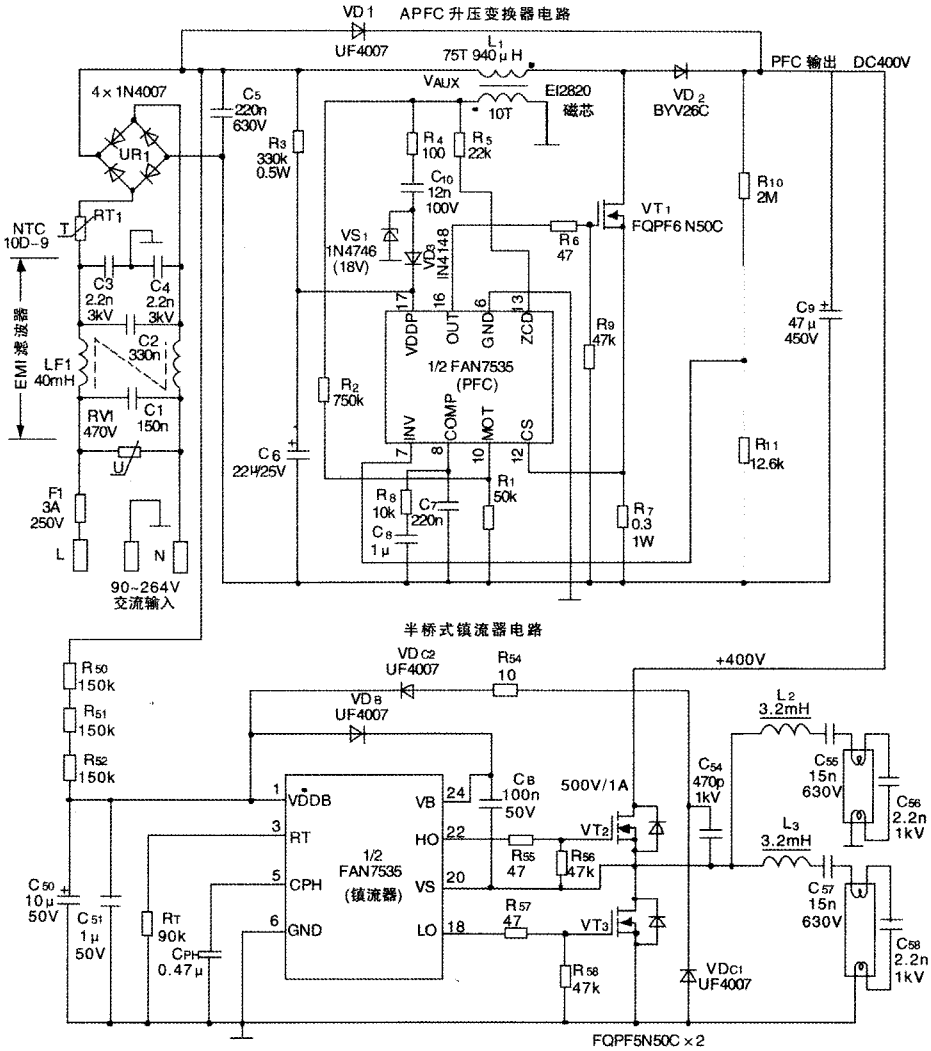

图4 采用FAN7535的32W双灯管电子镇流器电路

个开关周期。

当VT_1导通时，二极管VD_2截止，通过L_1的电流I_{L1}从零开始线性增长。一旦I_{L1}达到峰值，VT_1则关断，L_1中的储能使VD_2导通，L_1放电，电流线性减小。一旦I_{L1}降为零，VT_1再次导通，开始下一个开关周期。

每个开关周期中的I_{L1}呈高频三角波，其峰值都跟踪AC输入电压（Vin）的瞬时变化。高频电流I_{L1}经输入电容C_5（220nF）滤除高频成分，则复原为正弦工频（50Hz/60Hz）电流波形，如图5所示。

FAN7525的PFC控制器工作在临界导电模式（CRM），由其组成的APFC升压变换器的作用是：

（1）在桥式整流器输入端产生非失真的正弦AC电流，输入AC电流谐波符合IEC1000-3-2等标准的规定限制，THD可以小于10%。

（2）由于AC输入电流与电压趋于同相位，因此线路功率因数λ>0.98，在高线路电压上λ可达0.995，几乎等于1。

（3）在国际通用AC线路电压（90~264V）下，不需要电源选择开关，可以得到400V的稳定DC输出电压，作为镇流器电路的DC总线电压，可使灯管稳定工作，保持在不变的亮度电平上。输出电压$V_{O(PFC)}$纹波很小，频率为AC电源频率（50Hz/60Hz）的2倍。

3.2.2 镇流器电路工作原理

图4所示下半部分为半桥式镇流器电路。在系统通电后，整流后的电压经启动电阻R_{50}、R_{51}、R_{52}对电容C_{50}充电。当IC①脚（VDDB）上的电压超过13.2V的启动门限时，①脚导通，㉒脚和⑱脚上的输出驱动半桥两个MOSFET（VT_2、VT_3）交替导通，半桥逆变电路开始工作。一旦半桥开始工作，IC①脚则由C_{54}、二极管VD_{C1}和VD_{C2}、电阻R_{54}组成的电荷泵辅助电源供电，这样就大大降低了启动电阻R_{50}、R_{51}和R_{52}上的功率损耗。启动电阻由三个电阻串联，可以承受较高的电压。连接在IC①脚与㉔脚之间的自举二极管VD_B和连接在IC㉔脚与⑳脚之间的自举电容C_B，用作为IC㉔脚内部的高端驱动器供电。IC⑱脚内部的低端驱动器，则由①脚上的电压V_{DDB}供电。

IC的镇流器控制器有5种工作模式，在不同模式时的IC引脚CPH（⑤脚）上的电压V_{CPH}、工作频率f和死区时间t_{DT}如图6所示。

（1）灯丝预热模式

在IC导通振荡器启动之后，一个2μA的电流从IC⑤脚上流出对电容C_{PH}充电，IC输出预热频率f_{PH}对灯丝加热。C_{PH}上的电压V_{CPH}从0V至3V所需要的时间t_{PH}（即t_0~t_1），即为预热时间，其值为

$$t_{PH}=3\times C_{PH}/2\mu A=3\times 0.47\mu F/2\mu A=0.7s$$

预热频率f_{PH}由IC③脚上的电阻R_T确定，其值为

$$f_{PH}=1.6\times(4\times 10^9/R_T)=1.6\times(4\times 10^9/90k\Omega)=71KHz$$

（2）灯触发（即点火）模式

预热结束后，频率从f_{PH}向运行频率f_{RUN}斜偏，V_{CPH}从3V继续升高。在频率线性降低扫描过程中，当接近或等于镇流器高Q值的谐振输出级的固有频率时，L_2、C_{56}和L_3、C_{58}等串联谐振电路将发生谐振，在C_{56}、C_{58}上产生800~1500V的谐振电压加在灯管两端，对灯进行触发。V_{CPH}从3V升至5V所需要的时间t_{IGN}（即t_1~t_2），则为触发时间。由于在触发模式，C_{PH}上的充电电流为12μA，触发时间为：

$$t_{IGN}=2\times(C_{PH}/12\mu A)=2\times(0.47\mu F/12\mu A)=78ms$$

（3）运行（正常点燃）模式

灯一旦被成功触发，IC进入运行模式。运行频率f_{RUN}比预热频率f_{RUN}低1.6倍，因此可得：

$$f_{RUN}=f_{PH}/1.6=71kHz/1.6\approx 44.4kHz$$

（4）有源零电压开关（AZVS）模式

当$V_{CPH}\geqslant 6V$时，AZVS控制电路使能，可自适应ZVS，从而有最小的开关损耗和热损耗。

（5）关闭模式

如果使$V_{CPH}<2.6V$，例如在IC③脚外部连接一个NPN晶体管（发射极接地，集电极接IC③脚），当在其基极加一个逻辑高电平信号时，晶体管导通，此时$V_{CPH}\leqslant 2.6V$，IC则进入关闭模式。

FAN7535不需外加专门电路，能自动检测灯开路故障，对功率MOSFET提供保护。若芯片结温超过165°，IC将进入关闭模式，仅消耗250μA的微电流。

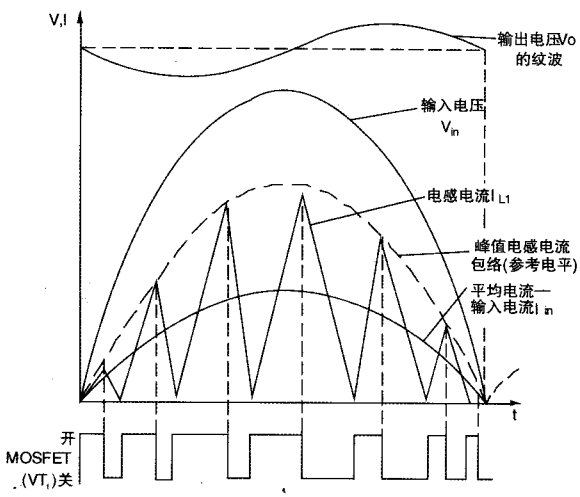

图5 CRM-PFC变换器的相关电压和电流波形

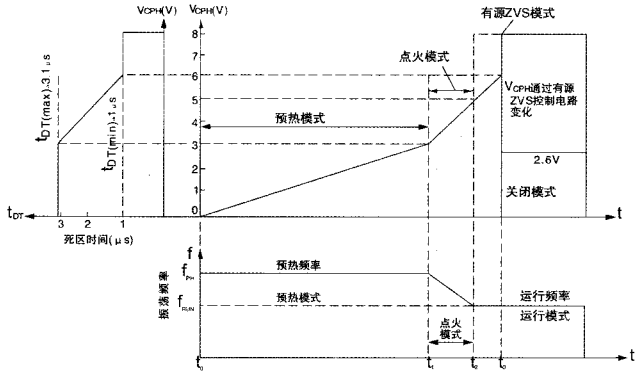

图6 不同工作模式FAN7535引脚CPH上的电压、频率及死区时间

3.3 主要元件的选择

（1）PFC启动电阻R_3的选择

R_3应保证在最低AC输入电压下$V_{in(min)}$=90V下，能提供足够的启动电流。PFC控制器的最大启动电流$I_{st(max)}$=70μA，IC脚VDDP上的启动门限最大值V_{th}=13V，R_3值应满足：

$$R_3 \le \frac{V_{in(\min)} \times \sqrt{2} - V_{th}}{I_{st(\max)}} = \frac{90V \times \sqrt{2} - 13V}{70\mu A} = 1.63M\Omega$$

R_3的功耗不大于0.5W，即

$$P_{R3} = \frac{V_{in(\max)}^2}{R_3} \le 0.5W$$

即 $$R_3 \ge \frac{(264V)^2}{0.5W} = 139K\Omega$$

由于139kΩ≤R_3≤1.63MΩ，可以选择R_3=330 kΩ。

（2）镇流器控制器启动电阻的选择

IC脚1（VDDB）上的最大启动门限是14.4V，启动电流为150μA，因此

$$Rst \le \frac{90V \times \sqrt{2} - 14.4V}{150\mu A} = 733k\Omega$$

启动电阻功耗可以不大于1W，因此

$$Rst \ge \frac{(264V)^2}{1W} = 69.7k\Omega$$

由于69.7kΩ≤Rst≤733kΩ，可以选择Rst=450 kΩ。Rst可用3个0.25W的150 kΩ电阻串联，即Rst=R_{50}+R_{51}+R_{52}=150 kΩ×3=450 kΩ。

（3）电感元件的选择

电感元件是比较关键的元件，必须精心设计，正确选择。

LF_1电感值为40mH，L_1采用EI2820磁心，初级75匝，电感值为0.94mH，次级10匝。L_2、L_3均采用EI2820磁心，绕组共130匝，电感值为3.2mH。因篇幅所限，计算过程从略。

4 结束语

FAN7535型PFC与镇流器控制IC，为设计高功率因数、低输入电流THD和高性能、高可靠荧光灯电子镇流器提供了单芯片解决方案。基于FAN7535的荧光灯电子镇流器，输入电流谐波完全符合相关标准的限量要求，可以进入国际市场。这种镇流器提供灯丝预热和过电压、过电流、过热保护，并且预热时间、预热频率、灯触发时间和运行频率均可根据需要由一个电容（C_{PH}）和一个电阻（R_T）进行编程。

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FAN7535
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Features

- PFC, Ballast Control, and Half-Bridge Driver in One IC
- PFC Driver Current Capability: +500mA/-800mA
- Critical Conduction Mode Control Type PFC
- Internal Clamping Zener Diode (PFC): 23V
- Under-Voltage Lockout with 3.5V of Hysteresis (PFC)
- Internal Clamping Zener Diode (Ballast): 15V
- Lower di/dt Gate Driver for Better Noise Immunity
- Under-Voltage Lockout with 1.8V Hysteresis (Ballast)
- Ballast Driver Current Capability: +350mA/-650mA
- Programmable Preheat Time & Frequency
- Programmable Run Frequency
- Programmable Ignition Sweep Time
- Internal Active ZVS Control
- Internal Protection Function (Latch Mode)

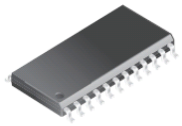
Applications

- Fluorescent Lamp Ballast

Description

FAN7535 provides simple, high-performance, active power factor correction (PFC), and ballast control. The FAN7535 is optimized for all kinds of fluorescent lamps, which require minimum board area and reduced external components. The FAN7535 PFC control block to reduce the input current THD lower than conventional CRM boost PFC methods. An innovative Active Zero Voltage Switching (AZVS) block reduces the swtiching power loss. A dedicated timing section in the FAN7535 allows the user set the necessary parameters for proper lamp preheat and ignition.

24-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN7535M	24-SOP	-25°C ~ 125°C	Tube
FAN7535MX			Tape & Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Typical Application Diagrams

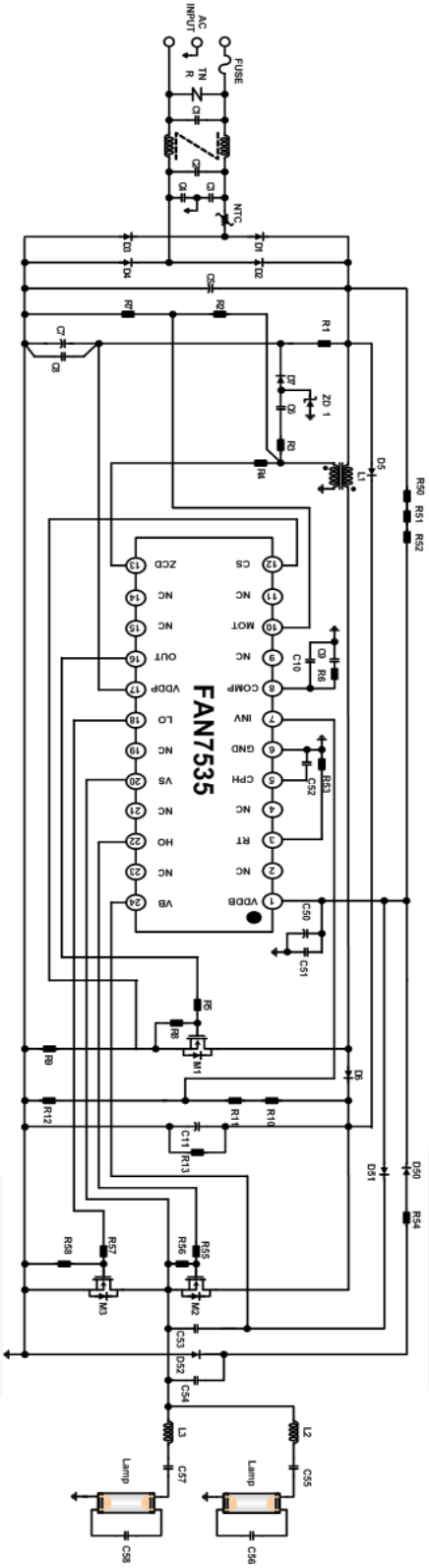


Figure 1. Typical Application Circuit for Fluorescent Lamp

Internal Block Diagram

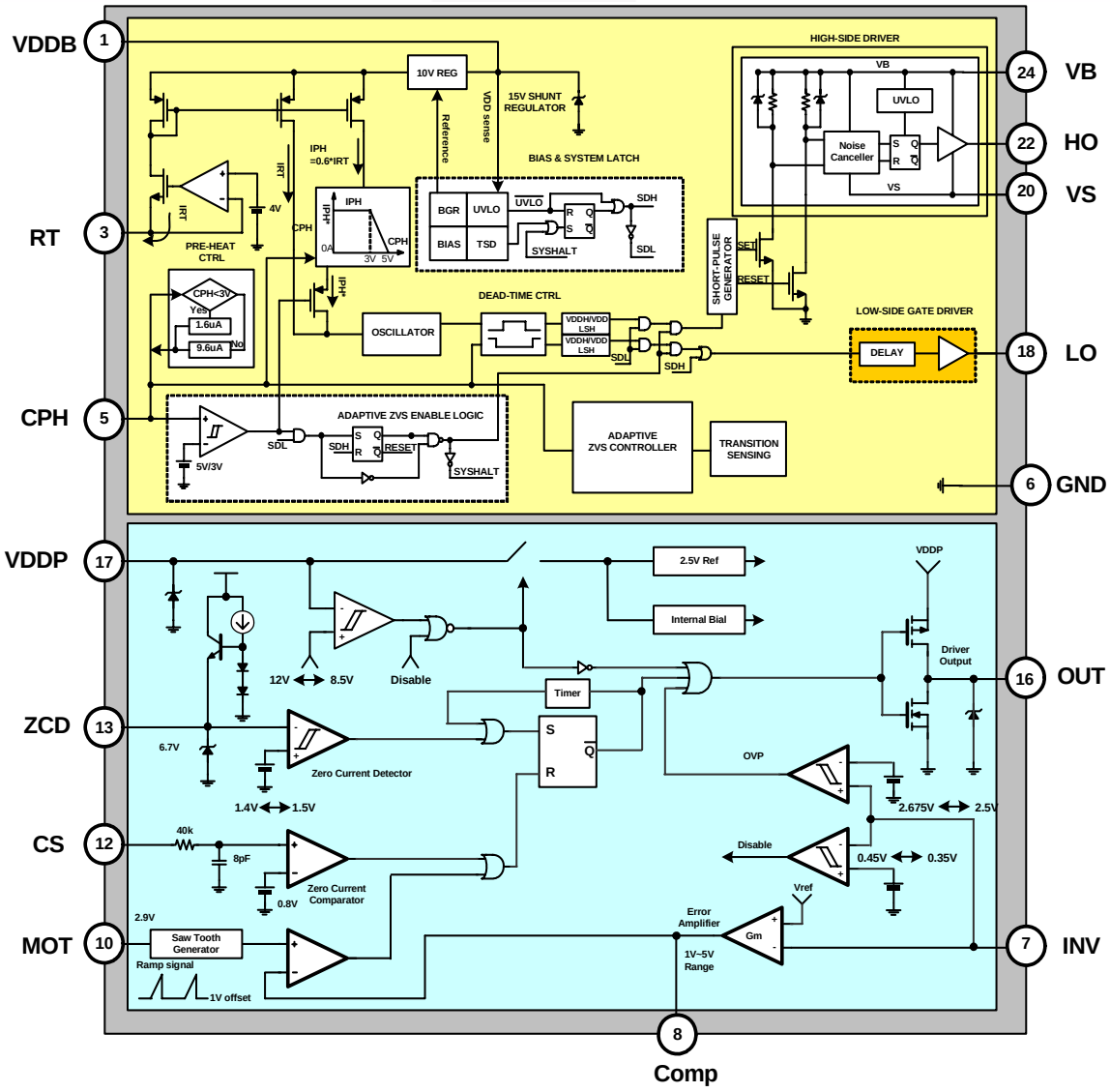


Figure 2. Functional Block Diagram (2chips-1PKG)

Pin Configuration

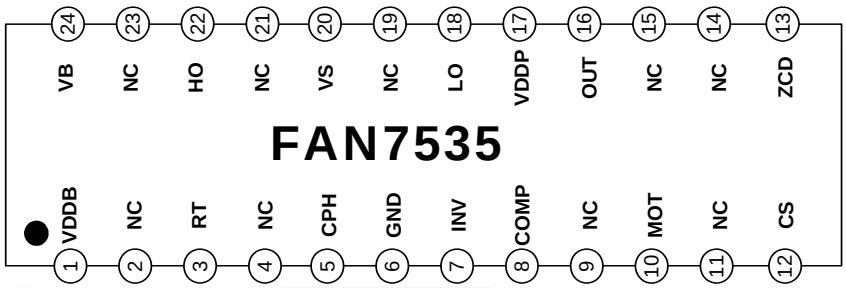


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	VDDB	Supply voltage for ballast part
2	NC	No connection
3	RT	Oscillator frequency set resistor
4	NC	No connection
5	CPH	Preheating time set capacitor
6	GND	Ground for ballast part & PFC part
7	INV	Inverting input of the error amplifier
8	COMP	Output of the transconductance error amplifier
9	NC	No connection
10	MOT	Set the slope of the internal ramp
11	NC	No connection
12	CS	Input of the over-current protection comparator
13	ZCD	Input of the zero current detection block
14	NC	No connection
15	NC	No connection
16	OUT	Gate driver output
17	VDDP	Supply voltage for PFC block
18	LO	Low-side output
19	NC	No connection
20	VS	High-side floating supply return
21	NC	No connection
22	HO	High-side output
23	NC	No connection
24	VB	High-side floating supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability.

The absolute maximum ratings are stress ratings only. T_A=25°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
PFC PART					
V_{DDP}	Supply Voltage		Vz		V
I_{OH}, I_{OL}	Peak Drive Output Current	-800		+500	mA
I_{CLAMP}	Driver Output Clamping Diodes $V_O > V_{CC}$ or $V_O < -0.3V$		±10		
I_{DET}	Detector Clamping Diodes		±10		
V_{IN}	Error Amplifier, MOT, CS Input Voltages	-0.3		6.0	V
BALLAST PART					
V_B	High-side Floating Supply	-0.3		625.0	V
V_S	High-side floating supply return	-0.3		600.0	
V_{IN}	RT, CPH Pins Input Voltage	-0.3		8.0	
V_{CL}	Clamping Voltage		V_{CL}		
I_{CL}	Clamping Current Level		25		mA
dV_S/dt	Allowable Offset Voltage Slew Rate			50	V/ns
Common					
T_{OPR}	Operating Temperature Range	-25		+125	°C
T_{STG}	Storage Temperature Range	-65		+150	
P_D	Total Power Dissipation		1.5		W
θ_{JA}	Thermal Resistance (Junction-to-Air)			83	°C/W

Caution:

Do not supply a low-impedance voltage source to the internal clamping Zener diode between the GND and the VDDB and VDDP pins of this device. Use a common supply between the two ICs (PFC, Ballast) only under careful attention.

Electrical Characteristics

V_{DDP}=14V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
PFC PART(1)						
UNDER-VOLTAGE LOCKOUT SECTION						
$V_{th(start)}$	Start Threshold Voltage	V_{DDP} Increasing	11	12	13	V
$V_{th(stop)}$	Stop Threshold Voltage	V_{DDP} Decreasing	7.5	8.5	9.5	
$H_{Y(UVLO)}$	UVLO Hysteresis		3.0	3.5	4.0	
Vz	Zener Voltage	I_{DDP} = 20mA	20	22	24	
SUPPLY CURRENT SECTION						
I_{st}	Start-up Supply Current	V_{DDP} = $V_{TH(START)}$ -0.2V		40	70	mA
I_{DDP}	Operating Supply Current	Output not switching		1.5	3.0	mA
$I_{DDP(dyn)}$	Dynamic Operating Supply Current	50kHz, C_L = 1nF		2.5	4.0	
$I_{DD(dis)}$	Operating Current at Disable	V_{INV} = 0V	20	65	95	mA
ERROR AMPLIFIER SECTION						
V_{ref1}	Voltage Feedback Input Threshold1	T_A = 25°C	2.465	2.500	2.535	V
DV_{ref1}	Line Regulation	14V ≤ V_{DDP} ≤ 20V		0.1	10.0	mV
DV_{ref3}(1)	Temperature Stability of V_{REF}			20		
$Ib_{(ea)}$	Input Bias Current	1V ≤ V_{inv} ≤ 4V	-0.5		0.5	mA
I_{source}	Output Source Current	V_{inv} = V_{ref1}-0.1V		-12		
I_{sink}	Output Sink Current	V_{inv} = V_{ref1}+0.1V		12		
$V_{eao(H)}$	Output Upper Clamp Voltage	V_{inv} = V_{ref1}-0.1V	5.4	6.0	6.6	V
$V_{eao(Z)}$	Zero Duty Cycle Output Voltage		0.9	1.0	1.1	
g_m(2)	Transconductance		90	115	140	µmho
MAXIMUM ON-TIME SECTION						
V_{MOT}	Maximum On-Time Voltage	R_{MOT} = 40.5Ω	2.784	2.900	3.016	V
T_{ON-MAX}	Maximum On-Time Programming	R_{MOT} = 40.5Ω,T_A = 25°C	19	24	29	µs
CURRENT-SENSE SECTION						
$V_{CS(LIMIT)}$	Current Sense Input Threshold Voltage Limit		0.7	0.8	0.9	V
$Ib_{(cs)}$	Input Bias Current	0V ≤ V_{CS} ≤ 1V	-1.0	-0.1	1.0	mA
$Td_{(cs)}$(1)	Current Sense Delay to Output			350	500	ns

Notes:

1. Please refer to the FAN7529 datasheet and AN-6026 application note for more detailed information. Available on Fairchild's website at:

   Datasheet: http://www.fairchildsemi.com/ds/FA%2FFAN7529.pdf

   Application Note: http://www.fairchildsemi.com/an/AN/AN-6026.pdf

2. This parameter, although guaranteed, is not 100% tested in production.

Electrical Characteristics (Continued)

V_{DDP} = 14V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
ZERO CURRENT DETECT SECTION						
$V_{th(ZCD)}$ (3)	Input Voltage Threshold		1.35	1.50	1.65	V
$HY_{(ZCD)}$ (3)	Detect Hysteresis		0.05	0.10	0.15	
$V_{clamp(h)}$	Input High Clamp Voltage	I_{DET} = 3mA	6.0	6.7	7.4	
$V_{clamp(l)}$	Input Low Clamp Voltage	I_{DET} = -3mA	0	0.65	1.00	
$Ib_{(ZCD)}$	Input Bias Current	1V ≤ V_{ZCD} ≤ 5V	-1.0	-0.1	1.0	mA
$I_{source(ZCD)}$ (3)	Source Current Capability	T_A = 25°C			-10	mA
$I_{sink(ZCD)}$ (3)	Sink Current Capability	T_A = 25°C			10	
T_{DEAD} (3)	Maximum Delay, ZCD to Output Turn-on		100		200	
OUTPUT SECTION						
V_{oh}	Output Voltage High	I_O = -100mA, T_A = 25°C	9.2	11.0	12.8	V
V_{ol}	Output Voltage Low	I_O = 100mA, T_A = 25°C		1.0	2.5	
T_r (3)	Rising Time	C_l = 1nF		50	100	ns
T_f (3)	Falling Time	C_l = 1nF		50	100	
$V_{O(MAX)}$	Maximum Output Voltage	V_{DDP} = 20V, I_O = 100mA	11.5	13.0	14.5	V
$V_{O(UVLO)}$	Output Voltage with UVLO Activated	V_{DDP} = 5V, I_O = 100mA			1	
RESTART TIMER SECTION						
$t_{d(rst)}$	Restart Time Delay		50	150	300	ms
OVER-VOLTAGE PROTECTION SECTION						
V_{OVP}	OVP Threshold Voltage	T_A = 25°C	2.620	2.675	2.730	V
$HY_{(OVP)}$	OVP Hysteresis	T_A = 25°C	0.120	0.175	0.230	
ENABLE SECTION						
$V_{th(en)}$	Enable Threshold Voltage		0.40	0.45	0.50	V
$HY_{(en)}$	Enable Hysteresis		0.05	0.10	0.15	

Note:

3. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (Continued)

V_{BIAS} (V_{DDB}, V_{BS}) = 14.0V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
BALLAST PART(4)						
Supply Voltage Section						
$V_{DDTH(ST+)}$	V_{DDB} UVLO Positive Going Threshold	V_{DDB} Increasing	12.4	13.4	14.4	V
$V_{DDTH(ST-)}$	V_{DDB} UVLO Negative Going Threshold	V_{DDB} Decreasing	10.8	11.6	12.4	
$V_{DDHY(ST)}$	V_{DDB}-side UVLO Hysteresis			1.8		
V_{CL}	Supply Clamping Voltage	I_{DDB} = 10mA	14.8	15.2		
I_{ST}	Start-up Supply Current	V_{DDB} = 12V		150		µA
$I_{DDB(dyn)}$	Dynamic Operating Supply Current	50kHz, C_L = 1nF		3.2		mA
High-Side Supply Section (V_B-V_S)						
$V_{HSTH(ST+)}$	High-side UVLO Positive Going Threshold	V_{BS} Increasing	8.5	9.2	10.0	V
$V_{HSTH(ST-)}$	High-side UVLO Negative Going Threshold	V_{BS} Decreasing	7.9	8.6	9.5	
$V_{HSHY(ST)}$	High-side UVLO Hysteresis			0.6		
I_{HST}	High-side Quiescent Supply Current	V_{BS} = 14V		50		µA
I_{HD}	High-side Dynamic Operating Supply Current	50kHz, C_L = 1nF		1		mA
I_{LK}	Offset Supply Leakage Current	V_B = V_S = 600V			45	µA
Oscillator Section						
V_{MPH}	CPH Pin Preheating Voltage Range		2.5	3.0	3.5	V
I_{PH}	CPH Pin Charging Current During Preheating	V_{CPH} = 1V	1.25	2.00	2.85	µA
I_{IG}	CPH Pin Charging Current During Ignition	V_{CPH} = 4V	8	12	16	
V_{MO}	CPH Pin Voltage Level at Running Mode			7.0		V
f_{PRE}	Preheating Frequency	R_T = 80kΩ, V_{CPH} = 2V	72	85	98	kHz
f_{OSC}	Running Frequency	R_T = 80kΩ	48.2	53.0	57.8	kHz
DT_{MAX}	Maximum Dead Time	V_{CPH} = 1V, V_S = GND in Preheat Mode		3.1		µs
DT_{MIN}	Minimum Dead Time	V_{CPH} = 6V, V_S = GND in Run Mode		1.0		µs
Output Section						
I_{OH+}	High-side Driver Sourcing Current	PW = 10µs	250	350		mA
I_{OH-}	High-side Driver Sinking Current	PW = 10µs	500	650		
I_{OL+}	Low-side Driver Sourcing Current	PW = 10µs	250	350		
I_{OL-}	Low-side Driver Sink Current	PW = 10µs	500	650		
t_{HOR}	High-side Driver Turn-on Rising Time	C_L = 1nF, V_{BS} = 15V		45		ns
t_{HOL}	High-side Driver Turn-off Rising Time	C_L = 1nF, V_{BS} = 15V		25		
t_{LOR}	Low-side Driver Turn-on Rising Time	C_L = 1nF, V_{BS} = 15V		45		
t_{LOL}	Low-side Driver Turn-off Rising Time	C_L = 1nF, V_{BS} = 15V		25		
V_S(5)	Maximum Negative V_S Swing Range for Signal Propagation to High-side Output			-9.8		V

Electrical Characteristics (Continued)

V_{BIAS} (V_{DDB}, V_{BS}) = 14.0V, T_A = 25°C, unless otherwise specified.

Symbol	Characteristics	Condition	Min.	Typ.	Max.	Unit
Protection Section						
V_{CPHSD}	Shutdown Voltage	V_{RT} = 0 After Run Mode	2.6			V
I_{SD}	Shutdown Current			250	450	µA
TSD(5)	Thermal Shutdown			165		°C

Notes:

4. Please refer to the FAN7711 datasheet for more detailed information. Available on Fairchild's website at:
   Datasheet: http://www.fairchildsemi.com/ds/FA%2FFAN7711.pdf

5. This parameter, although guaranteed, is not 100% tested in production.

Component List for 32W Two Lamps

Part	Value	Note
Resistor		
R1	330kΩ	1/2W
R2	750kΩ	1/4W
R3	100Ω	1/2W
R4	20kΩ	1/4W
R5	47Ω	1/4W
R6	10kΩ	1/4W
R7	50kΩ	1/4W
R8	47kΩ	1/4W
R9	0.3Ω	1W
R10	1MΩ	1/4W
R11	1MΩ	1/4W
R12	12.6kΩ	1/4W,1%
R13	220kΩ	2W
R50	150kΩ	1/4W
R51	150kΩ	1/4W
R52	150kΩ	1/4W
R53	90kΩ	1/4W,1%
R54	10Ω	1/4W
R55	47Ω	1/4W
R56	47kΩ	1/4W
R57	47Ω	1/4W
R58	47kΩ	1/4W
Capacitor		
C1	47nF/275V_{AC}	Box Capacitor
C2	150nF/275V_{AC}	Box Capacitor
C3	2200pF/3kV	Ceramic Capacitor
C4	2200pF/3kV	Ceramic Capacitor
C5	0.22µF/630V	Miller Capacitor
C6	12nF/50V	Ceramic Capacitor
C7	22µF/50V	Electrolytic Capacitor
C8	39pF/50V	Ceramic Capacitor
C9	1µF/50V	Ceramic Capacitor
C10	0.1µF/50V	Ceramic Capacitor
C11	47µF/450V	Electrolytic Capacitor
C50	10µF/50V	Electrolytic Capacitor
C51	1µF/50V	Ceramic Capacitor
C52	0.47µF/25V	Ceramic Capacitor, 5%
C53	100nF/50V	Ceramic Capacitor
C54	470pF/1kV	Ceramic Capacitor

Part	Value	Note
C55	15nF/630V	Miller Capacitor
C56	2.7nF/1kV	Miller Capacitor
C57	15nF/630V	Miller Capacitor
C58	2.7nF/1kV	Miller Capacitor
Diode		
D1	1N4007	1kV,1A
D2	1N4007	1kV,1A
D3	1N4007	1kV,1A
D4	1N4007	1kV,1A
D5	UF4007	Ultra Fast,1kV,1A
D6	UF4007	Ultra Fast,1kV,1A
D7	1N4148	100V,1A
D8	1N4148	100V,1A
D50	UF4007	Ultra Fast,1kV,1A
D51	UF4007	Ultra Fast,1kV,1A
D52	UF4007	Ultra Fast,1kV,1A
ZD1	IN4746A	Zener 18V, 1W
MOSFET		
M1	FQPF5N60C	500V,6A
M2	FQPF5N50C	500V,5A
M3	FQPF5N50C	500V,5A
Fuse		
Fuse	3A/250V	
TNR		
TNR	471	
NTC		
NTC	10D-09	
Line Filter		
LF1	40mH	
Transformer		
L1	0.94mH (75T:10T)	EI2820
Inductor		
L2	3.2mH (130T)	EI2820
L3	3.2mH (130T)	EI2820
IC		
U1	FAN7535	Fairchild Semiconductor

Package Dimensions

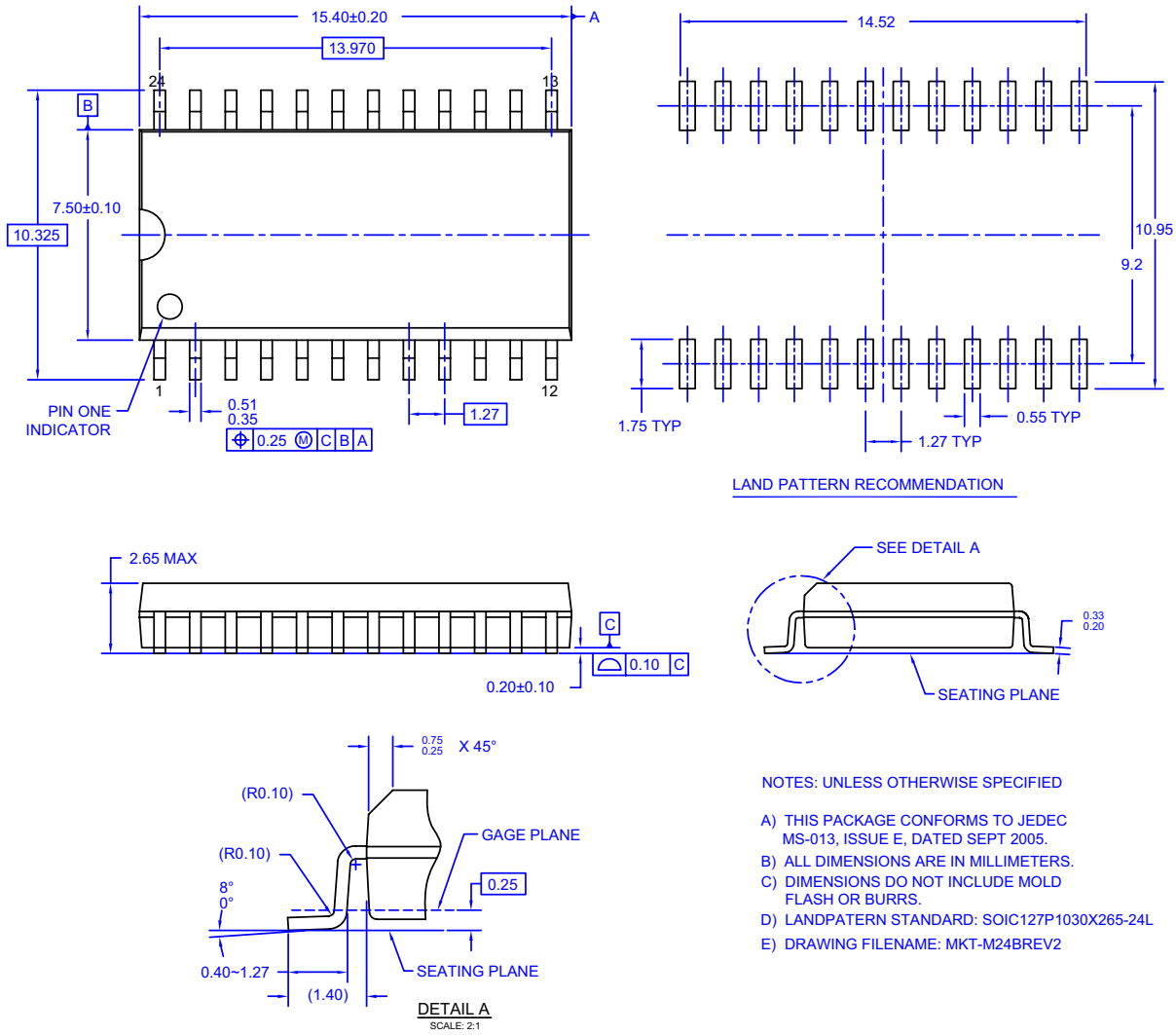


Figure 4. 24-Lead Small Outline Package (SOP)

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Rev. I32