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介绍一款采用 M65831 数码卡拉 OK 芯片的 甲类前级板

□ 莫爱雄

随着人们生活水平的提高，家庭娱乐方式更加丰富多彩。茶余饭后唱唱卡拉 OK 已成为人们自娱自乐的首选方式。

专用的混响芯片很多，其中以日本三菱公司的 M65831 性能最好，其失真低，信噪比高。M65831 的取样频率在延迟 100ms 以下时为 500kHz，延迟 100ms 以上时为 250kHz。这样高的取样频率能轻易地达到 20KHz 的音频响应。M65831 的内置静态存储器为 48Kbit，延迟时间由 12.5—169.6ms 分 16 档可调，延迟时间由 4 脚、5 脚、6 脚、7 脚的高低电平编程控制。

目前市面上出售的 M65831 卡拉 OK 板很多，各厂设计的档次各不相同。在这里笔者就向广大电子爱好者介绍一款由广东美顺电子厂生产的高品质的

M65831 数码卡拉 OK 甲类前级板。

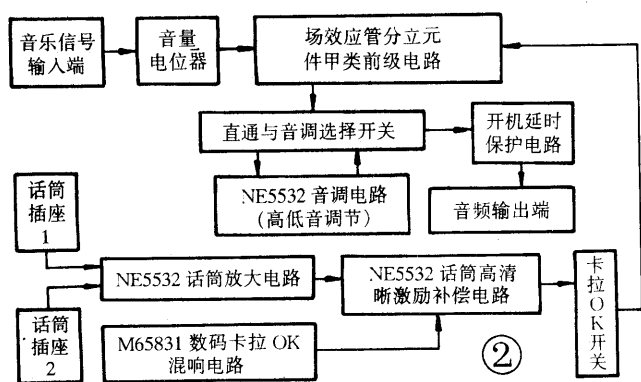
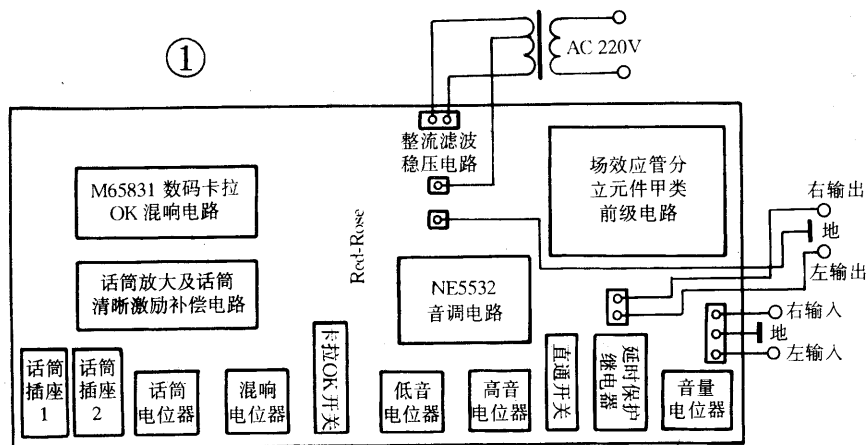
美顺 M65831 数码卡拉 OK 甲类前级板的设计特点：①元件质量上乘。电阻为进口五色环金属膜电阻，精度±1%。无级电容是日本乐声 CBB 金属化无感电容、荷兰汤姆逊的 MKP 电容等；音频耦合用钽质电容，电解电容采用日本的 ELNA、乐声、黑金刚等优质品。话筒放大、话筒高清晰激励补偿电路及音调电路由 NE5532 担任。担任音量、音调、话筒音量、混响控制电位器均采用优质 W·L 品牌；②线路板采用标准环氧板，线路镀银处理。③线路设计合理，带电源整流滤波稳压，注重退耦、接地方式，降低噪音干扰。④音频放大大部分采用名牌场效应管 K246 作为输入级、电压放大级与恒流源共同构成甲类输出级，并且精确

设定了负反馈量。音色取向柔和、自然、音乐味丰富，充分体现了甲类放大电路的优点。⑤混响芯片是正装正品。为确保演唱效果增加了高清晰激励补偿电路。⑥本板设有卡拉 OK 关断开关和音调电路切断开关，前级可直通后级，保持“原汁原味”。⑦为防止

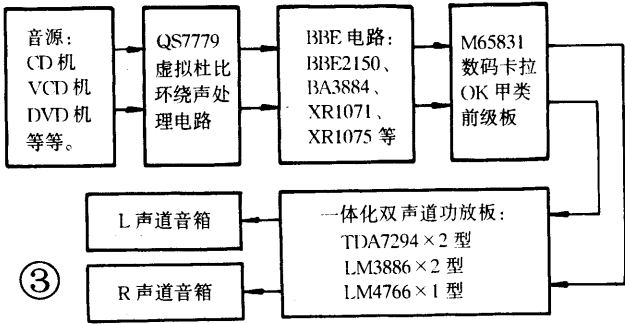
前级开机时的直流输出，本板设有延时保护电路。⑧本板带 2 个话筒插座，自备机壳及变压器等就可组成一台优质的卡拉 OK 甲类前级。

图 1 是该板的整体分布及接线图，图 2 是该板的各部分功能原理方框图。图 3 是该台卡拉 OK 甲类前级板与各种音响板组接图。实际组装视个人喜好进行取舍，并注意信号线的屏蔽（屏蔽层要单端接地），各板采用一点接地法。

若已拥有功放，需要加装该板，原功放的卡拉 OK 部分，前级的音调前置放大应取消，以本板作为前级。本板电源部分需增设一个



双 12V—双 18V 的有 5W 以上的小变压器。此外，原



功放面板的各功能电位器由本板上相应功能的电位器替换。完成上述接线确认，是否有碰线短路现象等，确保万无一失方可通电试音投入使用。

本板性能稳定，演唱效果令人满意。能让您一改噪音，以丰满圆润的歌喉，过一把歌星瘾。

• 套件供应 •

本文介绍的 M65831 数码卡拉 OK 甲类前级板及文中提及的各种音响板等广东省郁南县美顺电子厂均有邮购，广告见本刊广告插页，也可访问其网站（有说明书，文章及价目表等）：<http://www.meishun.chn.net> 广告：2000-09-08 ◀

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 Notice ; This is not a final specification.
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M65831AP/FP

DIGITAL ECHO (DIGITAL DELAY)

DESCRIPTION

The M65831A is an IC developed for producing echo effects added to voice signals picked up by microphone for karaoke applications.

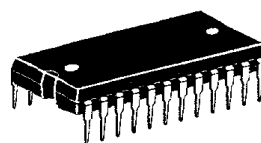
The IC has the largest memory among the digital delay series. As it's design is aimed at high performance, it is best suited to provide radio cassette tape recorders and miniature unit audio system with quality echo function.

Being pin compatible with the M65830CP / FP and M65843AP / FP, the M65831AP / FP is suitable for upgrading the series.

FEATURES

- Built-in input / output filters, A-D and D-A converters, and memory realize a delay system with only a single chip
- Capable of composing low-noise and low-distortion delay system at low cost by ADM system
 (No=-92dB typ, THD=0.5% typ)
- Control mode selections available from 2 kinds : easy mode using parallel data and microcomputer mode using serial data
- Sleep mode can be selected to stop IC functions
- Built-in automatic reset circuit

Outline



Outline 24P4 (AP)
 2.54mm pitch 600mil DIP
 (13.0mm X 31.1mm X 3.8mm)



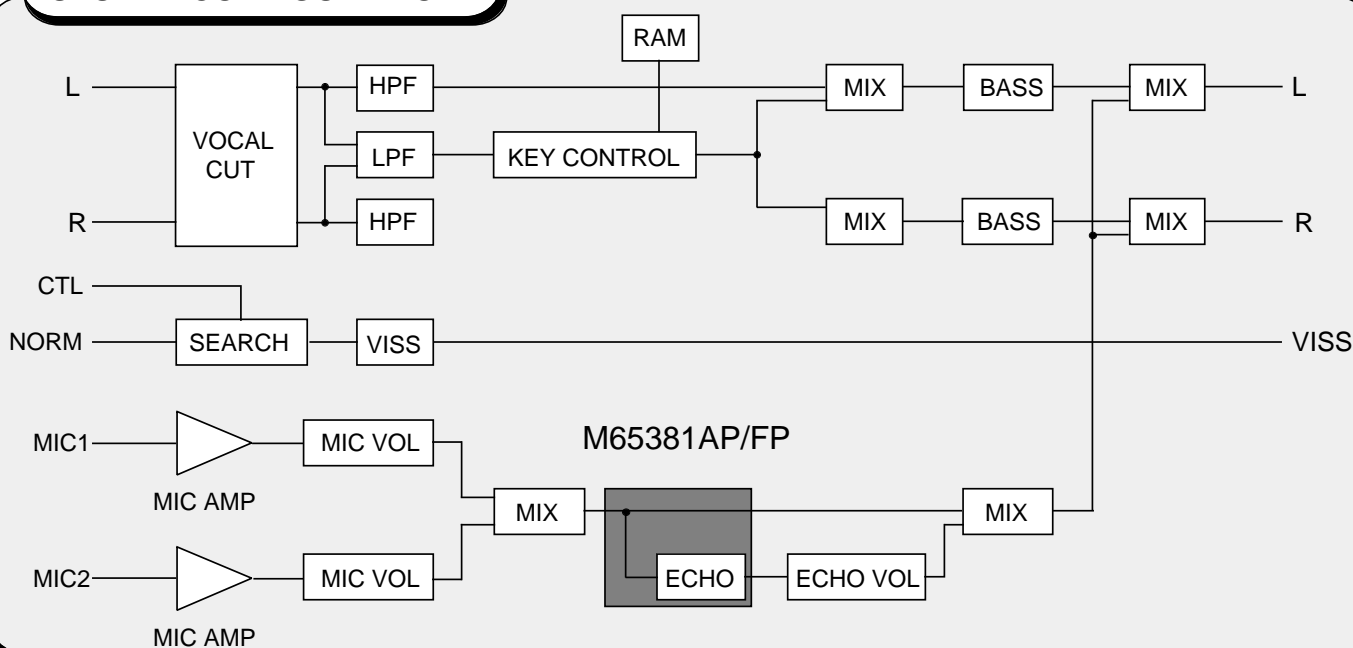
Outline 24P2W-A(AFP)
 1.27mm pitch 450mil SOP
 (8.4mm X 15.0mm X 2.0mm)

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ----- VCC,VDD=4.5 to 5.5V

Rated supply voltage ----- VCC,VDD=5.0V

SYSTEM CONFIGURATION

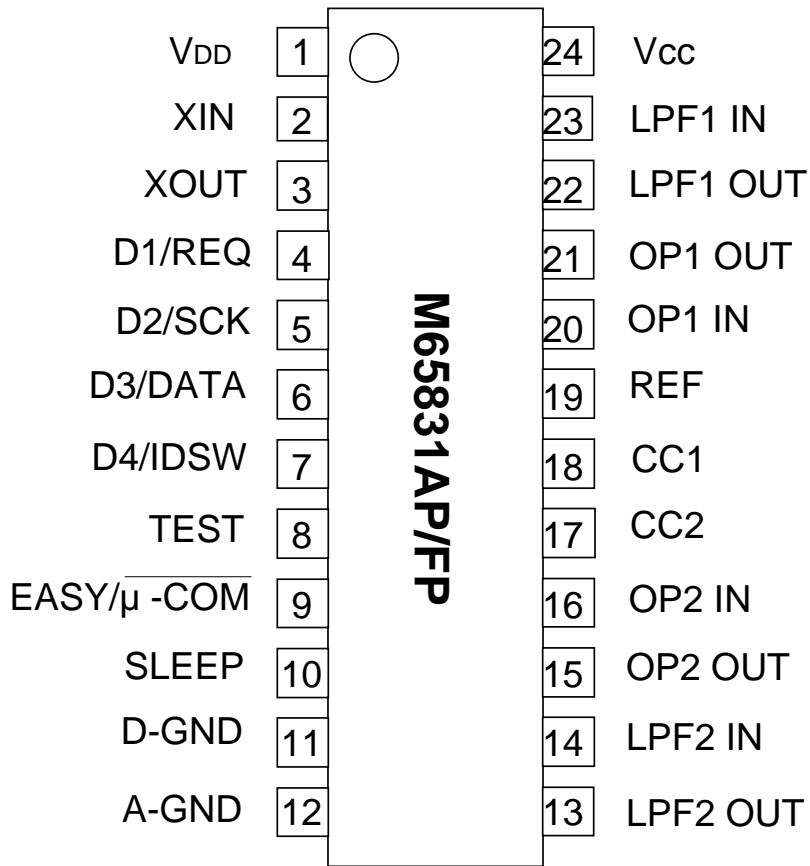


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DIGITAL ECHO (DIGITAL DELAY)

Pin Configuration

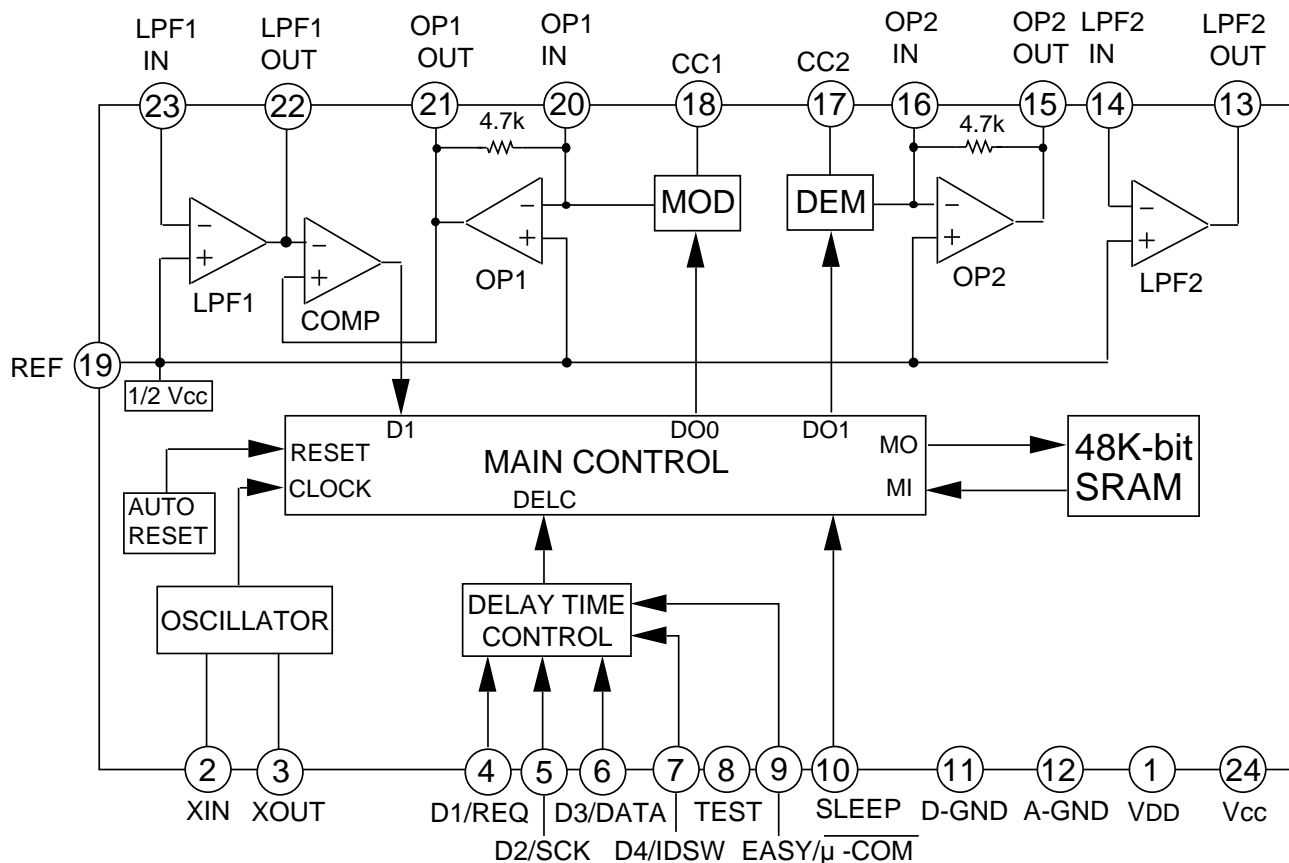


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DIGITAL ECHO (DIGITAL DELAY)

BLOCK DIAGRAM



Unit Resistance:



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DIGITAL ECHO (DIGITAL DELAY)

PIN DESCRIPTION

No.	Symbol	Name	I/O	Function
①	VDD	Digital VDD	—	Supply voltage
②	XIN	Oscillator input	I	
③	XOUT	Oscillator output	O	Connects to 2MHz ceramic filter
④	D1/REQ	Delay1/Request	I	Easy mode:inputs D1 data μ -COM mode:inputs request data
⑤	D2/SCK	Delay2/Shift clock	I	Easy mode:inputs D2 data μ -COM mode:inputs shift clock
⑥	D3/DATA	Delay3/Serial data	I	Easy mode:inputs D3 data μ -COM mode:inputs serial data
⑦	D4/IDSW	Delay4/ID switch	I	Easy mode:inputs D4 data μ -COM mode:controls ID code
⑧	TEST	Test	I	L=normal mode
⑨	EASY/ $\overline{\mu -COM}$	Easy/ $\overline{\mu -COM}$	I	H=easy mode L=μ -COM mode
⑩	SLEEP	Sleep	I	H=sleep mode L=normal mode
⑪	D GND	Digital GND	—	Connects to analog GND at one point
⑫	A GND	Analog GND	—	Connects to analog GND
⑬	LPF2 OUT	Low pass filter2 output	O	Forms low pass filter with external C.R
⑭	LPF2 IN	Low pass filter2 input	I	
⑮	OP2 OUT	OP-AMP2 output	O	Forms integrator with external C.R
⑯	OP2 IN	OP-AMP2 input	I	
⑰	CC2	Current control 2	—	
⑱	CC1	Current control 1	—	
⑲	REF	Reference	—	=1/2VCC
⑳	OP1 IN	OP-AMP1 input	I	Forms integrator with external C.R
㉑	OP1 OUT	OP-AMP1 output	O	
㉒	LPF1 OUT	Low pass filter1 output	O	Forms low pass filter with external C.R
㉓	LPF1 IN	Low pass filter1 input	I	
㉔	Vcc	Analog Vcc	—	Supply voltage

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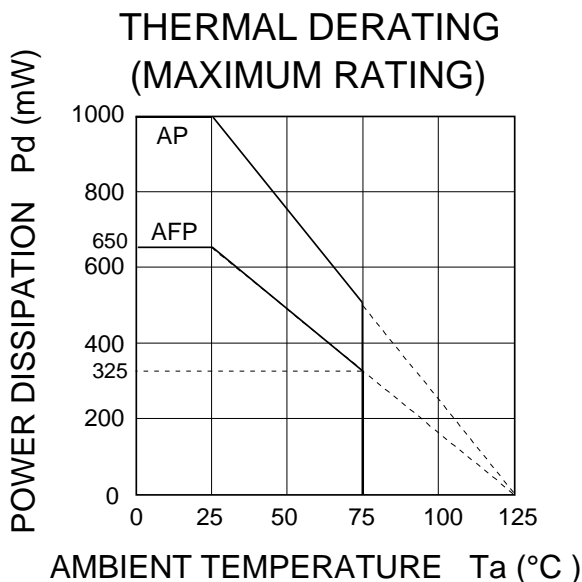
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DIGITAL ECHO (DIGITAL DELAY)

ABSOLUTE MAXIMUM RATINGS

(Vcc=5V, f=1kHz, Vi=100mVrms, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Units
Vcc	Supply voltage		6.5	V
Icc	Circuit current		100	mA
Pd	Power dissipation	M65831AP	1	W
		M65831AFP	650	mW
Topr	Operating temperature		-20~+75	°C
Tstg	Storage temperature		-40~+125	°C



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
Vcc	Supply voltage		4.5	5	5.5	V
VDD	Supply voltage		4.5	5	5.5	V
Vcc-VDD	Difference voltage		-0.3	0	0.3	V
fck	Clock frequency		1	2	3	MHz
VIH	High input voltage		0.7VDD		VDD	V
VIL	Low input voltage		0		0.3VDD	V



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DIGITAL ECHO (DIGITAL DELAY)

ELECTRICAL CHARACTERISTICS

(Vcc=5V, f=1kHz, Vi=100mVrms, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units	
			Min	Typ	Max		
Icc	Circuit current	No signal	—	18.0	40.0	mA	
Gv	Voltage gain	RL=47k	-3.5	-0.5	2.5	dB	
Vomax	Maximum output voltage	THD=10%	0.7	1	—	Vrms	
THD	Output distortion	30kHz LPF	fs=500kHz	—	0.3	1.0	%
			fs=250kHz	—	0.5	1.5	
No	Output noise voltage	DIN-AUDIO (fs=250kHz)	—	-92	-75	dBV	
SVRR	Supply voltage rejection ratio	Vcc=-20dBV, f=100Hz	—	-40	-25	dB	
TMUTE	Mute time	Upon changing Delay Time	508	528	548	ms	
		Upon canceling Sleep Mode	508	528	548		
Iccs	Circuit current (Sleep mode)	Sleep Mode	—	14.0	30.0	mA	



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DIGITAL ECHO (DIGITAL DELAY)

OPERATION

1) DELAY TIME

D4	D3	D2	D1	fs	Td
L	L	L	L	500	12.3
			H		24.6
		H	L		36.9
			H		49.2
	H	L	L		61.4
			H		73.7
		H	L		86.0
			H		98.3
H	L	L	L	250	110.6
			H		122.9
		H	L		135.2
			H		147.5
	H	L	L		159.7
			H		172.0
		H	L		184.3
			H		196.6

fs=sampling frequency(kHz)

Td=delay time(msec)



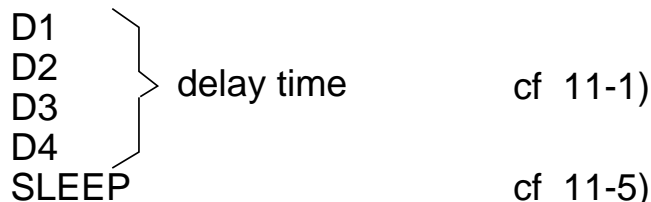
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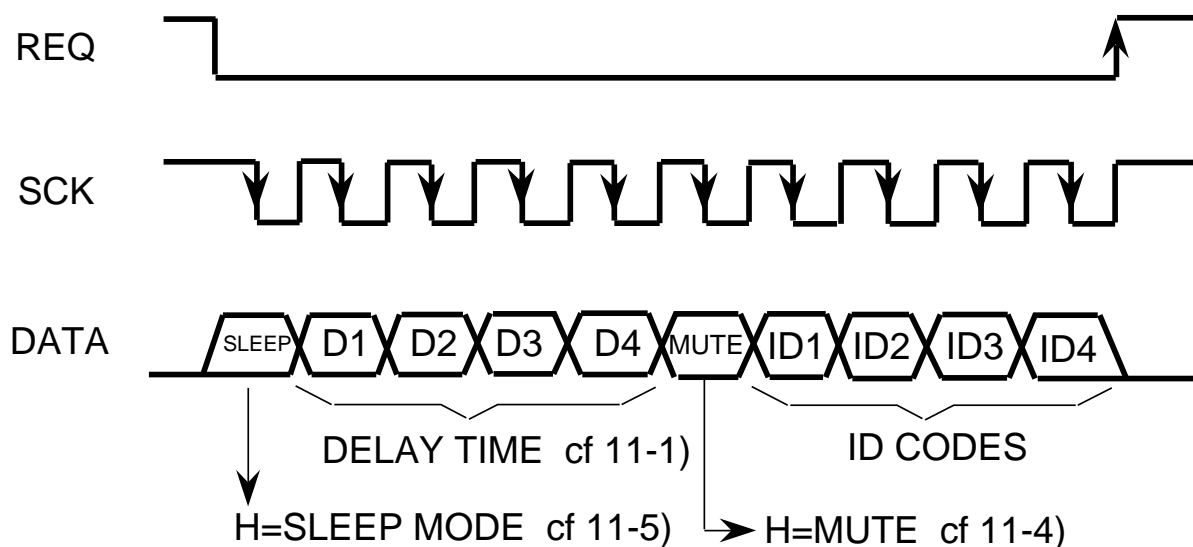
DIGITAL ECHO (DIGITAL DELAY)

2) EASY MODE (EASY / $\overline{\mu\text{-COM}}=H$)

D1,D2,D3,D4 and sleep are for easy mode



3) $\mu\text{-COM}$ MODE (EASY / $\overline{\mu\text{-COM}}=L$)



TIMING DIAGRAM

This Timing chart shows that delay time is set by serial data from $\mu\text{-COM}$.

DATA signal is latched at the falling edge of SCK signal, the last ten data are set at the rising edge of REQ signal when ID codes are satisfied. *

- * { ID1, ID3: L
- { ID2 : H
- { ID4 : equal to IDSW

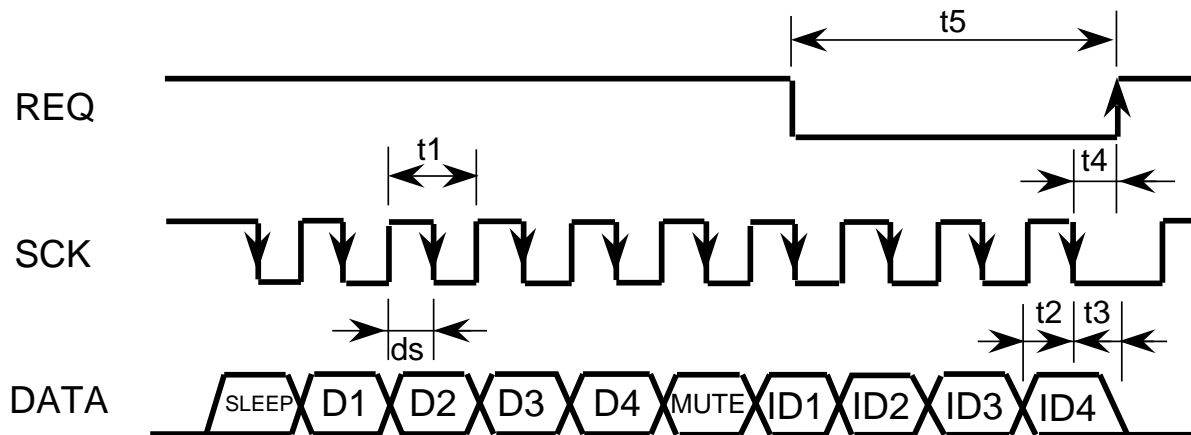


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DIGITAL ECHO (DIGITAL DELAY)

REQ,SCK,DATA INPUT TIMING



Symbol	Parameter	min	typ	max	Units
t_1	SCK pulse width	250	—	—	nsec
ds	SCK pulse duty	—	50	—	%
t_2	DATA setup time	100	$t_1/2$	—	nsec
t_3	DATA hold time	100	$t_1/2$	—	nsec
t_4	REQ hold time	100	—	—	nsec
t_5	REQ pulse width	250	—	—	nsec



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DIGITAL ECHO (DIGITAL DELAY)

4) MUTING

(1) Easy mode

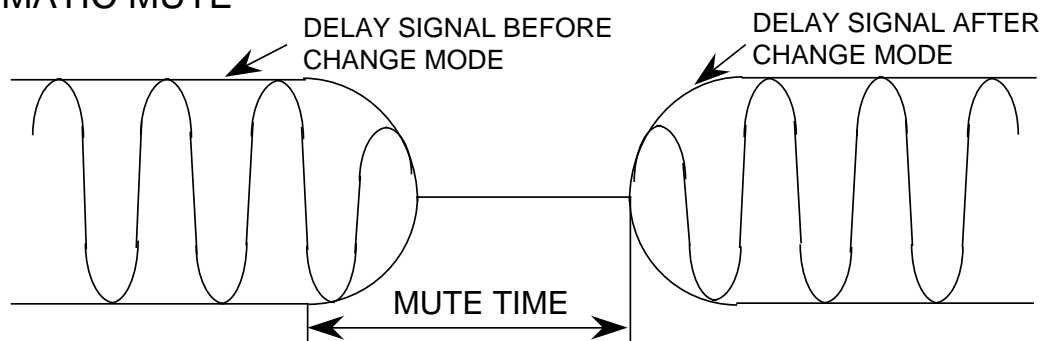
Automatic mute upon changing delay time, cancelling SLEEP mode and power-on.

(2) μ -COM mode

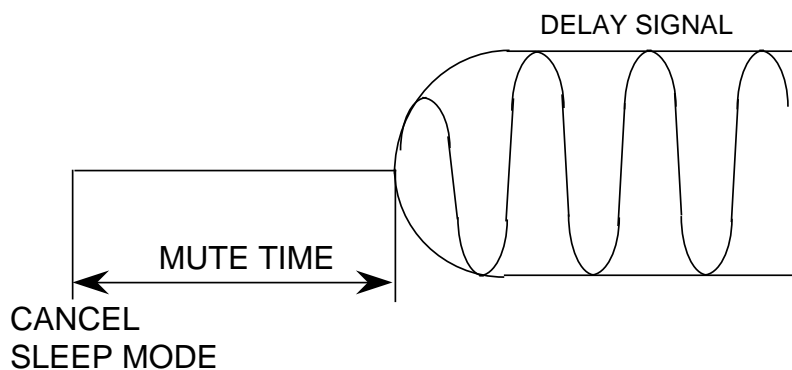
MUTE=H:mute

MUTE=L:automatic mute

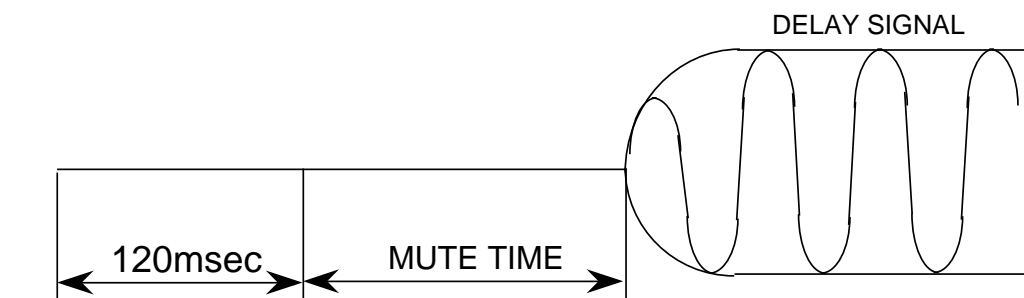
AUTOMATIC MUTE



(a) UPON CHANGING DELAY TIME



(b) UPON CANCELLING SLEEP MODE



POWER ON

(c) UPON POWER-ON



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DIGITAL ECHO (DIGITAL DELAY)

5) SLEEP MODE

SLEEP data is

- (H:clock and RAM stop to reduce circuit current (SLEEP mode)
- L:normal operation

6) SYSTEM RESET

Automatically reset power-on. The reset time is about 120msec.

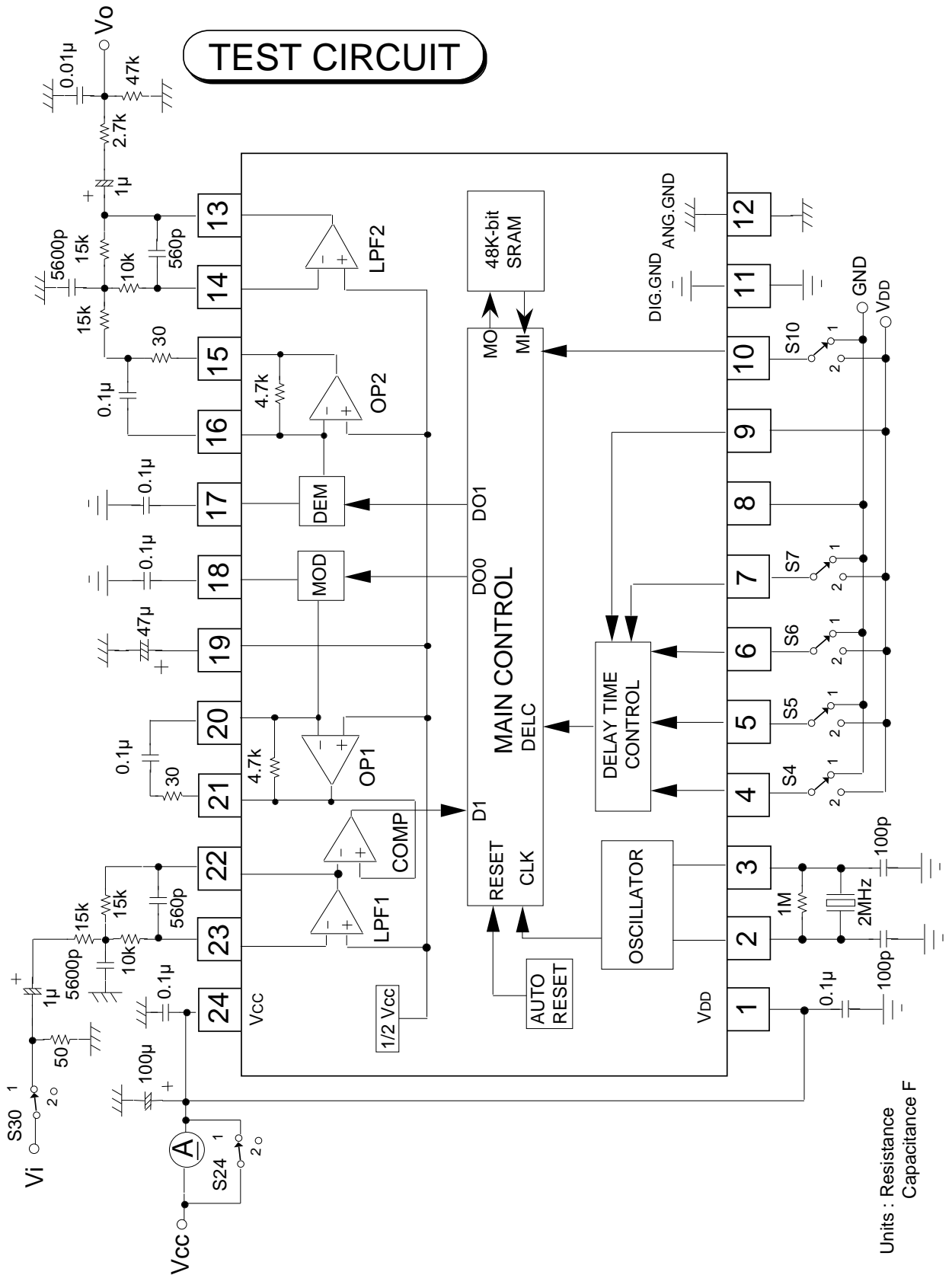
Delay time is set at 147.5msec.

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DIGITAL ECHO (DIGITAL DELAY)

TEST CIRCUIT



Units: Resistance
 Capacitance F



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DIGITAL ECHO (DIGITAL DELAY)

TEST METHODS

Switch condition

* 1 or 2

No	Parameter	Sampling frequency	Symbol	S 4	S 5	S 6	S 7	S 10	S 24	S 30	notes
1	Current circuit	—	Icc	1	1	1	1	1	2	2	No signal
2	Voltage gain	500kHz	Gv1	*	*	*	1	1	1	1	
		250kHz	Gv2	*	*	*	2	1	1	1	
3	Delay time	500kHz	Tda	1	1	1	1	1	1	1	cf. 11-1)
			Tdb	2	1	1	1	↓	↓	↓	
			Tdc	1	2	1	1	↓	↓	↓	
			Tdd	2	2	1	1	↓	↓	↓	
			Tde	1	1	2	1	↓	↓	↓	
			Tdf	2	1	2	1	↓	↓	↓	
			Tdg	1	2	2	1	↓	↓	↓	
			Tdh	2	2	2	1	↓	↓	↓	
		250kHz	Tdi	1	1	1	2	↓	↓	↓	
			Tdj	2	1	1	2	↓	↓	↓	
			Tdk	1	2	1	2	↓	↓	↓	
			Tdl	2	2	1	2	↓	↓	↓	
			Tdm	1	1	2	2	↓	↓	↓	
			Tdn	2	1	2	2	↓	↓	↓	
4	Output voltage (max)	500kHz	Vomax 1	*	*	*	1	1	1	1	30kHz L.P.F. THD=10%
		250kHz	Vomax 2	*	*	*	2	1	1	1	
5	Total harmonic distortion	500kHz	THD 1	*	*	*	1	1	1	1	30kHz L.P.F.
		250kHz	THD 2	*	*	*	2	1	1	1	
6	Output noise voltage	250kHz	No	*	*	*	2	1	1	1	DIN AUDIO Vi=0mVrms
7	Supply voltage rejection ratio	—	SVRR	*	*	*	*	1	1	2	Vcc=-20dBv, f=100Hz
8	Mute time	—	MUTE T	² ↓ ₁	*	*	*	1	1	1	Upon changing Delay Time
		—	MUTE S	*	*	*	*	² ↓ ₁	1	1	Upon cancelling Sleep Mode



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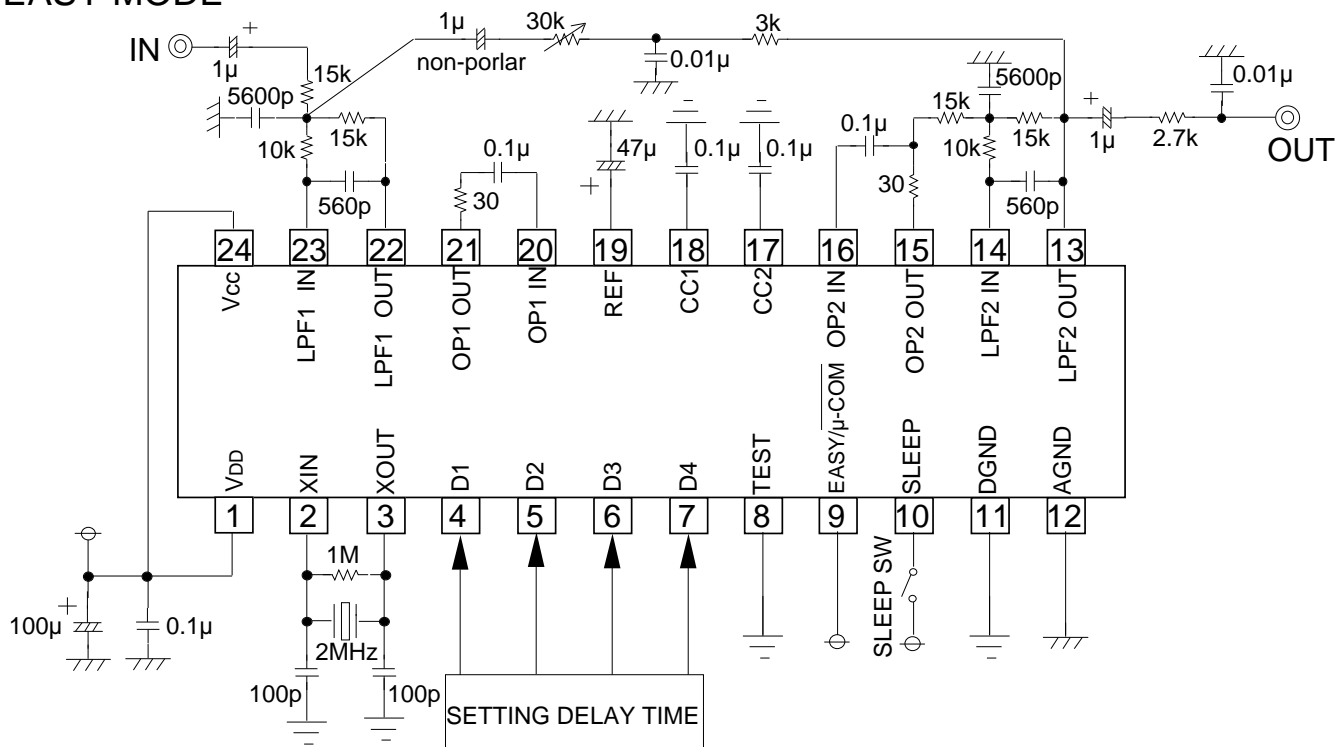
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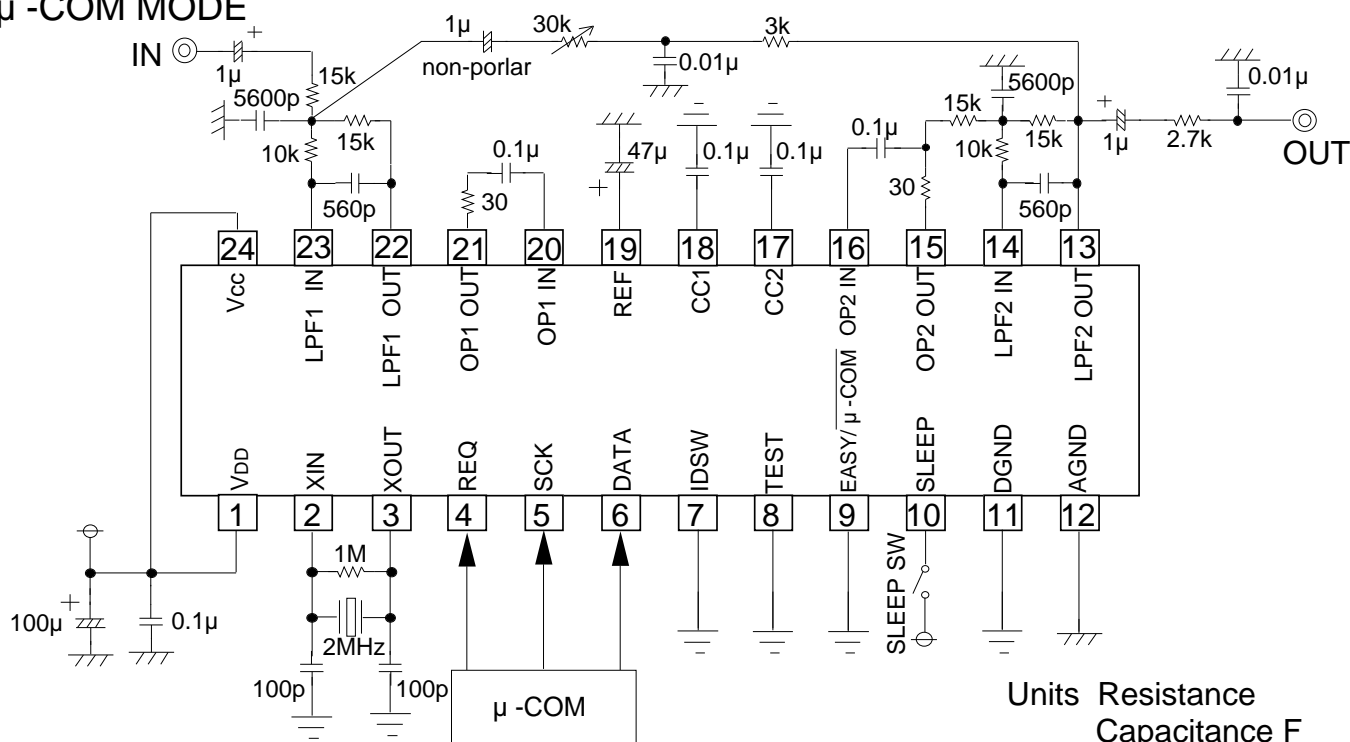
DIGITAL ECHO (DIGITAL DELAY)

APPLICATION EXAMPLE

1.EASY MODE



2.µ -COM MODE



Units Resistance
Capacitance F

