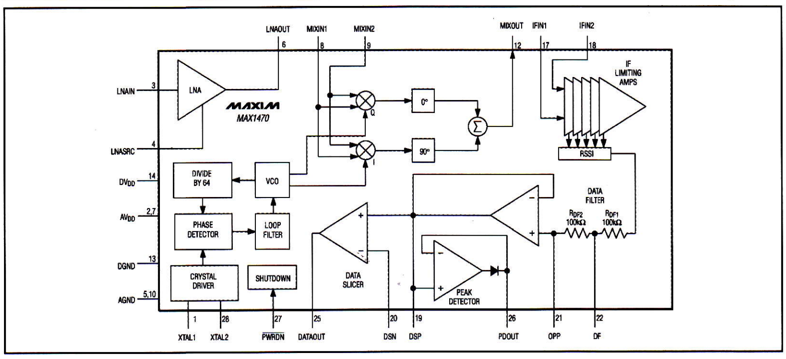
MAX1470

315MHz、低功耗、+3V、超外差接收器

112dB灵敏度、300MHz至450MHz超外差接收器，提供50dB镜频抑制

MAX1470为完全集成的低功耗、CMOS超外差接收器，用于315MHz频段的幅移键控（ASK）数据。需要极少的外部元器件并提供低电流工作模式，非常适合对成本和功耗要求苛刻的汽车与消费类产品。该芯片包括一个315MHz低噪声放大器（LNA）、一路镜频抑制混频器、完全集成的315MHz锁相环（PLL）、带有接收信号强度指示（RSSI）的10.7MHz IF限幅放大器、ASK解调器以及模拟基带数据恢复电路。MAX1470提供28引脚TSSOP封装。

Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

关键特性

- 工作电压范围为+3.0V到+3.6V
- 内置53dB RF镜频抑制电路
- -115dBm接收灵敏度*
- 250μs启动时间
- 5.5mA低工作电流
- 1.25μA低电流关断模式,有效节省功率
- 250MHz至500MHz工作带宽(镜频抑制优化在315MHz)
- 集成了PLL,内置压控振荡器(VCO)及环路滤波器
- 通过外部滤波器选择IF带宽
- 从RF到数字数据输出的完备接收系统

应用

- 车库开门器
- 医疗系统
- 远端控制
- 远端无线钥匙门禁
- 安全系统
- 玩具
- 视频游戏机控制器
- 无线计算机外设
- 无线传感器

19-2135; Rev 1; 8/02

MAXIM

315MHz Low-Power, +3V Superheterodyne Receiver

General Description

The MAX1470 is a fully integrated low-power CMOS superheterodyne receiver for use with amplitude-shift-keyed (ASK) data in the 315MHz band. With few required external components, and a low-current power-down mode, it is ideal for cost- and power-sensitive applications in the automotive and consumer markets. The chip consists of a 315MHz low-noise amplifier (LNA), an image rejection mixer, a fully integrated 315MHz phase-lock-loop (PLL), a 10.7MHz IF limiting amplifier stage with received-signal-strength indicator (RSSI) and an ASK demodulator, and analog baseband data-recovery circuitry.

The MAX1470 is available in a 28-pin TSSOP package.

Applications

Remote Keyless Entry

Garage Door Openers

Remote Controls

Wireless Sensors

Wireless Computer Peripherals

Security Systems

Toys

Video Game Controllers

Medical Systems

Features

- ♦ Operates from a Single +3.0V to +3.6V Supply
- ♦ Built-In 53dB RF Image Rejection
- ♦ -115dBm Receive Sensitivity*
- ♦ 250µs Startup Time
- ♦ Low 5.5mA Operating Supply Current
- ♦ 1.25µA Low-Current Power-Down Mode for Efficient Power Cycling
- ♦ 250MHz to 500MHz Operating Band (Image Rejection Optimized at 315MHz)
- ♦ Integrated PLL with On-Board Voltage-Controlled Oscillator (VCO) and Loop Filter
- ♦ Selectable IF Bandwidth Through External Filter
- ♦ Complete Receive System from RF to Digital Data Out

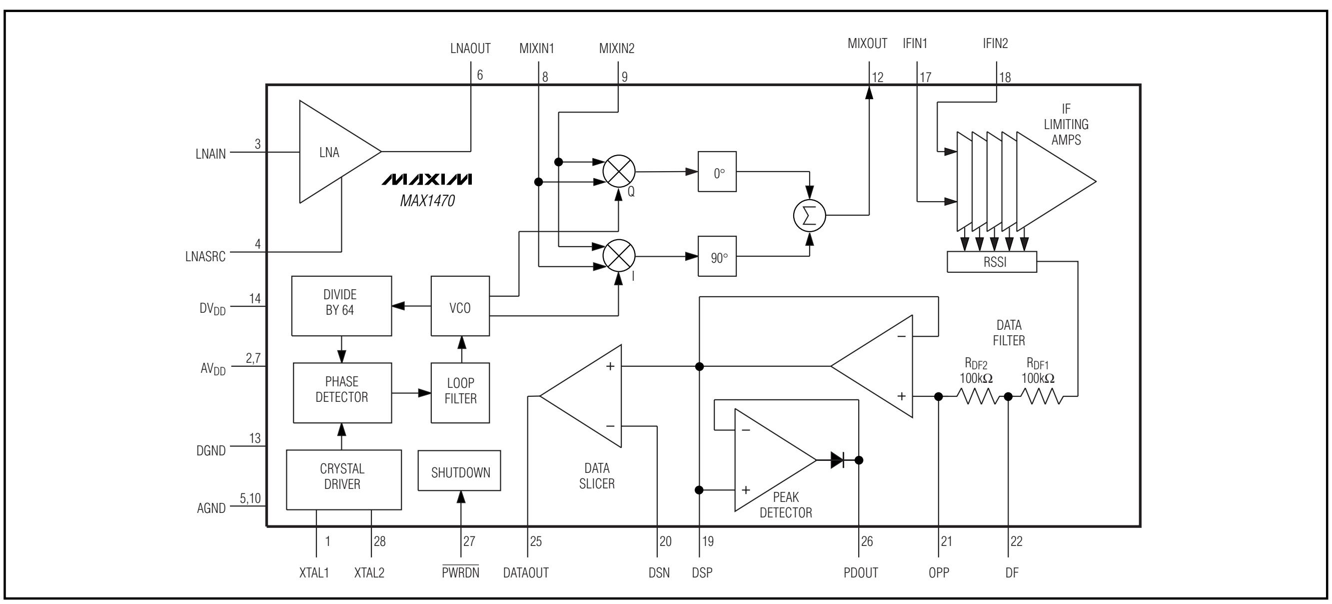
**See Note 2, AC Electrical Characteristics.*

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1470EUI	-40°C to +85°C	28 TSSOP

Typical Application Circuit appears at end of data sheet.
Pin Configuration appears at end of data sheet.

Functional Diagram



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315MHz Low-Power, +3V Superheterodyne Receiver

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND ....-0.3V to +4.0V
DV_{DD} to DGND..-0.3V to +4.0V
All Other Pins Referenced to AGND...........-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin TSSOP (derate 13mW/°C above +70°C) 1039mW

Operating Temperature Range
MAX1470EUI ....-40°C to +85°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, V_{DD} = +3.0V to +3.6V, no RF signal applied, T_A = -40°C to +85°C. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		3.0		3.6	V
Supply Current	I_{DD}	$\overline{PWRDN}$ = V_{DD}		5.5		mA
Shutdown Supply Current	$I_{SHUTDOWN}$	$\overline{PWRDN}$ = GND		1.25		µA
$\overline{PWRDN}$ Voltage Input Low	V_{IL}				0.4	V
$\overline{PWRDN}$ Voltage Input High	V_{IH}		V_{DD} - 0.4			V
DATAOUT Voltage Output Low	V_{OL}	$I_{DATAOUT}$ = 100µA			0.4	V
DATAOUT Voltage Output High	V_{OH}	$I_{DATAOUT}$ = -100µA	V_{DD} - 0.4			V

AC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +3.3V, T_A = +25°C, f_{RFIN} = 315MHz, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS						
Maximum Startup Time	T_{ON}	Time from $\overline{PWRDN}$ deasserting to valid data out		250		µs
Maximum Receiver Input Level	$RFIN_{MAX}$	Modulation depth ≥ 60dB		0		dBm
Minimum Receiver Input Level, 315MHz	$RFIN_{MIN}$	Average carrier power level (Note 2)		-115		dBm
		Peak power level (Note 2)		-109		
Minimum Receiver Input Level, 433.92MHz		Average carrier power level (Note 2)		-110		dBm
		Peak power level (Note 2)		-104		
Receivers	f_{RFIN}			250 to 500		MHz
LOW-NOISE AMPLIFIER (LNA)						
Input Impedance	$S11_{LNA}$	Normalized to 50Ω (Note 3)		1 - j4		
1dB Compression Point	$P1dB_{LNA}$			-22		dBm
Input-Referred 3rd-Order Intercept	$IIP3_{LNA}$			-18		dBm
LO Signal Feedthrough to Antenna				-95		dBm
Output Impedance	$S22_{LNA}$	Normalized to 50Ω		0.12 - j4.4		

AC ELECTRICAL CHARACTERISTICS (continued)

(Typical Application Circuit, all RF inputs and outputs are referenced to 50Ω, V_{DD} = +3.3V, T_A = +25°C, f_{RFIN} = 315MHz, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Noise Figure	NF_{LNA}			2.0		dB
Power Gain				16		dB
MIXER						
Input Impedance	$S11_{MIX}$	Normalized to 50Ω		0.25 - j2.4		
Input-Referred 3rd-Order Intercept	$IIP3_{MIX}$			-18		dBm
Output Impedance	Z_{OUT_MIX}			330		Ω
Image Rejection		f_{RFIN} = 315MHz, f_{RF_IMAGE} = 293.6MHz (Note 4)	40	53		dB
		f_{RFIN} = 433.92MHz, f_{RF_IMAGE} = 412.52MHz		39		
Noise Figure	NF_{MIX}			16		dB
Conversion Gain		330Ω IF filter load		13		dB
INTERMEDIATE-FREQUENCY DEMODULATOR BLOCK						
Input Impedance	Z_{IN_IF}			330		Ω
Operating Frequency	f_{IF}			10.7		MHz
RSSI Linearity				±1		dB
RSSI Dynamic Range				65		dB
RSSI Level		P_{RFIN} < -120dBm		1.2		V
		P_{RFIN} > -50dBm		2.0		
DATA FILTER						
Maximum Bandwidth	BW_{DF}			100		kHz
DATA SLICER						
Comparator Bandwidth	BW_{CMP}			100		kHz
Maximum Load Capacitance	C_{LOAD}			10		pF
CRYSTAL OSCILLATOR						
Reference Frequency	f_{REF}			4.7547		MHz

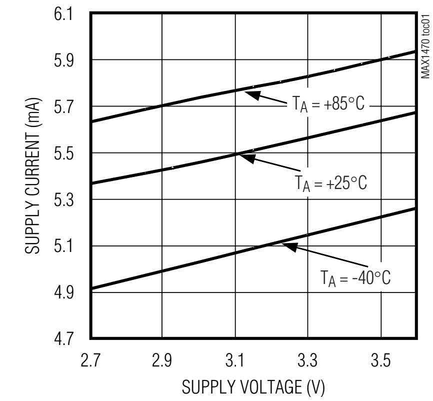
Note 1: Parts are production tested at T_A = +25°C; Min and Max values are guaranteed by design and characterization.
Note 2: BER = 2E-3, Manchester encoded, data rate = 4kbps, IF bandwidth = 350kHz.
Note 3: Input impedance is measured at the LNAIN pin. Note that the impedance includes the 15nH inductive degeneration connected from the LNASRC.
Note 4: Guaranteed by production test.

315MHz Low-Power, +3V Superheterodyne Receiver

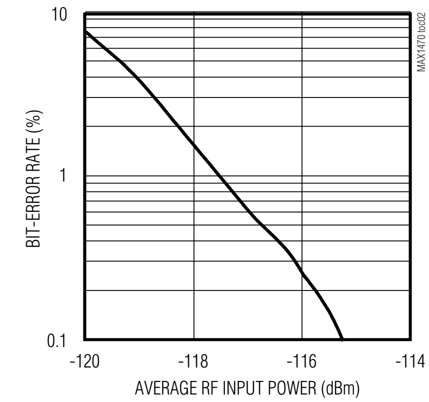
Typical Operating Characteristics

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. Typical Application Circuit.)

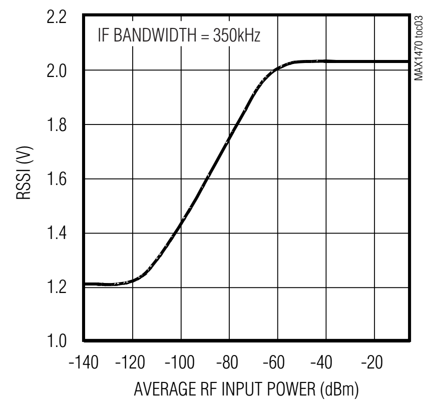
SUPPLY CURRENT vs. SUPPLY VOLTAGE



BIT-ERROR RATE vs. AVERAGE RF INPUT POWER



RSSI vs. AVERAGE RF INPUT POWER



RECEIVER SENSITIVITY vs. TEMPERATURE

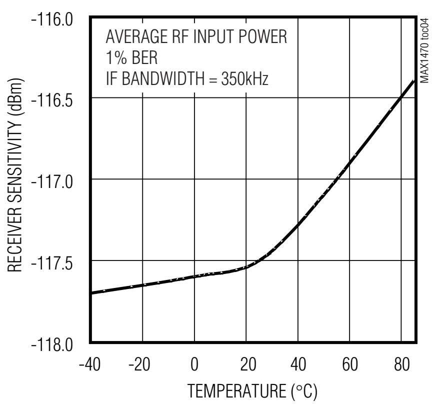
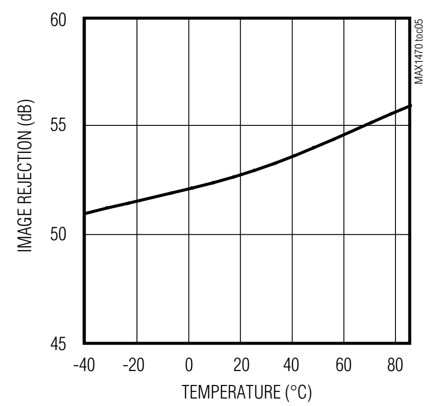
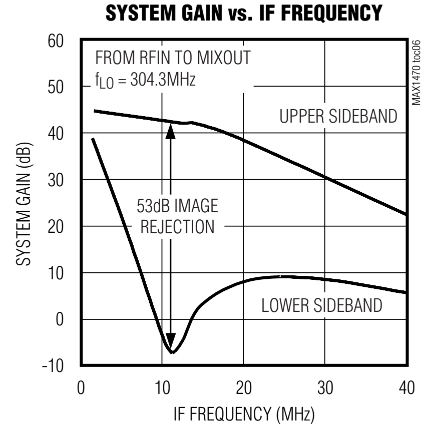


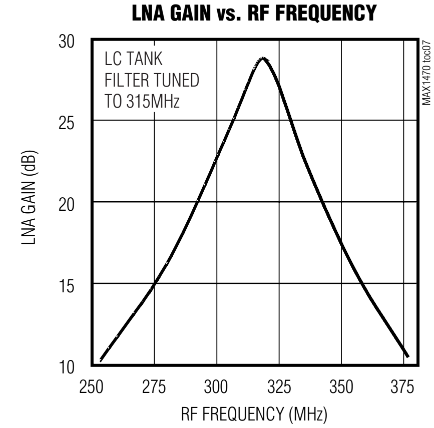
IMAGE REJECTION vs. TEMPERATURE



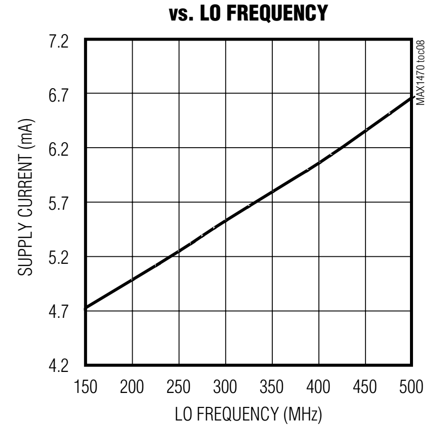
SYSTEM GAIN vs. IF FREQUENCY



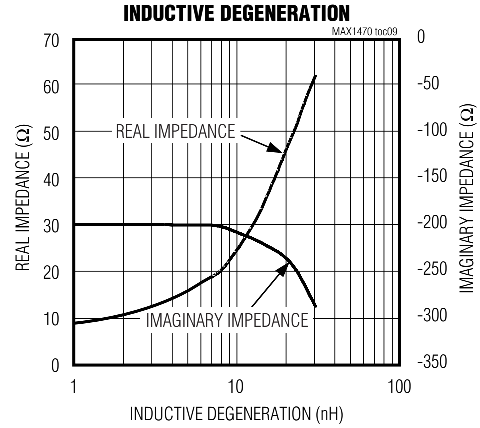
LNA GAIN vs. RF FREQUENCY



SUPPLY CURRENT vs. LO FREQUENCY



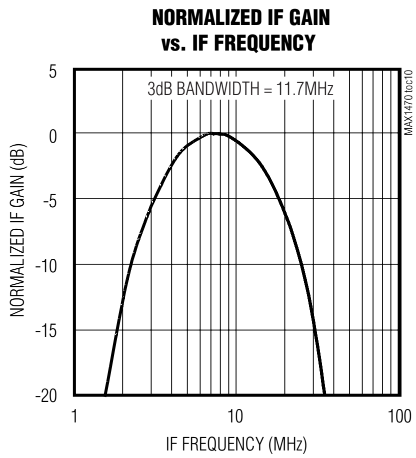
INPUT IMPEDANCE vs. INDUCTIVE DEGENERATION

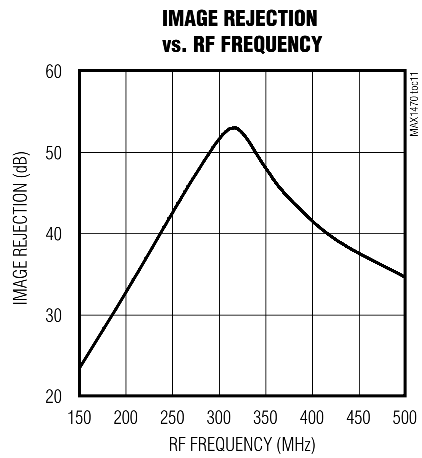


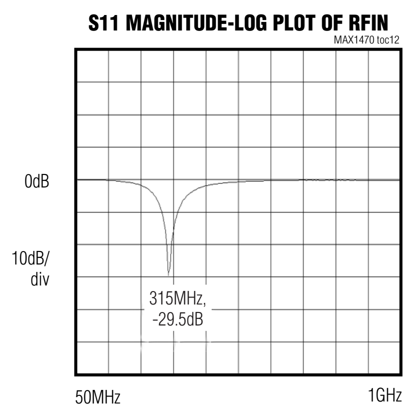
MAXIM

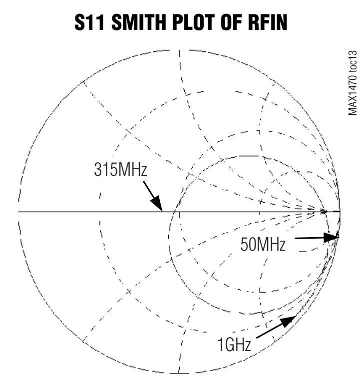
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted. Typical Application Circuit.)









Pin Description

PIN	NAME	FUNCTION
1	XTAL1	1st Crystal Input
2, 7	AV_{DD}	Positive Analog Supply Voltage for RF Sections. Decouple to AGND with 0.01µF capacitors.
3	LNAIN	Low-Noise Amplifier Input
4	LNASRC	Low-Noise Amplifier Source. Connect inductor to ground to set LNA input impedance (see *Low-Noise Amplifier* section).
5, 10	AGND	Analog Ground
6	LNAOUT	Low-Noise Amplifier Output
8	MIXIN1	1st Differential Mixer Input. Must be AC-coupled to driving input.
9	MIXIN2	2nd Differential Mixer Input. Must be AC-coupled to driving input.
11, 15, 16, 23, 24	I.C.	Internally Connected. Do not make connection to these pins.
12	MIXOUT	330Ω Mixer Output
13	DGND	Digital Ground
14	DV_{DD}	Positive Digital Supply Voltage. Decouple to DGND with a 0.01µF capacitor.
17	IFIN1	1st Differential Intermediate Frequency Limiter Amplifier Input
18	IFIN2	2nd Differential Intermediate Frequency Limiter Amplifier Input
19	DSP	Positive Data Slicer Input
20	DSN	Negative Data Slicer Input
21	OPP	Noninverting Op Amp. Input for the Sallen-Key data filter.
22	DF	Data Filter Feedback Node. Input for the feedback of the Sallen-Key data filter.
25	DATAOUT	Digital Baseband Data Output
26	PDOUT	Peak Detector Output
27	$\overline{PWRDN}$	Power-Down Select Input. Drive this pin with a logic low to shut down the IC.
28	XTAL2	2nd Crystal Input

Detailed Description

The MAX1470 CMOS superheterodyne receiver and a few external components provide the complete receive chain from the antenna to the digital output data. Depending on signal power and component selection, data rates as high as 100kbps can be achieved.

The MAX1470 is designed to receive binary ASK data on a 315MHz carrier. ASK modulation uses a difference in amplitude of the carrier to represent logic 0 and logic 1 data.

Low-Noise Amplifier

The LNA is a cascode amplifier with off-chip inductive degeneration that achieves approximately 16dB of power gain with a 2.0dB noise figure and an IIP3 of -18dBm. The gain and noise figure is dependent on both the antenna matching network at the LNA input, and the LC tank network between the LNA output and the mixer inputs.

The off-chip inductive degeneration is achieved by connecting an inductor from LNASRC to AGND. This inductor sets the real part of the input impedance at LNAIN, allowing for a more flexible match for low-input impedance such as a PC board trace antenna. A nominal value for this inductor with a 50Ω input impedance is 15nH, but is affected by PC board trace. See *Typical Operating Characteristics* for the relationship between the inductance and input impedance.

The LC tank filter connected to LNAOUT comprises L1 and C9 (see *Typical Applications Circuit*). L1 and C9 values are selected to resonate at the RF input frequency of 315MHz. The resonant frequency is given by:

$$f = \frac{1}{2\pi\sqrt{L_{TOTAL} \times C_{TOTAL}}}$$

where:

$$L_{TOTAL} = L1 + L_{PARASITICS}$$
$$C_{TOTAL} = C9 + C_{PARASITICS}$$

$L_{PARASITICS}$ and $C_{PARASITICS}$ include inductance and capacitance of the PC board traces, package pins, mixer input impedance, LNA output impedance, etc. These parasitics at high frequencies cannot be ignored and can have a dramatic effect on the tank filter center frequency. Lab experimentation should be done to optimize the center frequency of the tank.

Mixer

A unique feature of the MAX1470 is the integrated image rejection of the mixer. This device was designed to eliminate the need for a costly front-end SAW filter for many applications. The advantage of not using a SAW filter is increased sensitivity, simplified antenna matching, less board space, and lower cost.

The mixer cell is a pair of double-balanced mixers that perform an IQ downconversion of the 315MHz RF input to the 10.7MHz IF with low-side injection (i.e., $f_{LO} = f_{RF} - f_{IF}$). The image rejection circuit then combines these signals to achieve ~50dB of image rejection over the full temperature range. Low-side injection is required due to the on-chip image-rejection architecture. The IF output is driven by a source-follower, biased to create a driving impedance of 330Ω to interface with an off-chip 330Ω ceramic IF filter. The voltage conversion gain driving a 330Ω load is approximately 13dB.

Phase-Lock Loop

The PLL block contains a phase detector, charge pump/integrated loop filter, VCO, asynchronous 64x clock divider, and crystal oscillator. This PLL does not require any external components. The quadrature VCO is centered at the nominal LO frequency of 304.3MHz. For an input RF frequency of 315MHz, a reference frequency of 4.7547MHz is needed for a 10.7MHz IF frequency (low-side injection is required). The relationship between the RF, IF, and reference frequencies is given by:

$$f_{REF} = (f_{RF} - f_{IF}) / 64$$

To allow the smallest possible IF bandwidth (for best sensitivity), the tolerance of the reference must be minimized.

Intermediate Frequency

The IF section presents a differential 330Ω load to provide matching for the off-chip ceramic filter. The internal five AC-coupled limiting amplifiers produce an overall gain of approximately 65dB, with a bandpass-filter-type response centered near the 10.7MHz IF frequency with a 3dB bandwidth of approximately 11.5MHz. The RSSI circuit demodulates the IF to baseband by producing a DC output proportional to the log of the IF signal level with a slope of approximately 15mV/dB (see *Typical Operating Characteristics*).

Applications Information

Crystal Oscillator

The XTAL oscillator in the MAX1470 is designed to present a capacitance of approximately 3pF between XTAL1 and XTAL2. If a crystal designed to oscillate with a different load capacitance is used, the crystal is pulled away from its stated operating frequency, introducing an error in the reference frequency. Crystals designed to operate with higher differential load capacitance always pull the reference frequency higher. For example, a 4.7547MHz crystal designed to operate with a 10pF load capacitance oscillates at 4.7563MHz with the MAX1470, causing the receiver to be tuned to 315.1MHz rather than 315.0MHz, an error of about 100kHz, or 320ppm.

In actuality, the oscillator pulls every crystal. The crystal's natural frequency is really below its specified frequency, but when loaded with the specified load capacitance, the crystal is pulled and oscillates at its specified frequency. This pulling is already accounted for in the specification of the load capacitance. Additional pulling can be calculated if the electrical parameters of the crystal are known. The frequency pulling is given by:

$$f_p = \frac{C_m}{2}\left(\frac{1}{C_{case} + C_{load}} - \frac{1}{C_{case} + C_{spec}}\right) \times 10^6$$

where:

f_p is the amount the crystal frequency is pulled in ppm.

C_m is the motional capacitance of the crystal.

C_{case} is the case capacitance.

C_{spec} is the specified load capacitance.

C_{load} is the actual load capacitance.

When the crystal is loaded as specified, i.e., C_{load} = C_{spec}, the frequency pulling equals zero.

Data Filter

The data filter is implemented as a 2nd-order lowpass Sallen-Key filter. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the fastest expected data rate from the transmitter. Keeping the corner frequency near the data rate rejects any noise at higher frequencies, resulting in an increase in receiver sensitivity.

The configuration shown in Figure 1 can create a Butterworth or Bessel response. The Butterworth filter offers a very flat amplitude response in the passband and a roll-off rate of 40dB/decade for the two-pole filter. The Bessel filter has a linear phase response, which works well for filtering digital data. To calculate the value of C5 and C6, use the following equations along with the coefficients in Table 1:

$$C5 = \frac{b}{a(100k\Omega)(\pi)(f_C)}$$

$$C6 = \frac{a}{4(100k\Omega)(\pi)(f_C)}$$

where f_C is the desired 3dB corner frequency.

For example, to choose a Butterworth filter response with a corner frequency of 5kHz:

$$C5 = \frac{1.000}{(1.414)(100k\Omega)(3.14)(5kHz)} \approx 450pF$$

$$C6 = \frac{1.414}{(4)(100k\Omega)(3.14)(5kHz)} \approx 225pF$$

Table 1. Coefficents to Calculate C5 and C6

FILTER TYPE	a	b
Butterworth (Q = 0.707)	1.414	1.000
Bessel (Q = 0.577)	1.3617	0.618

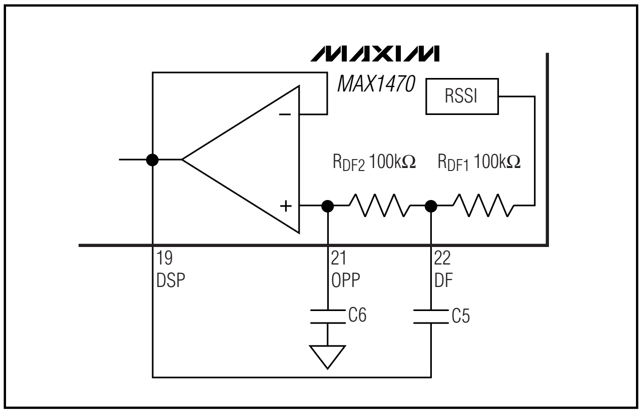


Figure 1. Sallen-Key Lowpass Data Filter

Choosing standard capacitor values changes C5 to 470pF and C6 to 220pF, as shown in the *Typical Application Circuit.*

Data Slicer

The purpose of the data slicer is to take the analog output of the data filter and convert it to a digital signal. This is achieved by using a comparator and comparing the analog input to a threshold voltage. The threshold voltage is set by the voltage on DSN, which is connected to the negative input of the data slicer comparator. The positive input is connected to the output of the data filter internally, and also the DSP pin for use with some data slicer configurations.

The suggested data slicer configuration uses a resistor (R1) connected between DSN and DSP with a capacitor (C4) from DSN to DGND (Figure 2). This configuration averages the analog output of the filter and sets the threshold to approximately 50% of that amplitude. With this configuration, the threshold automatically adjusts as the analog signal varies, minimizing the possibility for errors in the digital data. The sizes of R1 and C4 affect how fast the threshold tracks the analog amplitude. Be sure to keep the corner frequency of the RC circuit lower than the lowest expected data rate.

Note that a long string of zeros or ones can cause the threshold to drift. This configuration works best if a coding scheme, such as Manchester code, which has an equal number of zeros and ones, is used.

Peak Detector

The peak detector output (PDOUT), in conjunction with an external RC filter, creates a DC output voltage equal to the peak value of the data signal. The resistor provides a path for the capacitor to discharge, allowing the

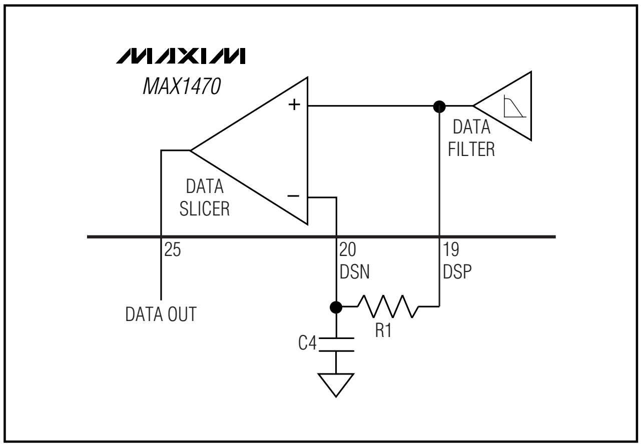


Figure 2. Generating Data Slicer Threshold

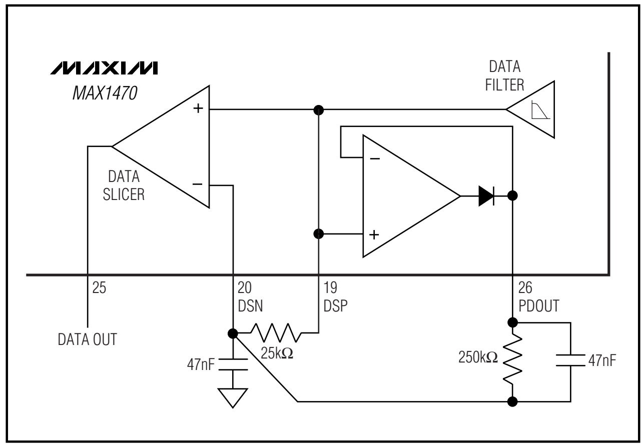


Figure 3. Using PDOUT for Faster Startup

peak detector to dynamically follow peak changes of the data filter output voltage. For faster receiver startup, the circuit shown in Figure 3 can be used.

433.92MHz Band

The MAX1470 can be configured to receive ASK modulated data with carrier frequency ranging from 250MHz to 500MHz. Only a small number of components need to be changed to retune the RF section to the desired RF frequency.

Table 2 shows a list of changed components and their values for a 433.92MHz RF; all other components remain unchanged.

The integrated image rejection of the MAX1470 is specifically designed to function with a 315MHz input frequency by attenuating any signal at 293.6MHz. The benefit of the on-chip image rejection is that an external SAW filter is not needed, reducing cost and the insertion loss associated with SAW filters. The image rejection cannot be retuned for different RF input frequencies and therefore is degraded. The image rejection at 433.92MHz is typically 39dB.

Table 2. Changed Component Values for 433.92MHz

COMPONENT	VALUE FOR 433MHz RF
C9	1.0pF
L1	15nH
L2	56nH
Y1	6.6128MHz

Note: *These values are affected by PC board layout.*

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are approximately 1/20 the wavelength or longer become antennas. For example, a 2in trace at 315MHz can act as an antenna.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PC board trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance or 10%.

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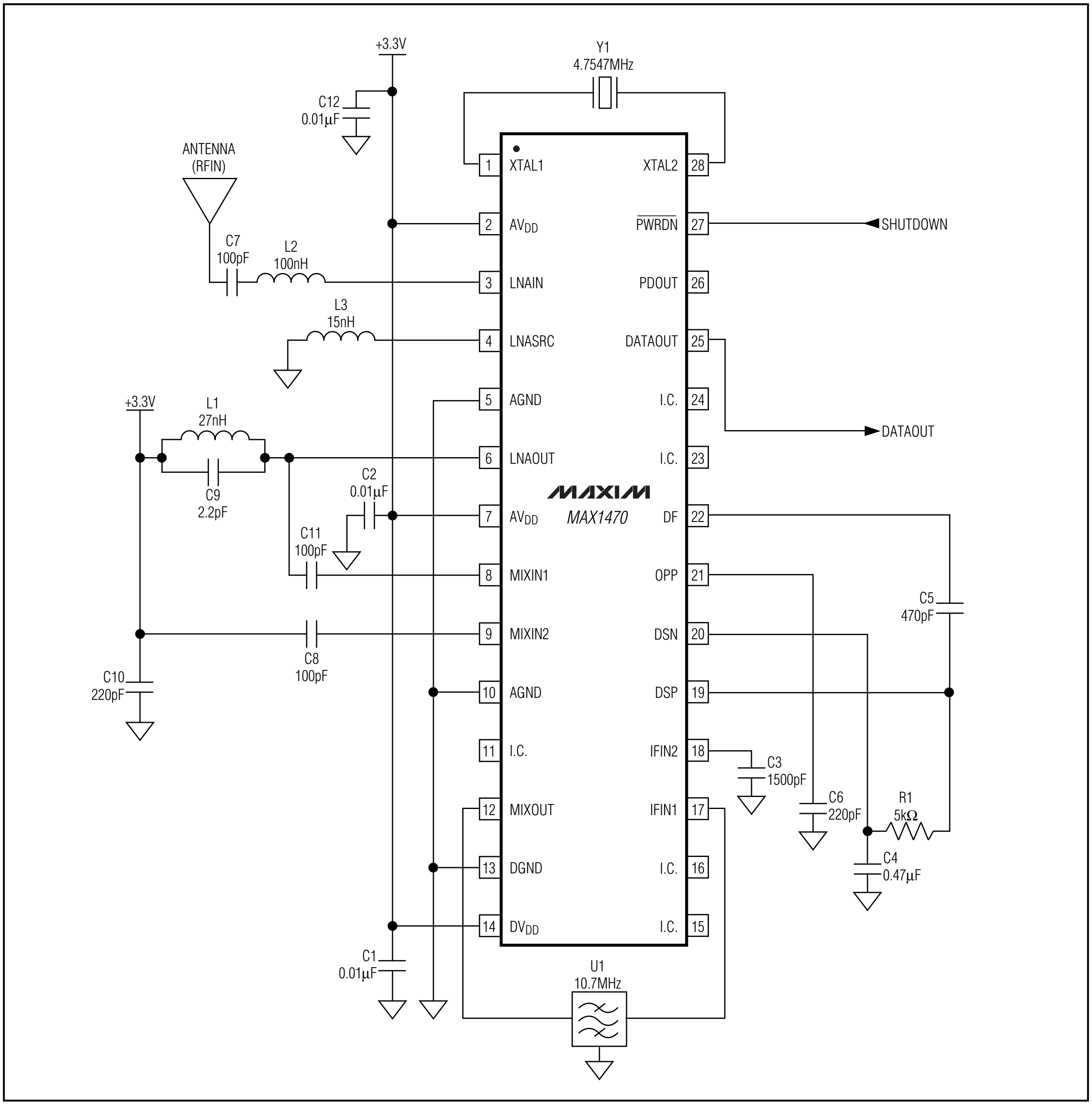
Chip Information

TRANSISTOR COUNT: 1835

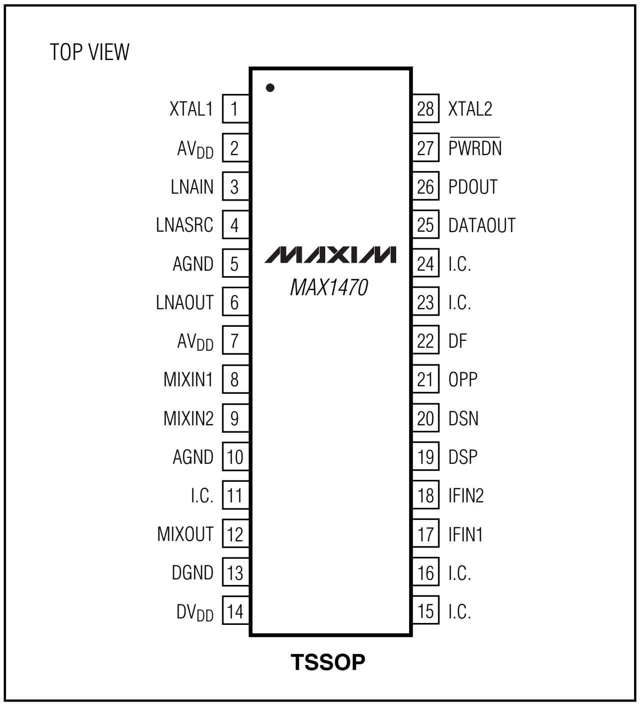
PROCESS: CMOS

315MHz Low-Power, +3V Superheterodyne Receiver

Typical Application Circuit



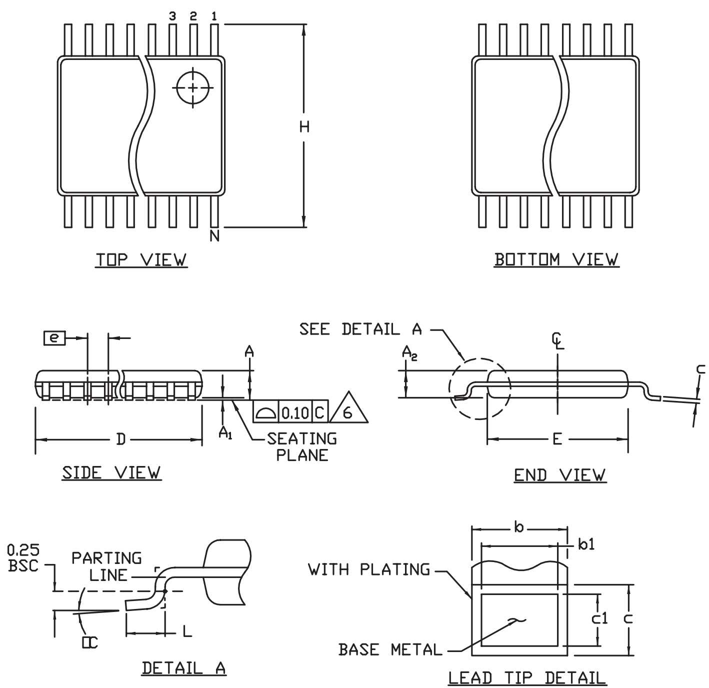
Pin Configuration



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL | DOCUMENT CONTROL NO. 21-0066 | REV. F | 1/1

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19-2609; Rev 1; 12/02

MAXIM

MAX1470 Evaluation Kit

General Description

The MAX1470 evaluation kit (EV kit) allows for a detailed evaluation of the MAX1470 superheterodyne receiver. It enables testing of the device's RF performance and requires no additional support circuitry. The RF input uses a 50Ω matching network and an SMA connector for convenient connection to test equipment. The EV kit can also directly interface to the user's embedded design for easy data decoding.

The MAX1470 EV kit comes in two versions: a 315MHz version and a 433.92MHz version. The passive components are optimized for these frequencies. These components can easily be changed to work at RF frequencies from 250MHz to 500MHz. In addition, the 5kbps data rate can be adjusted from 0kbps to 100kbps by changing two more components.

For easy implementation into the customer's design, the MAX1470 EV kit also features a proven PC board layout, which can be easily duplicated for quicker time to market. The EV kit Gerber files are available for download at www.maxim-ic.com.

Features

- ♦ **Proven PC Board Layout (Compact 3cm × 3cm)**
- ♦ **Proven Components Parts List**
- ♦ **Multiple Test Points Provided On-Board**
- ♦ **Available in 315MHz or 433.92MHz Optimized Versions**
- ♦ **250MHz to 500MHz* Adjustable Frequency Range**
- ♦ **Fully Assembled and Tested**
- ♦ **Can Operate as a Stand-Alone Receiver with Addition of an Antenna**

**Requires component changes.*

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX1470EVKIT-315	-40°C to +85°C	28 TSSOP
MAX1470EVKIT-433	-40°C to +85°C	28 TSSOP

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C2, C12	3	0.01µF ±10% ceramic capacitors (0603) Murata GRM188R71H103KA01
C3	1	1500pF ±10%, 50V X7R ceramic capacitor (0603) Murata GRM188R71H152KA01
C4	1	0.47µF +80% - 20% ceramic capacitor (0603) Murata GRM188F51C474ZA01
C5	1	470pF ±5% ceramic capacitor (0603) Murata GRM1885C1H471JA01
C6, C10	2	220pF ±5% ceramic capacitors (0603) Murata GRM1885C1H221JA01
C7, C8, C11	3	100pF ±5% ceramic capacitors (0603) Murata GRM1885C1H101JA01
C9 (315MHz)	1	4.7pF ±0.1pF ceramic capacitor (0603) Murata GRM1885C1H4R7BZ01
C9 (433MHz)	1	3.0pF ±0.1pF ceramic capacitor (0603) Murata GRM1885C1H3R0BD01
C13, C16, C18, C19	0	Not installed
C14, C15	2	15pF ±5%, 50V ceramic capacitors (0603) Murata GRM1885C1H150JZ01
C17	0	0.1µF +80% - 20% ceramic capacitor (0603) Murata GRM188R71H103KA01, not installed
F_IN	1	SMA connector edge mount, not installed EFJohnson 142-0701-801
JU1	1	3-pin header Digi-Key S1012-36-ND or equivalent
—	1	Shunt (JU1) Digi-Key S9000-ND or equivalent
JU3, JU4	0	Not installed

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
L1 (315MHz)	1	27nH ±5% inductor (0603) Murata LQG18HN27NJ00
L1 (433MHz)	1	15nH ±5% inductor (0603) Murata LQG18HN15NJ00
L2 (315MHz)	1	120nH ±5% inductor (0603) Toko LL1608FSR12J or Murata LQW18ANR12J00
L2 (433MHz)	1	68nH ±5% inductor (0603) Toko LL1608FH68J or Murata LQG18HN68NJ00
L3	1	15nH ±5% inductor (0603) Murata LQG18HN15NJ00
R1	1	5kΩ resistor (0603) Any supplier
R2, R4	0	Resistor (0603), not installed
R3	0	270Ω resistor (0603), not installed Any supplier
R5	1	10kΩ resistor (0603) Any supplier
RF_IN	1	SMA connector top mount EFJohnson 142-0701-201
MIX_OUT	0	SMA connector top mount, not installed EFJohnson 142-0701-201
TP1, TP2, TP4–TP8	0	Not installed
3.3V, GND, SHDN, DATA_OUT, TP3	5	Test points Mouser 151-203 or equivalent
Y1 (315MHz)	1	Crystal 4.754687MHz Hong Kong Crystals SSL4754687E03FAFZ8A0 or Crystek 016867
Y1 (433MHz)	1	Crystal 6.6128 MHz Hong Kong Crystals SSL6612813E03FAFZ8A0 or Crystek 016868
Y2	1	10.7MHz ceramic filter Murata SFTLA10M7FA00-B0
U1	1	MAX1470EUI
—	1	MAX1470 EV kit PC board

Component Suppliers

SUPPLIER	PHONE	FAX
Crystek	800-237-3061	941-561-1025
Hong Kong Crystals	852-2412-0121	852-2498-5908
Murata	800-831-9172	814-238-0490
Toko	408-432-8281	408-943-9790

Note: *Please indicate that you are using the MAX1470 when contacting these component suppliers.*

Quick Start

The following procedure allows for proper device evaluation.

Required Test Equipment

- Regulated power supply capable of providing 3.3V
- RF signal generator capable of delivering from -120dBm to 0dBm of output power at the operating frequency, in addition to AM or pulse-modulation capabilities (Agilent E4420B or equivalent)
- Optional ammeter for measuring supply current
- Oscilloscope

Connections and Setup

This section provides a step-by-step guide to operating the EV kit and testing the device's functionality. Do not turn on the DC power or RF signal generator until all connections are made:

1) Connect a DC supply set to 3.3V (through an ammeter, if desired) to the 3.3V and GND terminals on the EV kit. Do not turn on the supply.
2) Connect the RF signal generator to the RF_IN SMA connector. Do not turn on the generator output. Set the generator for an output frequency of 315MHz (or 433.92MHz) at a power level of -100dBm. Set the modulation of the generator to provide a 2kHz, 100% AM-modulated square wave (or a 2kHz pulse-modulated signal).
3) Connect the oscilloscope to test point TP3.

4) Turn on the DC supply. The supply current should read approximately 6mA.
5) Activate the RF generator's output without modulation. The scope should display a DC voltage that varies from approximately 1.2V to 2.0V as the RF generator amplitude is changed from -115dBm to -50dBm.
6) Set the RF generator to -100dBm. Activate the RF generator's modulation and set the scope's coupling to AC. The scope now displays a lowpass-filtered square wave at TP3 (filtered analog baseband data). Use the RF generator's LF OUTPUT (modulation output) to trigger the oscilloscope.
7) Monitor the DATA_OUT terminal and verify the presence of a 2kHz square wave.

Additional Evaluation

1) With the modulation still set to AM, observe the effect of reducing the RF generator's amplitude on the DATA_OUT terminal output. The error in this sliced digital signal increases with reduced RF signal level. The sensitivity is usually defined as the point at which the error in interpreting the data (by the following embedded circuitry) increases beyond a set limit (BER test).
2) With the above settings, a 315MHz-tuned EV kit should display a sensitivity of about -118dBm (1% BER), while a 433.92MHz kit displays a sensitivity of about -114dBm (1% BER). **Note:** The above sensitivity values are given in terms of average carrier power. If true pulse modulation is used instead of AM, then the sensitivity measurement is in terms of peak power, and as a result is reduced by 6dB.
3) Use capacitors C5 and C6 to set the corner frequency of the 2nd-order lowpass Sallen-Key data filter. The current values were selected for a corner frequency of 5kHz. Adjusting these values accommodates higher data rates (refer to the MAX1470 data sheet for more details).

Layout Issues

A properly designed PC board is an essential part of any RF/microwave circuit. On high-frequency inputs and outputs, use controlled-impedance lines and keep them as short as possible to minimize losses and radiation. At high frequencies, trace lengths that are approximately 1/20 the wavelength or longer become antennas. For example, a 2in trace at 315MHz can act as an antenna.

Keeping the traces short also reduces parasitic inductance. Generally, 1in of a PC board trace adds about 20nH of parasitic inductance. The parasitic inductance can have a dramatic effect on the effective inductance. For example, a 0.5in trace connecting a 100nH inductor adds an extra 10nH of inductance, or 10%.

To reduce the parasitic inductance, use wider traces and a solid ground or power plane below the signal traces. Using a solid ground plane can reduce the parasitic inductance from approximately 20nH/in to 7nH/in. Also, use low-inductance connections to ground on all GND pins, and place decoupling capacitors close to all VDD connections.

The EV kit PC board can serve as a reference design for laying out a board using the MAX1470. All required components have been enclosed in a 1.25in x 1.25in square, which can be directly "inserted" in the application circuit.

Table 1. Jumper Function Table

JUMPER	STATE	FUNCTION
JU1	1-2	Normal operation
JU1	2-3	Power-down mode
JU1	N.C.	External power-down control
JU3	1-2	Mixer output to MIX_OUT
JU3	2-3	External IF input
JU3	N.C.	Normal operation
JU4	1-2	Uses PDOUT for faster receiver startup
JU4	2-3	GND connection for peak detector filter

Table 2. Test Points

TP	DESCRIPTION
1	PLL control voltage (**Note:** Connecting anything to this test point degrades RF performance.)
2	Data slicer negative input
3	Data slicer positive input
4	Peak detector out
5	VDD
6	GND
7	Data filter feedback node
8	Data out
9	Power-down select input

Detailed Description

Power-Down Control

The MAX1470 can be controlled externally using the $\overline{\text{SHDN}}$ connector. The IC draws approximately 1.25µA in shutdown mode. Jumper JU1 is used to control this mode. The shunt can be placed between pins 2 and 3 for continuous shutdown, or pins 1 and 2 for continuous operation. Remove the JU1 shunt for external control. See Table 1 for the jumper function descriptions.

IF Input/Output

The 10.7MHz IF can be monitored with the help of a spectrum analyzer using the MIX_OUT SMA (not provided). Remove the ceramic filter for such a measurement and include R3 (270Ω) and C17 (0.01µF) to match the 330Ω mixer output with the 50Ω spectrum analyzer. Jumper JU3 needs to connect pins 1 and 2. It is also possible to use the MIX_OUT SMA to inject an external IF as a means of evaluating the baseband data slicing section. Jumper JU3 needs to connect pins 2 and 3.

F_IN External Frequency Input

For applications where the correct frequency crystal is not available, it is possible to directly inject an external frequency through the F_IN SMA (not provided). Connect the SMA to a function generator. The addition of C18 and C19 is necessary (use 0.01µF capacitors).

Test Points and I/O Connections

Additional test points and I/O connectors are provided to monitor the various baseband signals and for external connections. See Tables 2 and 3.

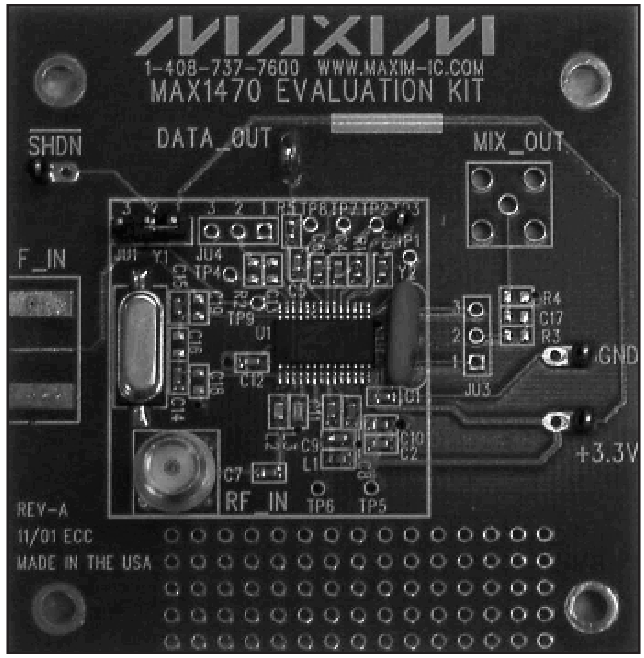
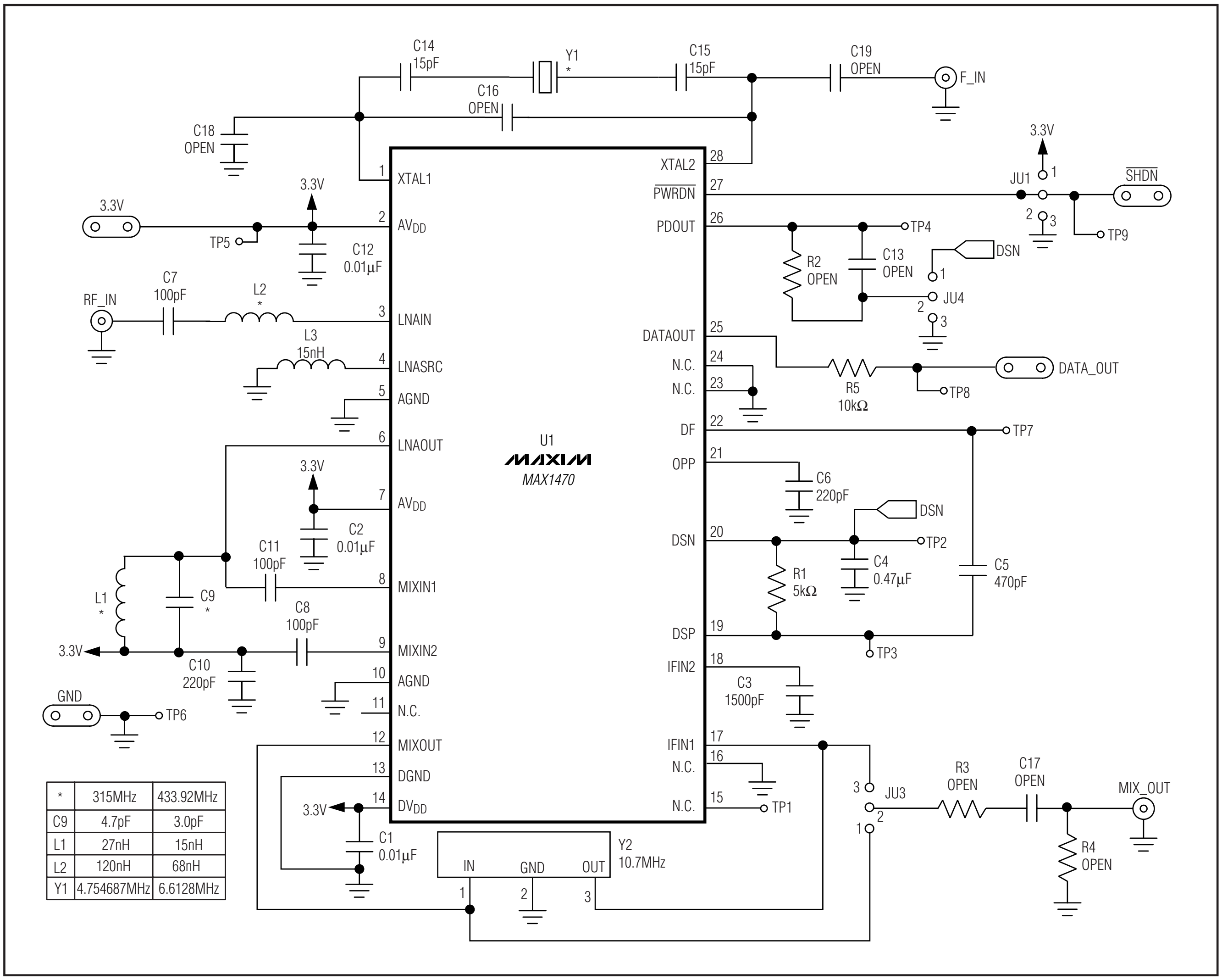


Figure 1. MAX1470 EV Kit

Table 3. I/O Connectors

SIGNAL	DESCRIPTION
RF_IN	RF input
F_IN	External reference frequency input
MIX_OUT	IF input/output
GND	Ground
3.3V	3.3V power input
DATA_OUT	Sliced data output
$\overline{\text{SHDN}}$	External power-down control



*	315MHz	433.92MHz
C9	4.7pF	3.0pF
L1	27nH	15nH
L2	120nH	68nH
Y1	4.754687MHz	6.6128MHz

Figure 2. MAX1470 EV Kit Circuit Diagram

MAX1470 Evaluation Kit

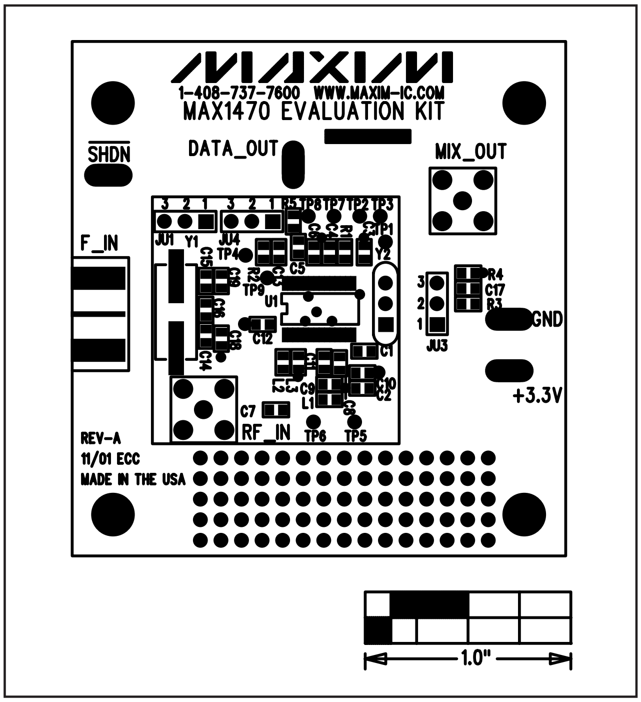


Figure 3. MAX1470 EV Kit Component Placement Guide—Top Silkscreen

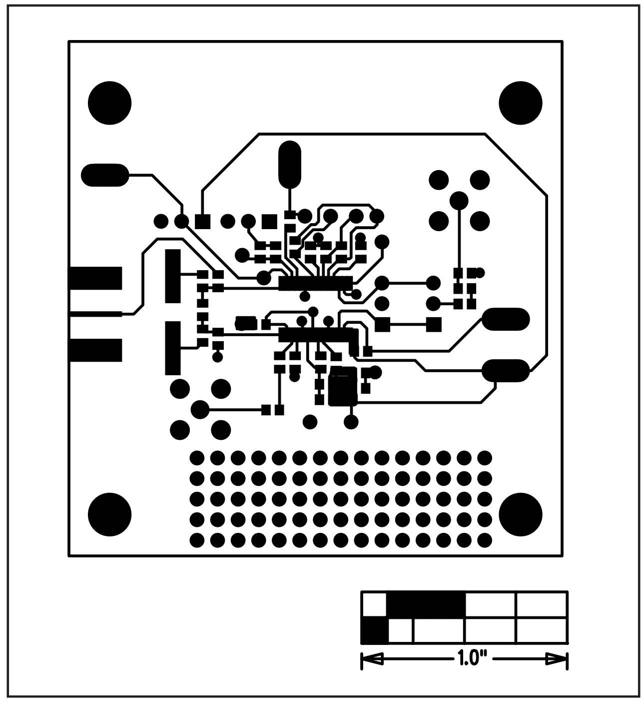


Figure 4. MAX1470 EV Kit PC Board Layout—Top Copper

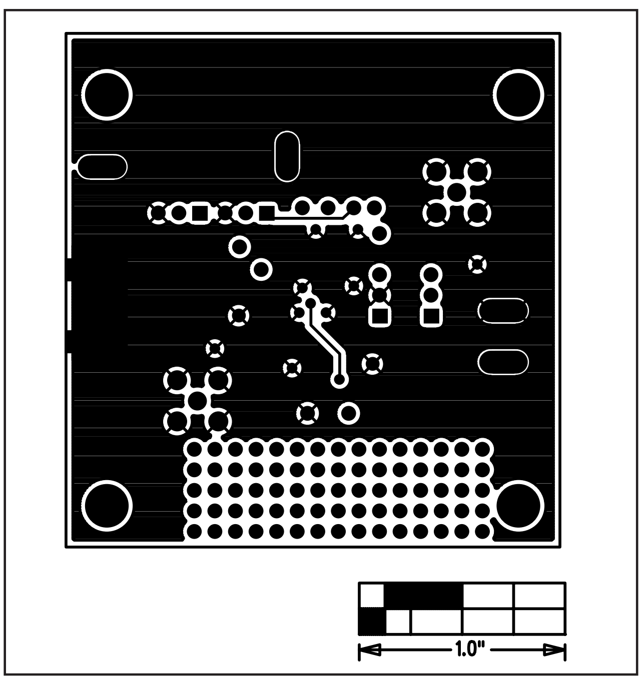


Figure 5. MAX1470 EV Kit PC Board Layout —Bottom Copper

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