19-4080; Rev 0; 4/08

MAXIM

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

概述

MAX2067高线性度模拟可变增益放大器(VGA)是单芯片SiGe BiCMOS衰减器及放大器，工作在50MHz至1000MHz频率范围，用于连接50Ω系统(参见*典型应用电路*)。利用外部电压或通过SPI™接口控制片上8位DAC实现模拟衰减器调节。

因为每级电路都具有RF输入和RF输出，通过适当配置可以优化NF (第1级为放大器)或OIP3 (最后一级为放大器)。该器件还包含具有22dB增益的放大器(放大器本身)，增益最大时NF为4dB (包括衰减器的插入损耗)，并提供+43dBm的高OIP3。这些特性使得MAX2067能够为众多接收器和发射器提供一个理想的VGA。

另外，MAX2067采用+5V单电源供电，提供功能完备的解决方案；工作在+3.3V时，性能指标略有降低，可以调节偏置电流在电流损耗和线性度方面进行折衷。器件采用紧凑、带裸焊盘的40引脚、薄型QFN封装(6mm x 6mm)。工作在扩展级温度范围(T_C = -40°C至+85°C)。

应用

IF和RF增益分级设计

温度补偿电路

蜂窝频段WCDMA和cdma2000®基站

GSM 850/GSM 900 EDGE基站

WiMAX和LTE基站以及用户驻地设备

固定宽带无线接入

无线本地环路

军用系统

视频点播(VOD)和DOCSIS®兼容于EDGE QAM调制

电缆调制解调器端接系统(CMTS)

RFID手持终端及门禁读卡器

特性

- ♦ 50MHz到1000MHz RF频率范围
- ♦ 引脚兼容的系列产品包括：
  MAX2065 (模拟/数字VGA)
  MAX2066 (数字VGA)
- ♦ +21.9dB (典型值)最大增益
- ♦ 100MHz带宽内保持0.5dB增益平坦度
- ♦ 31dB增益范围
- ♦ 内置用于模拟衰减控制的DAC
- ♦ 优异的线性指标(配置放大器为最后一级)
  +43dBm OIP3
  +66dBm OIP2
  +19dBm输出1dB压缩点
  -70dBc HD2
  -87dBc HD3
- ♦ 4dB典型噪声系数(NF)
- ♦ 单电源+5V供电(可选择+3.3V单电源供电)
- ♦ 优异的外部电流设置电阻，提供降功率/降性能两种工作模式

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX2067ETL+	-40°C to +85°C	40 Thin QFN-EP*
MAX2067ETL+T	-40°C to +85°C	40 Thin QFN-EP*

+表示无铅封装。
**EP = 裸焊盘。*
T = 卷带包装。

引脚配置在数据资料的最后给出。

SPI是Motorola, Inc.的商标。
cdma2000是电信工业协会的注册商标。
DOCSIS和CableLabs是Cable Television Laboratories, Inc. (CableLabs®)的注册商标。

ABSOLUTE MAXIMUM RATINGS

VCC_ to GND .....-0.3V to +5.5V
VDD_LOGIC, DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT.....-0.3V to (VCC_ + 0.3V)
AMP_IN, AMP_OUT, VREF_IN, ANALOG_VCTRL .....-0.3V to (VCC_ + 0.3V)
ATTEN_IN, ATTEN_OUT.....-1.2V to +1.2V
RSET to GND.....-0.3V to +1.2V
RF Input Power (ATTEN_IN, ATTEN_OUT).....+20dBm
RF Input Power (AMP_IN).....+18dBm
Continuous Power Dissipation (Note 1) 6.5W
θ_{JA} (Notes 2, 3).....+38°C/W
θ_{JC} (Note 3) .....+10°C/W
Operating Temperature Range (Note 4).....T_C = -40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com.cn/thermal-tutorial**.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, high-current (HC) mode, $V_{CC} = V_{DD}$ = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at $V_{CC} = V_{DD}$ = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Note 5	3.0	3.3	3.6	V
Supply Current	I_{CC}			60	82	mA
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT)						
Input High Voltage	V_{IH}			2		V
Input Low Voltage	V_{IL}			0.8		V

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{DD}$ = +4.75V to +5.25V, T_C = -40°C to +85°C. Typical values are at $V_{CC} = V_{DD}$ = +5V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Low-current (LC) mode		72	92	mA
		High-current (HC) mode		123	146	
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, VDAC_EN, VREF_SELECT)						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Current Logic-High	I_{IH}		-1		+1	µA
Input Current Logic-Low	I_{IL}		-1		+1	µA

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = V_{DD} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +3.3V, HC mode with attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)	50		1000	MHz
Small-Signal Gain	G			21.3		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, maximum gain setting		38		dBm
Noise Figure	NF	Maximum gain setting		4.3		dB
Total Attenuation Range				31		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = V_{DD} = +4.75 to +5.25V, HC mode with attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)		50		1000	MHz
Small-Signal Gain	G	200MHz			21.9		dB
		350MHz, T_C = +25°C (Note 5)		20.3	21.3	22.3	
		450MHz			20.9		
		750MHz			19.4		
		900MHz			18.7		
Gain Variation vs. Temperature					-0.006		dB/°C
Gain Flatness vs. Frequency		Any 100MHz frequency band from 50MHz to 500MHz			0.5		dB
Noise Figure	NF	200MHz			4		dB
		350MHz, T_C = +25°C (Note 5)			4.2	5.2	
		450MHz			4.3		
		750MHz			4.8		
		900MHz			5		
Total Attenuation Range					31		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$			66		dBm
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, HC mode, Δf = 1MHz	200MHz		43		dBm
			350MHz		40.8		
			450MHz		39.8		
			750MHz		37.3		
			900MHz		36.2		
		P_{OUT} = 0dBm/tone, LC mode, Δf = 1MHz	200MHz		40		
			350MHz		38.2		
			450MHz		37.4		
			750MHz		35.5		
			900MHz		34.3		

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = V_{DD} = +4.75 to +5.25V, HC mode with attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	350MHz, T_C = +25°C (Notes 5, 8)	17	18.7		dBm
Second Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 5)	-61	-70		dBc
Third Harmonic		P_{OUT} = +3dBm, f_{RF} = 200MHz, T_C = +25°C (Note 5)	-74	-87		dBc
Attenuator Response Time (Note 9)		Input from ANALOG_VCTRL		1		µs
		Input from $\overline{CS}$ rising edge		3.2		
Group Delay		Maximum gain setting, includes EV kit PCB delays		0.8		ns
Input Return Loss		50Ω source, maximum gain setting		30		dB
Output Return Loss		50Ω load, maximum gain setting		16		dB
ANALOG ATTENUATOR						
Insertion Loss				1.2		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz, $f_1 + f_2$		70		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, maximum gain setting, Δf = 1MHz		36		dBm
Attenuation Range		Analog control input		31		dB
Gain-Control Slope		Analog control input		-12.5		dB/V
Maximum Gain-Control Slope		Over analog control input range		-35		dB/V
Insertion Phase Change		Over analog control input range		18		Degrees
Group Delay vs. Control Voltage		Over analog control input range		-0.25		ns
Analog Control Input Range			0.25		2.75	V
Analog Control Input Impedance				80		kΩ
Input Return Loss		50Ω source, maximum gain setting		22		dB
Output Return Loss		50Ω load, maximum gain setting		22		dB
DAC						
Number of Bits				8		Bits
Output Voltage		DAC code = 00000000			0.25	V
		DAC code = 11111111	2.75			

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = V_{DD} = +4.75 to +5.25V, HC mode with attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PERIPHERAL INTERFACE (SPI)						
Maximum Clock Speed	f_{CLK}			20		MHz
Data-to-Clock Setup Time	t_{CS}			2		ns
Data-to-Clock Hold Time	t_{CH}			2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}			3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}			7		ns
$\overline{CS}$ Setup Time	t_{EWS}			3.5		ns
Clock Pulse Width	t_{CW}			5		ns

Note 5: Guaranteed by design and characterization.

Note 6: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*

Note 7: Operating outside this range is possible, but with degraded performance of some parameters.

Note 8: It is advisable not to continuously operate the VGA RF input above +15dBm.

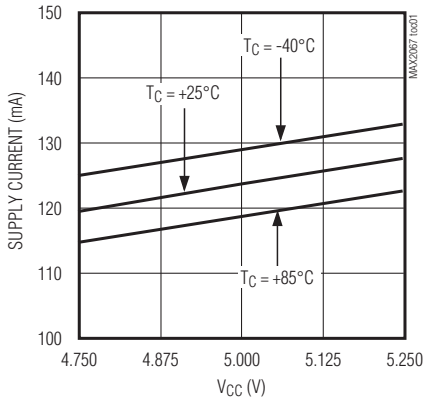
Note 9: Response time includes full attenuation range change with output setting to within ±0.1dB.

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

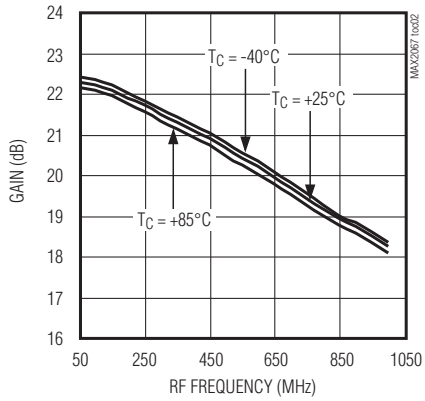
典型工作特性

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

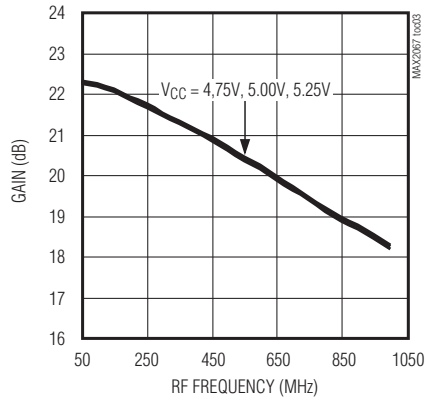
SUPPLY CURRENT vs. SUPPLY VOLTAGE



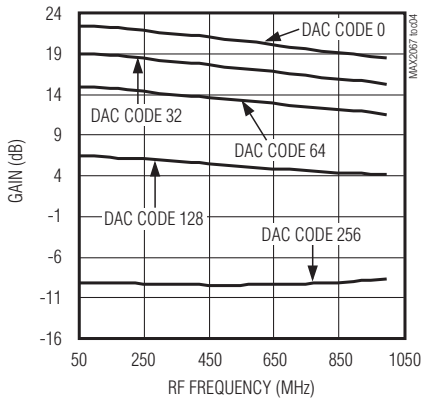
GAIN vs. RF FREQUENCY



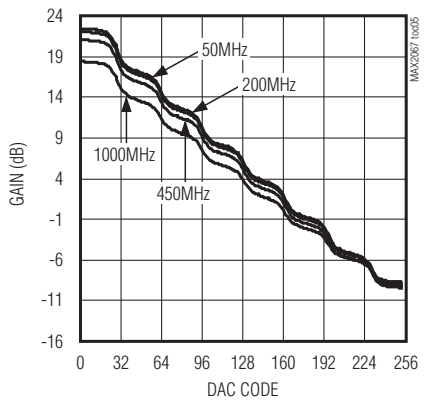
GAIN vs. RF FREQUENCY



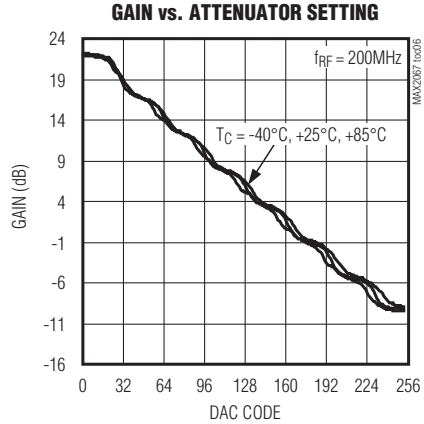
GAIN OVER ATTENENUATOR SETTING vs. RF FREQUENCY



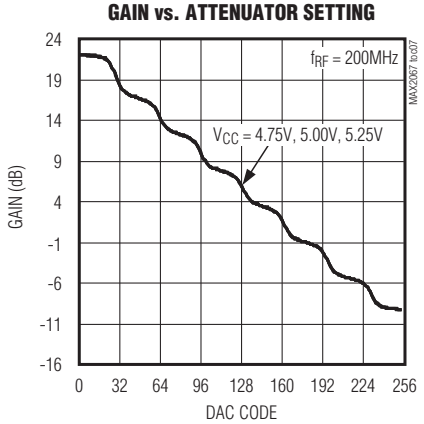
GAIN vs. ATTENUATOR SETTING



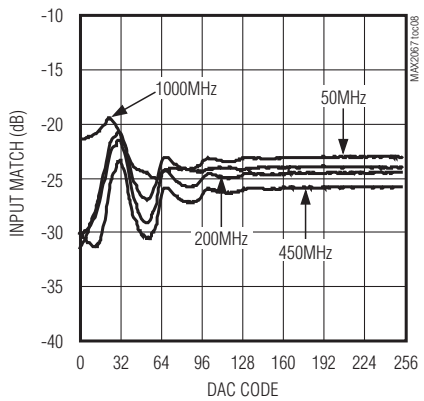
GAIN vs. ATTENUATOR SETTING



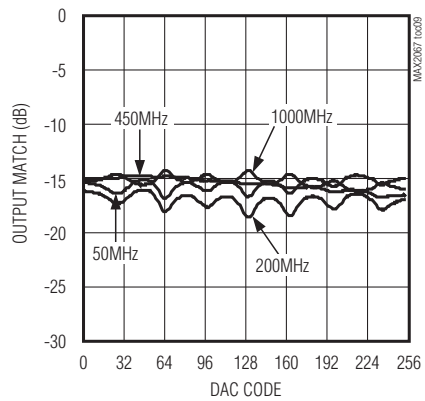
GAIN vs. ATTENUATOR SETTING



INPUT MATCH vs. ATTENUATOR SETTING



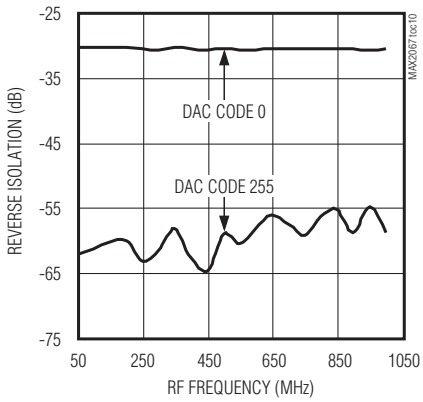
OUTPUT MATCH vs. ATTENUATOR SETTING



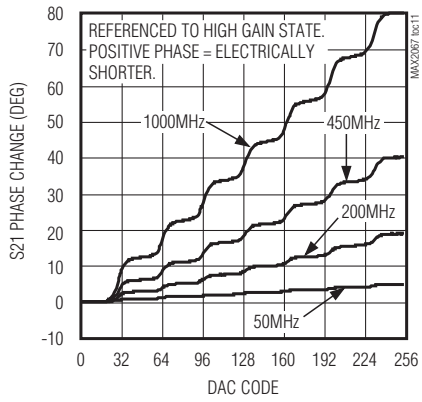
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

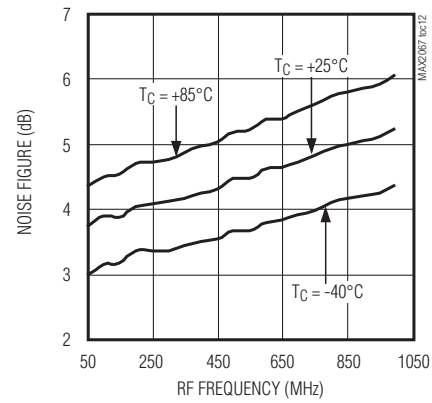
REVERSE ISOLATION OVER ATTENUATOR SETTING vs. RF FREQUENCY



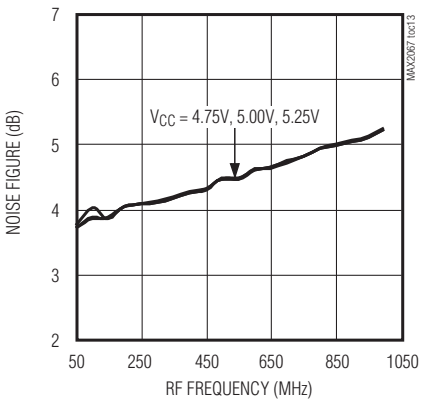
S21 PHASE CHANGE vs. ATTENUATOR SETTING



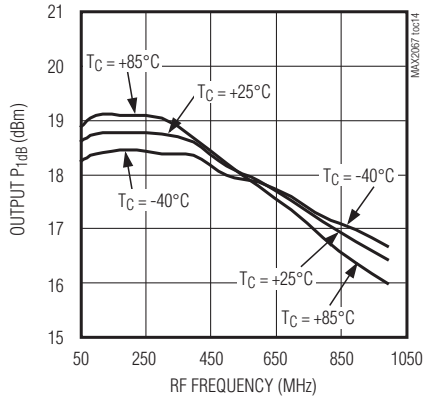
NOISE FIGURE vs. RF FREQUENCY



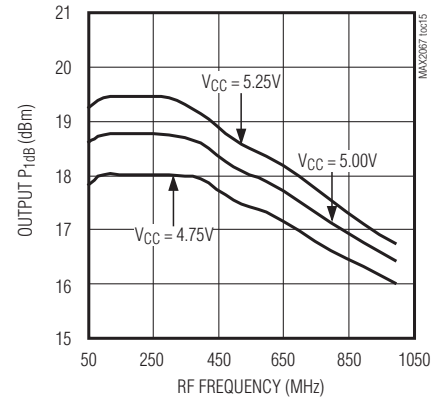
NOISE FIGURE vs. RF FREQUENCY



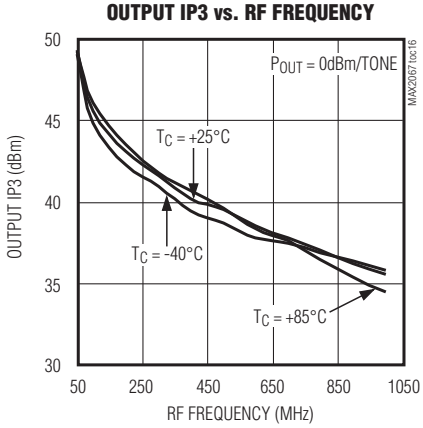
OUTPUT P_{1dB} vs. RF FREQUENCY



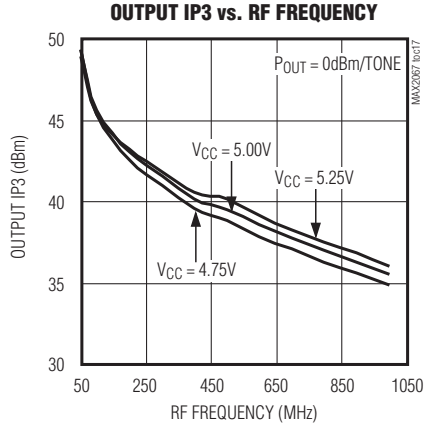
OUTPUT P_{1dB} vs. RF FREQUENCY



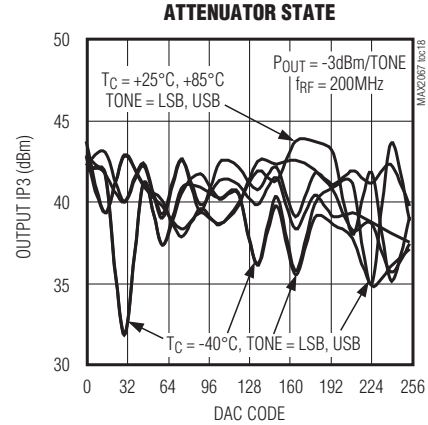
OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. ATTENUATOR STATE

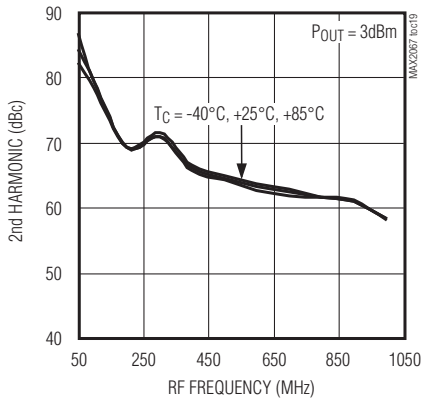


50MHz至1000MHz高线性度、可串行/模拟控制的VGA

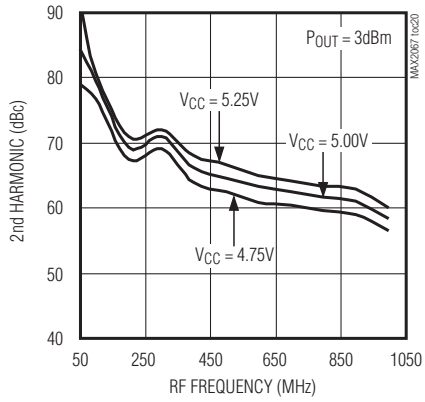
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

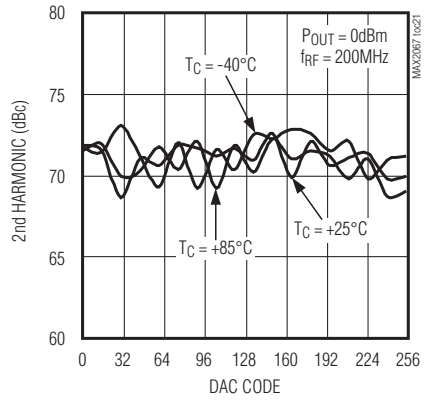
2nd HARMONIC vs. RF FREQUENCY



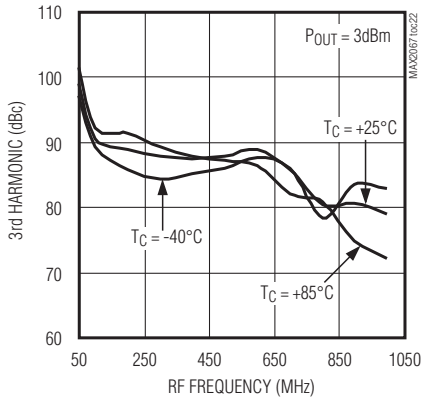
2nd HARMONIC vs. RF FREQUENCY



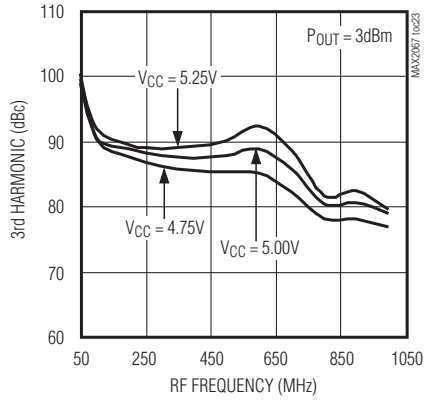
2nd HARMONIC vs. ATTENUATOR STATE



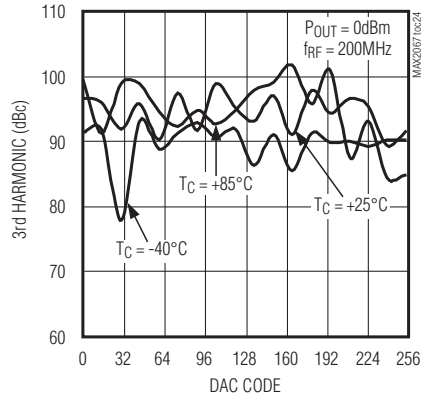
3rd HARMONIC vs. FREQUENCY



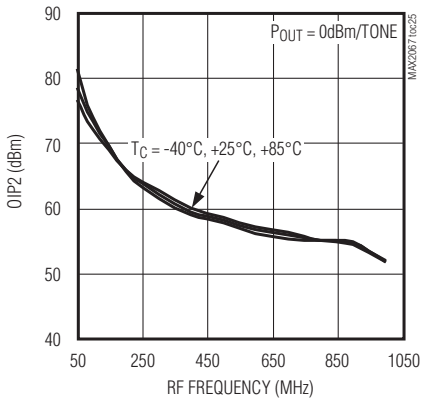
3rd HARMONIC vs. RF FREQUENCY



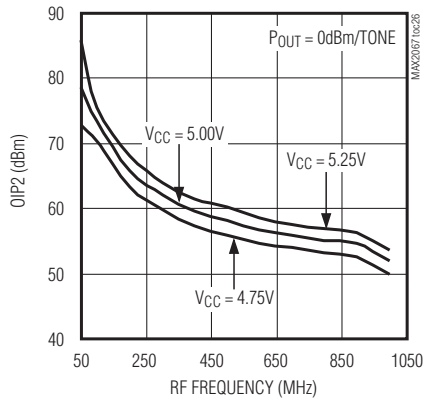
3rd HARMONIC vs. ATTENUATOR STATE



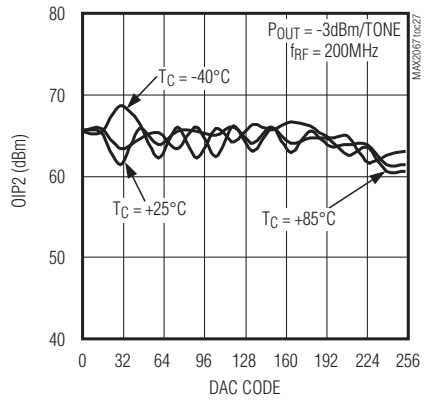
OIP2 vs. RF FREQUENCY



OIP2 vs. RF FREQUENCY



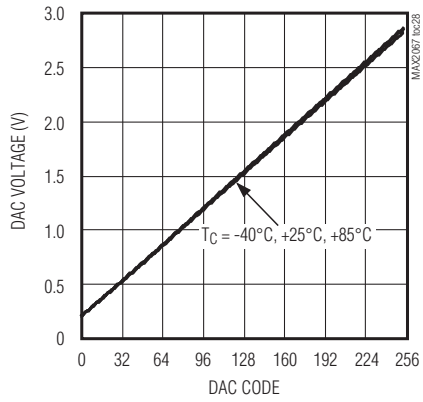
OIP2 vs. ATTENUATOR STATE



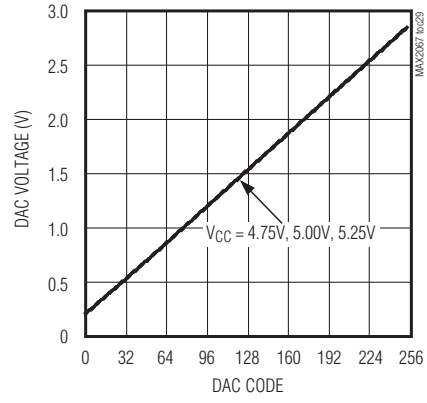
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

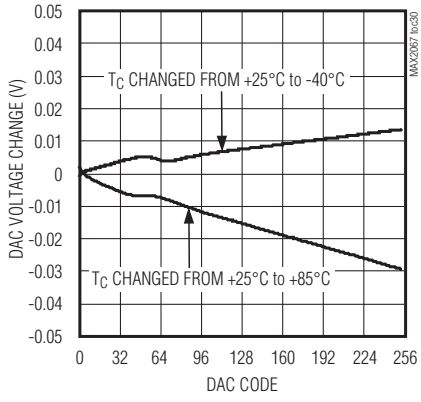
DAC VOLTAGE USING INTERNAL REFERENCE vs. DAC CODE



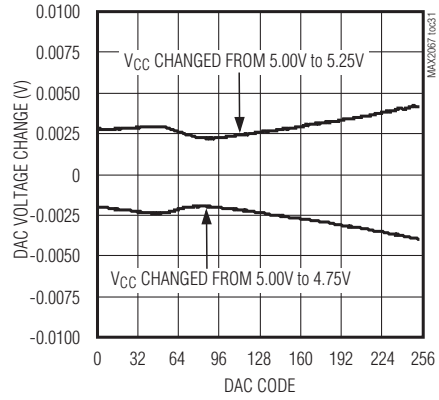
DAC VOLTAGE USING INTERNAL REFERENCE vs. DAC CODE



DAC VOLTAGE DRIFT USING INTERNAL REFERENCE vs. DAC CODE



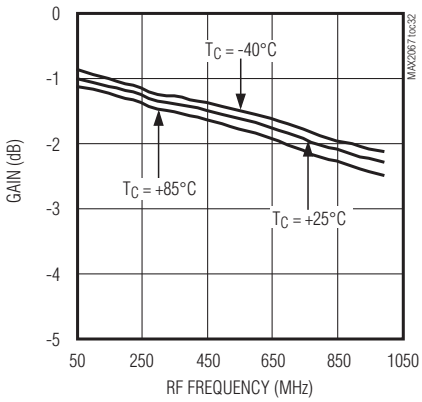
DAC VOLTAGE DRIFT USING INTERNAL REFERENCE vs. DAC CODE



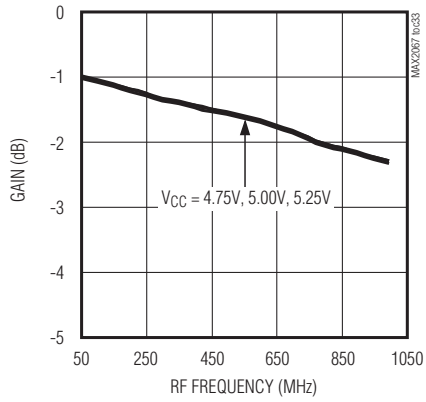
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, attenuator only**, maximum gain, P_{IN} = -20dBm, and T_C = +25°C, unless otherwise noted.)

GAIN vs. RF FREQUENCY (ATTENUATOR ONLY)



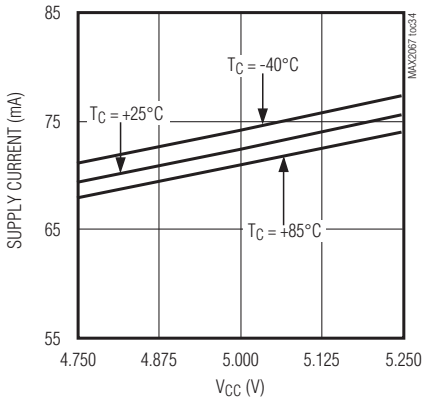
GAIN vs. RF FREQUENCY (ATTENUATOR ONLY)



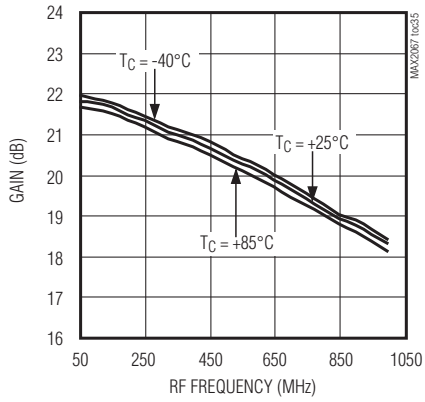
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

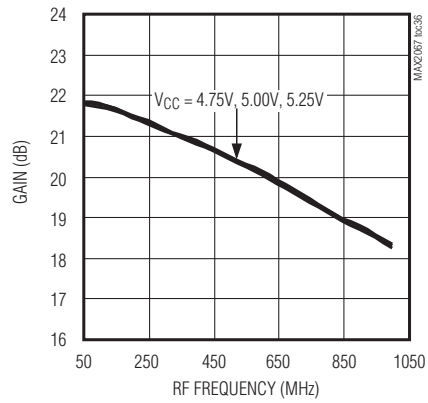
SUPPLY CURRENT vs. SUPPLY VOLTAGE (LOW-CURRENT MODE)



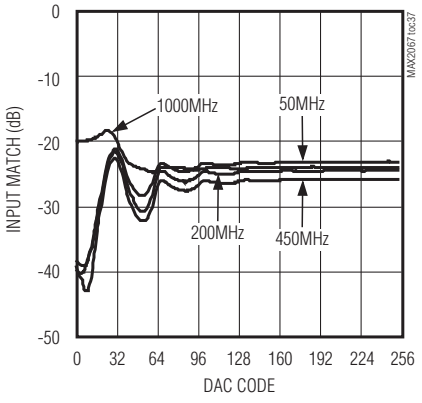
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



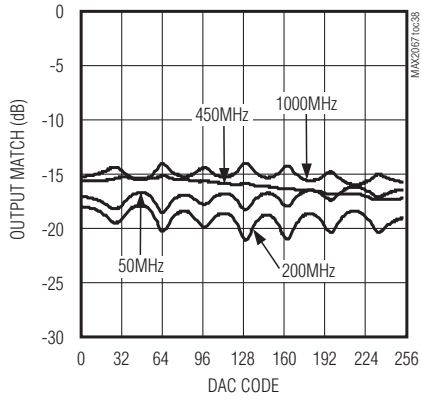
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



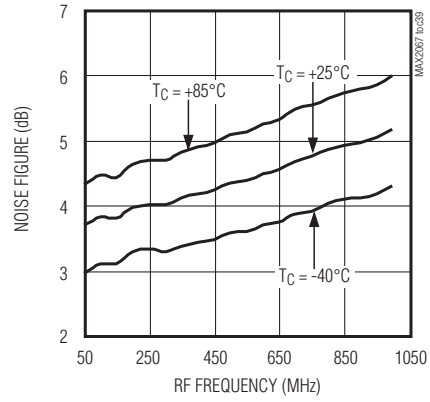
INPUT MATCH vs. ATTENUATOR SETTING (LOW-CURRENT MODE)



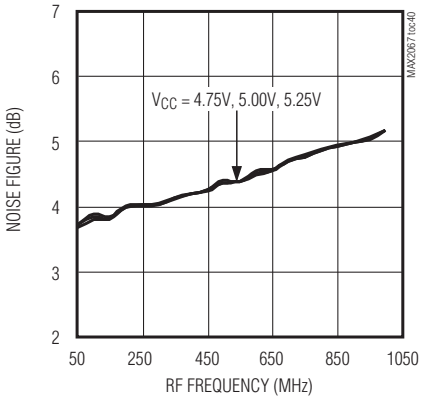
OUTPUT MATCH vs. ATTENUATOR SETTING (LOW-CURRENT MODE)



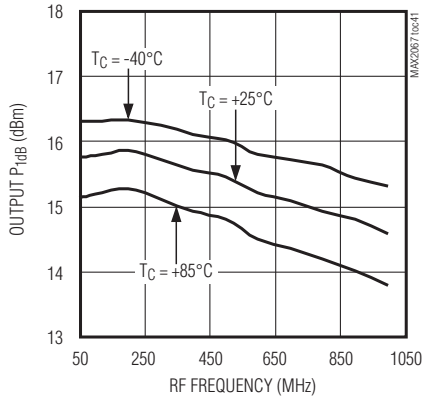
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



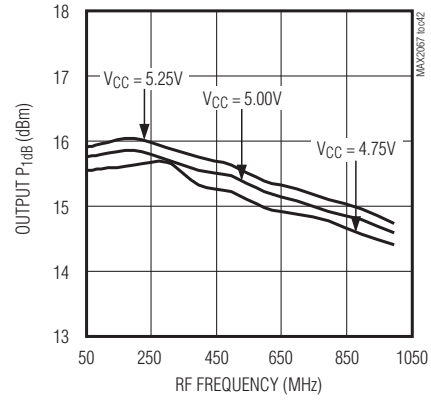
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P_{1dB} vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P_{1dB} vs. RF FREQUENCY (LOW-CURRENT MODE)

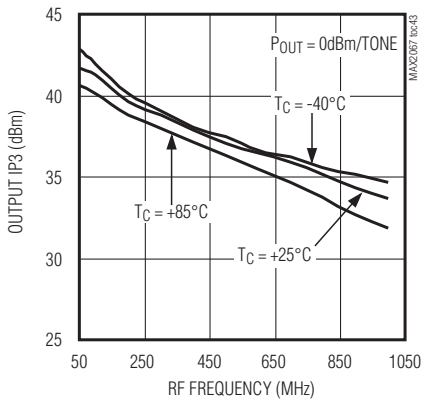


50MHz至1000MHz高线性度、可串行/模拟控制的VGA

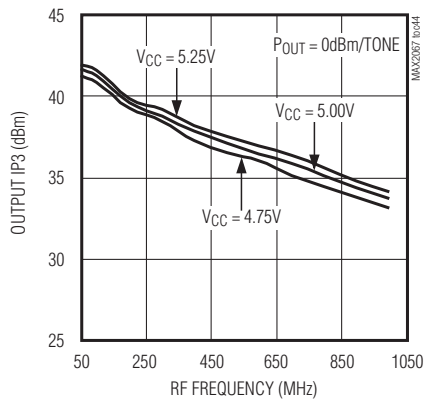
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

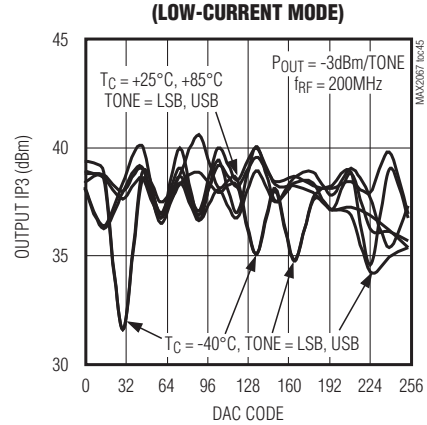
OUTPUT IP3 vs. RF FREQUENCY (LOW-CURRENT MODE)



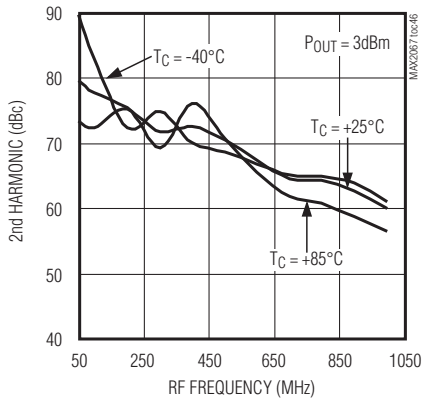
OUTPUT IP3 vs. RF FREQUENCY (LOW-CURRENT MODE)



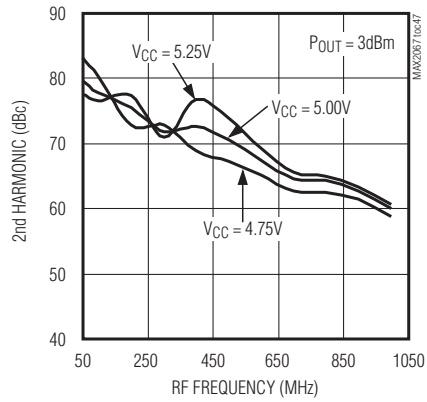
OUTPUT IP3 vs. ATTENUATOR STATE (LOW-CURRENT MODE)



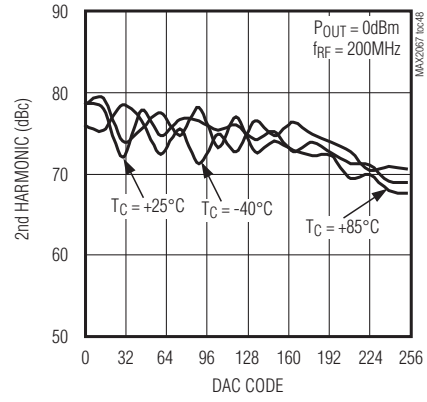
2nd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



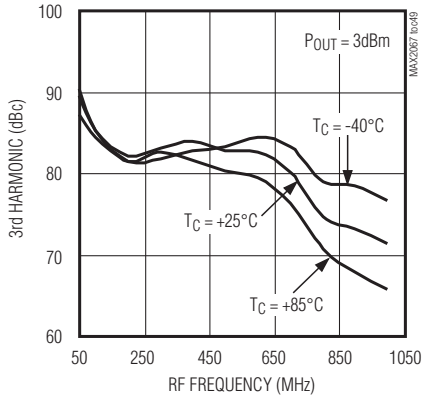
2nd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



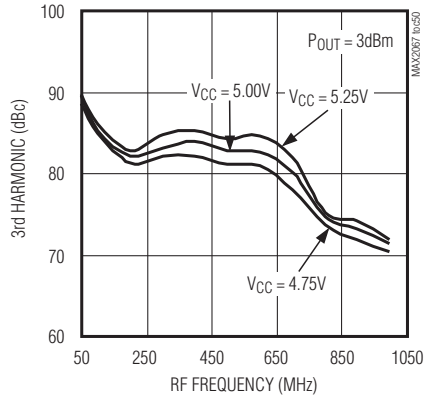
2nd HARMONIC vs. ATTENUATOR STATE (LOW-CURRENT MODE)



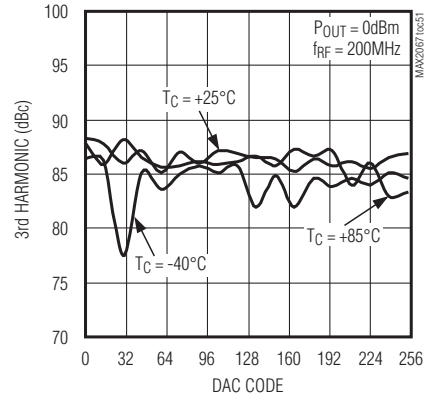
3rd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



3rd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



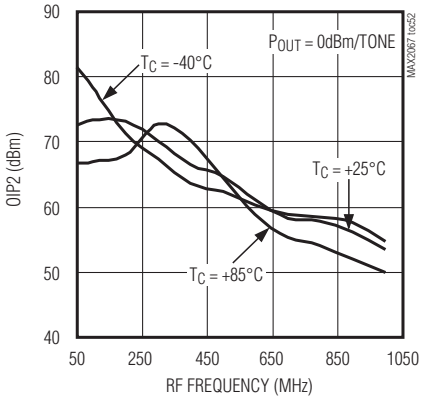
3rd HARMONIC vs. ATTENUATOR STATE (LOW-CURRENT MODE)



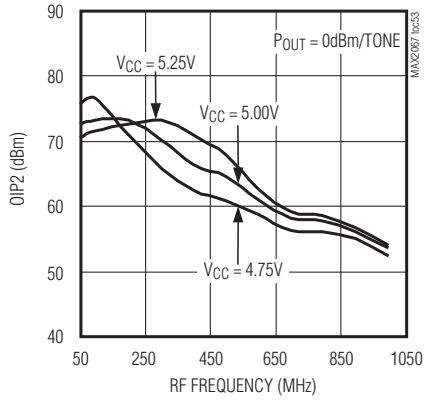
典型工作特性(续)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

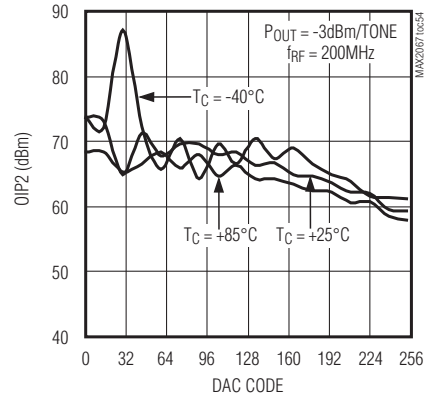
OIP2 vs. RF FREQUENCY (LOW-CURRENT MODE)



OIP2 vs. RF FREQUENCY (LOW-CURRENT MODE)



OIP2 vs. ATTENUATOR STATE (LOW-CURRENT MODE)

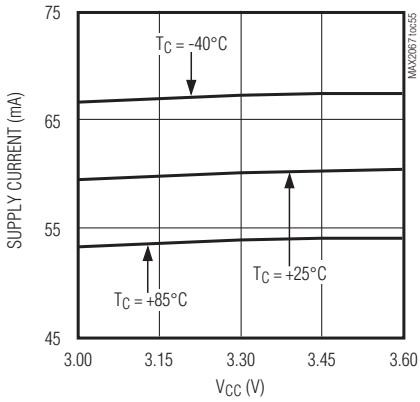


50MHz至1000MHz高线性度、可串行/模拟控制的VGA

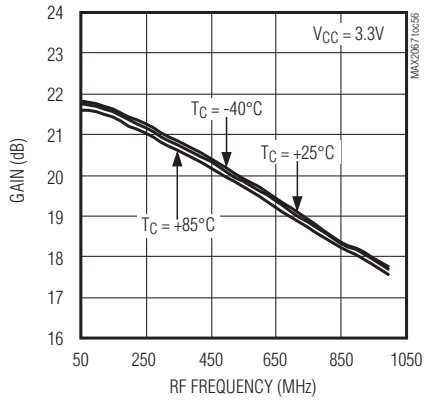
典型工作特性(续)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

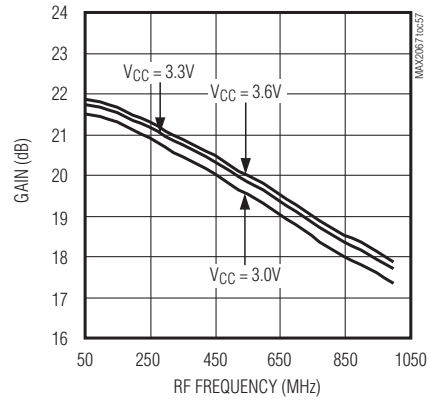
SUPPLY CURRENT vs. SUPPLY VOLTAGE



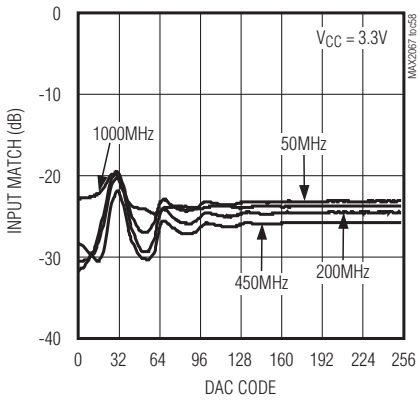
GAIN vs. RF FREQUENCY



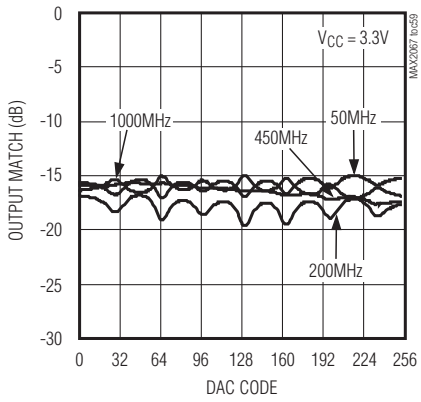
GAIN vs. RF FREQUENCY



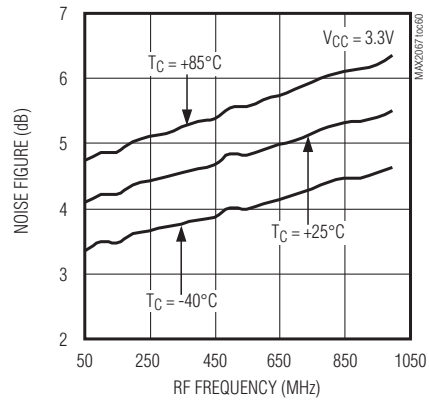
INPUT MATCH vs. ATTENUATOR SETTING



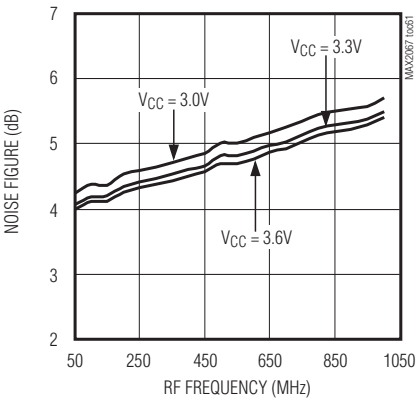
OUTPUT MATCH vs. ATTENUATOR SETTING



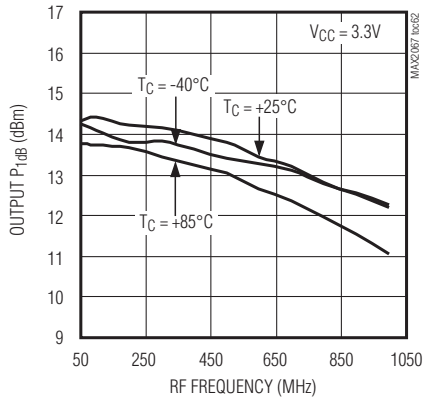
NOISE FIGURE vs. RF FREQUENCY



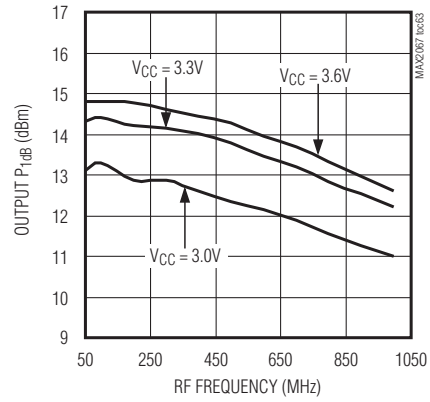
NOISE FIGURE vs. RF FREQUENCY



OUTPUT P_{1dB} vs. RF FREQUENCY



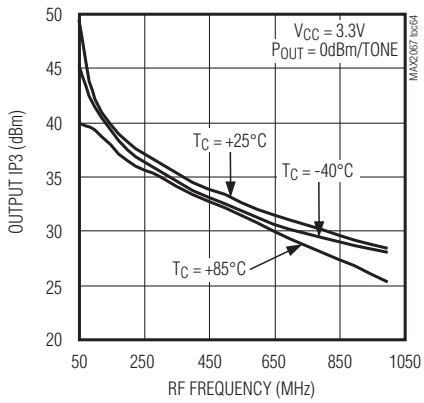
OUTPUT P_{1dB} vs. RF FREQUENCY



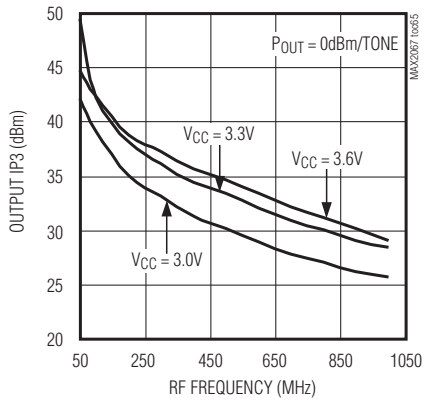
典型工作特性(续)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

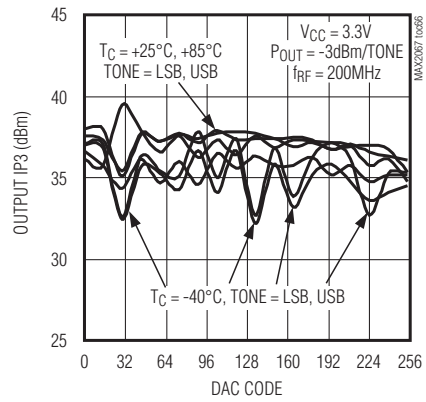
OUTPUT IP3 vs. RF FREQUENCY



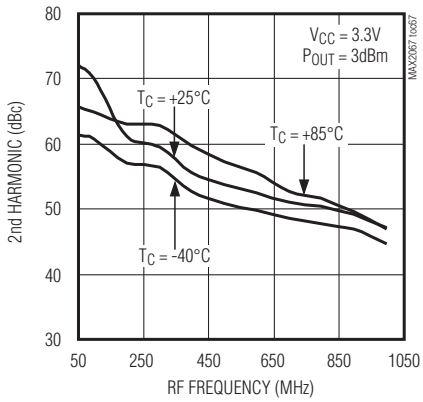
OUTPUT IP3 vs. RF FREQUENCY



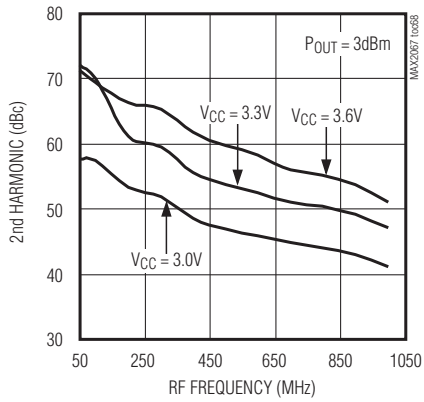
OUTPUT IP3 vs. ATTENUATOR STATE



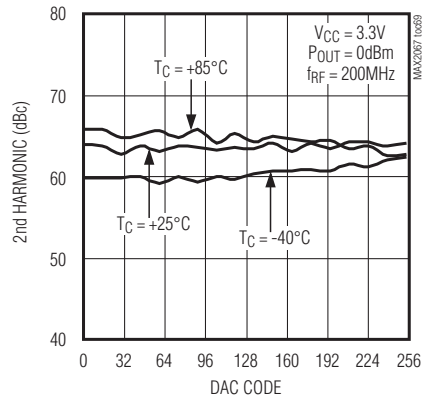
2nd HARMONIC vs. RF FREQUENCY



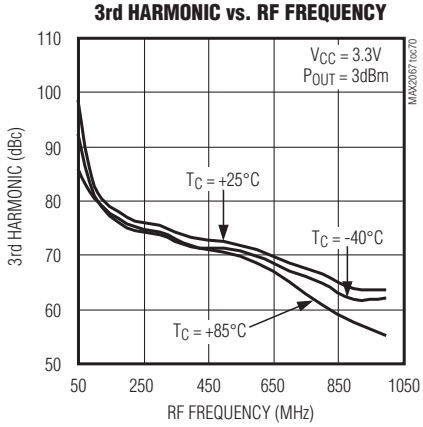
2nd HARMONIC vs. RF FREQUENCY



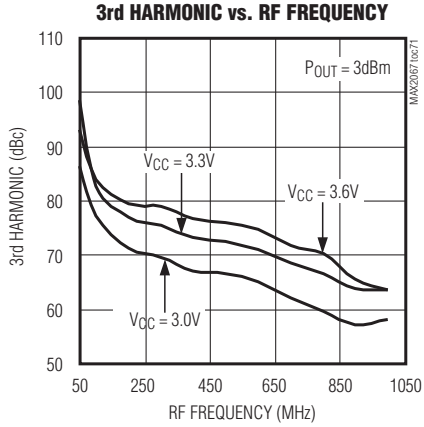
2nd HARMONIC vs. ATTENUATOR STATE



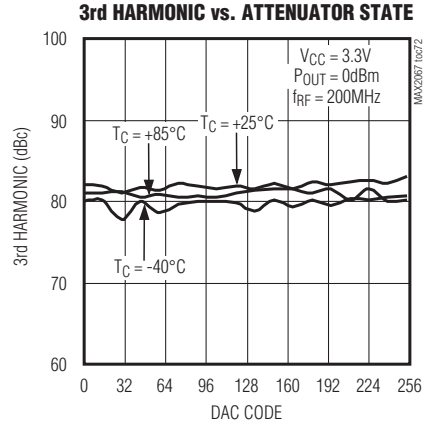
3rd HARMONIC vs. RF FREQUENCY



3rd HARMONIC vs. RF FREQUENCY



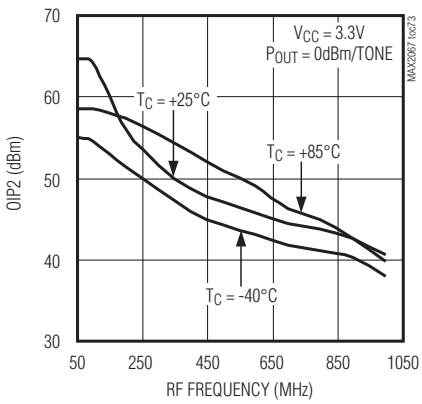
3rd HARMONIC vs. ATTENUATOR STATE



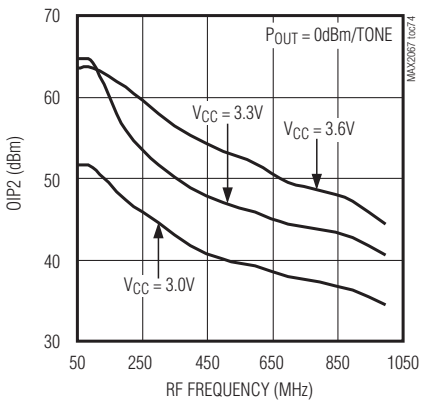
典型工作特性(续)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, internal DAC reference used, unless otherwise noted.)

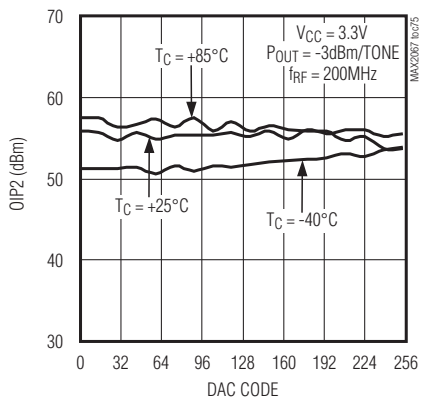
OIP2 vs. RF FREQUENCY



OIP2 vs. RF FREQUENCY



OIP2 vs. ATTENUATOR STATE



引脚说明

引脚	名称	功能
1, 16, 19, 22, 24–28, 30, 31, 33–36	GND	地。
2	VREF_SELECT	DAC基准电压选择逻辑输入。逻辑1 = 内部DAC基准电压；逻辑0 = 外部DAC基准电压。当VDAC_EN = 逻辑0时，逻辑输入被禁用(可忽略)。
3	VDAC_EN	DAC使能/关闭控制逻辑输入。逻辑0 = 关闭DAC电路；逻辑1 = 打开DAC电路。
4	DATA	SPI数字数据输入。
5	CLK	SPI数字时钟输入。
6	$\overline{CS}$	SPI数字片选输入。
7	VDD_LOGIC	数字逻辑电路供电输入，连接到数字逻辑电源，V_{DD}。在尽可能靠近该引脚的位置安装10nF电容，将其旁路至GND。
8–15, 23, 29	GND	地，请参考*引脚兼容性考虑*部分。
17	AMP_OUT	放大器驱动输出(50Ω)，详细信息请参考*典型应用电路*。
18	RSET	放大器驱动偏置电流设置，请参考*外部偏置*部分。
20	AMP_IN	放大器驱动输入(50Ω)，详细信息请参考*典型应用电路*。
21	VCC_AMP	放大器驱动电源输入，连接到电源V_{CC}。在尽可能靠近该引脚的位置安装1000pF和10nF电容，将其旁路至GND，较小容值的电容离器件更近。
32	ATTEN_OUT	模拟衰减器输出，内部匹配至50Ω。需外接隔直流电容。
37	ATTEN_IN	模拟衰减器输入，内部匹配至50Ω。需外接隔直流电容。
38	VCC_ANALOG	模拟偏置和控制电路电源输入。在尽可能靠近该引脚的位置安装10nF电容，将其旁路至GND。
39	ANALOG_VCTRL	模拟衰减器控制电压输入。
40	VREF_IN	外部DAC基准电压输入。
—	EP	裸焊盘，内部连接到GND。将EP连接至GND有利于改善RF性能和散热。

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

详细说明

MAX2067高线性度模拟可变增益放大器是一款通用的高性能放大器，针对50MHz至1000MHz频率范围、50Ω系统接口的应用而设计。

MAX2067集成了一个模拟衰减器，可提供31dB的增益控制，同时可优化放大器驱动设计来提供高增益、高IP3、低噪声系数和低功耗指标。在对线性度要求不高的应用中，可通过调节外部电阻改变放大器的偏置电流，以进一步降低功耗。

利用外部电压或通过SPI接口控制片上8位DAC，实现衰减器的模拟调节。因为每级电路都具有RF输入和RF输出，通过适当配置可以优化NF (第1级为放大器)或OIP3 (最后一级为放大器)。该器件还包含具有22dB增益的放大器(放大器本身)，增益最大时NF为4dB (包括衰减器的插入损耗)，并提供+43dBm的高OIP3。这些特性使得MAX2067能够为众多接收器和发射器提供一个理想的VGA。

另外，MAX2067采用+5V单电源供电，提供功能完备的解决方案；工作在+3.3V时，性能指标略有降低，可调节偏置电流在电流损耗和线性度方面进行折衷。

模拟衰减器

MAX2067集成的模拟衰减器具有31dB的动态范围，可利用外部电压或通过3线SPI控制片上8位DAC实现衰减器调节。请参考*应用信息*和表1所示衰减器设置，获得更多信息。该衰减器可用于静态和动态功率控制。

驱动器放大器

MAX2067包括一个22dB固定增益的高性能驱动器。该驱动器放大器优化于50MHz至1000MHz频率范围的高线性度指标。

应用信息

衰减器控制

在ANALOG_VCTRL (第39引脚)施加一个外部控制电压或通过片上8位DAC控制模拟衰减器，借助DAC控制，用户可以方便地通过SPI指令以0.12dB的步长增量调节模拟衰减器。DAC使能/禁止逻辑输入引脚(VDAC_EN)以及DAC基准电压选择逻辑输入引脚(VREF_SELECT)决定以何种方式控制衰减器。当DAC使能时，允许选择内部基准或外部基准。请参考表1所示衰减器和DAC工作真值表。

片上DAC无需使用外部模拟控制电压。当然，用户也可以选择禁止DAC工作，而利用外部模拟电压进行控制，例如：对于需要额外的衰减控制分辨率的应用，或者增益微调/自动增益控制(AGC)环路要求采用真正的模拟信号调节的应用。

SPI接口和衰减器设置

MAX2067采用3线SPI/MICROWIRE™兼容串行接口控制片上DAC。移入8位数据，MSB在前，并通过$\overline{CS}$打包。当$\overline{CS}$为低电平时，时钟有效，数据在时钟的上升沿移入。当$\overline{CS}$跳变到高电平时，数据被锁存，改变衰减器设置(图1)。表2给出了SPI数据格式的详细信息。

表1. 控制逻辑

VDAC_EN	VREF_SELECT	ANALOG ATTENUATOR	D/A CONVERTER
0	X	Controlled by external control voltage	Disabled
1	1	Controlled by on-chip DAC	Enabled (DAC uses on-chip voltage reference)
1	0	Controlled by on-chip DAC	Enabled (DAC uses external voltage reference)

X = 无关。

MICROWIRE是National Semiconductor Corp.的商标。

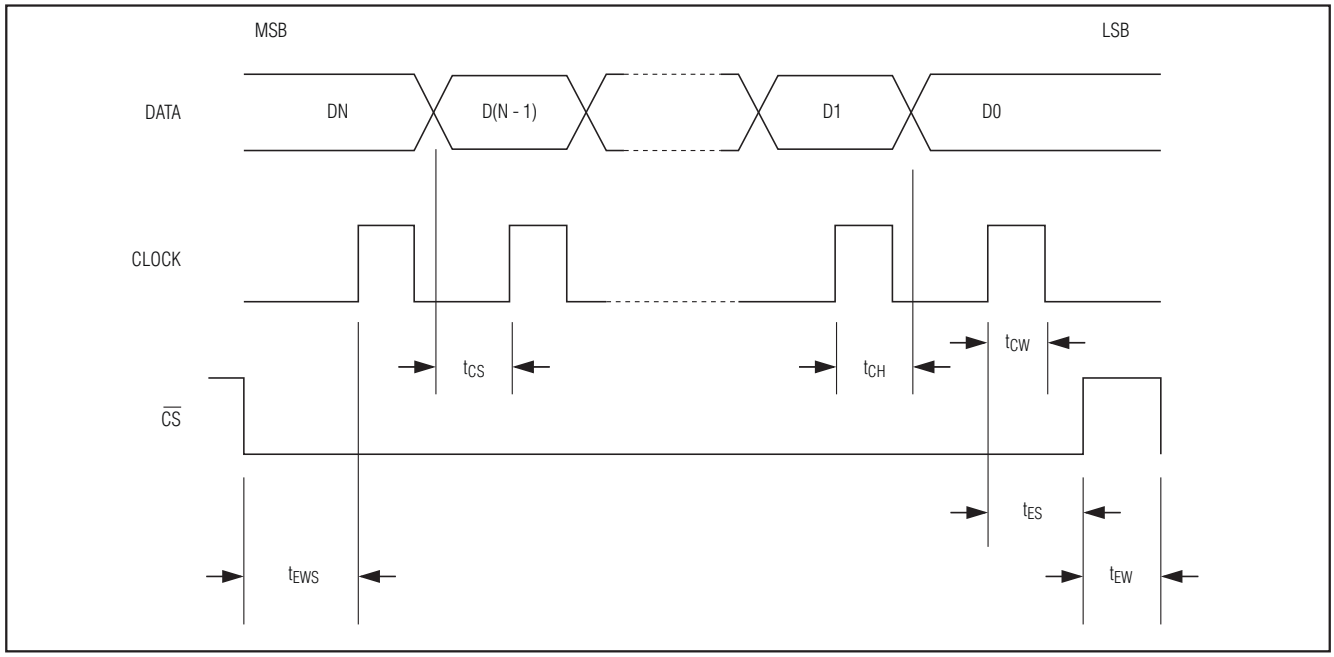


图1. SPI时序图

表2. SPI数据格式

FUNCTION	BIT	DESCRIPTION
On-Chip DAC	D7	Bit 7 (MSB) of on-chip DAC used to program the analog attenuator
	D6	Bit 6 of DAC
	D5	Bit 5 of DAC
	D4	Bit 4 of DAC
	D3	Bit 3 of DAC
	D2	Bit 2 of DAC
	D1	Bit 1 of DAC
	D0 (LSB)	Bit 0 (LSB) of the on-chip DAC

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

外部偏置

驱动放大器偏置电流可通过外部电阻设置并进行优化。将电阻R1和R1A连接到RSET (引脚18)，可以设置放大器的偏置电流。增大外部偏置电阻可降低工作电流，代价是降低系统性能。详细信息请参考表4和表5。

引脚兼容性考虑

MAX2067是MAX2065模拟/数字VGA的简化版本，MAX2067不含数字衰减器和并行输入D0–D4。相应的输入/输出引脚在内部接地(表3)。将不使用的输入/输出引脚接地有助于提高隔离度(请参考*典型应用电路*)。

+5V和+3.3V供电

MAX2067的另外一个供电选择是采用+3.3V供电，但在这种情况下系统的线性指标略有下降。

布局考虑

MAX2067经过优化的引脚配置有助于实现紧凑的器件布局和相关分立元件的布局。

MAX2067采用40引脚薄型QFN-EP封装，其裸焊盘(EP)提供了一条到管芯的低热阻通道。安装MAX2067的PCB设计需要利用EP散热，这一点非常关键。另外，EP与电气地的连接需要通过低电感路径。EP**必须**直接或通过一系列过孔焊接到PCB的地层。

表3. MAX2065/MAX2067引脚兼容性

PIN	MAX2065	MAX2067
8	SER/PAR	GND
9	STATE_A	GND
10	STATE_B	GND
11	D4	GND
12	D3	GND
13	D2	GND
14	D1	GND
15	D0	GND
23	ATTEN2_OUT	GND
29	ATTEN2_IN	GND

表4. 典型应用电路元件值(HC模式)

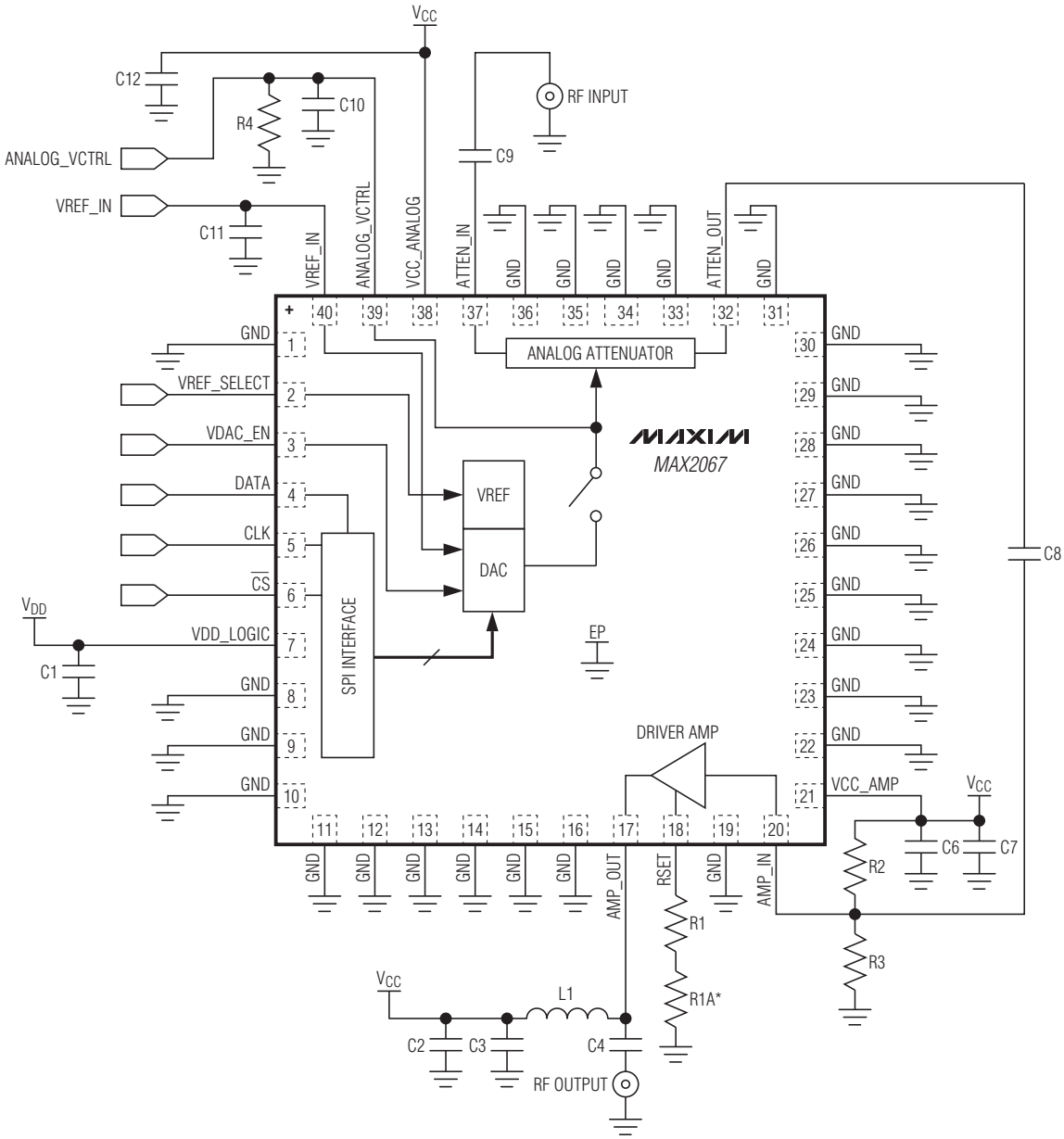
DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C12	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
C10, C11	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1, R1A	10Ω	0402	Panasonic Corp.	1%
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2067ETL+

表5. 典型应用电路元件值(LC模式)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7, C12	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
C10, C11	150pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1	24Ω	0402	Vishay	1%
R1A	10nF	0402	Murata Mfg. Co., Ltd.	X7R
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
R4 (+5V applications and using internal DAC only)	47kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2067ETL+

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

典型应用电路

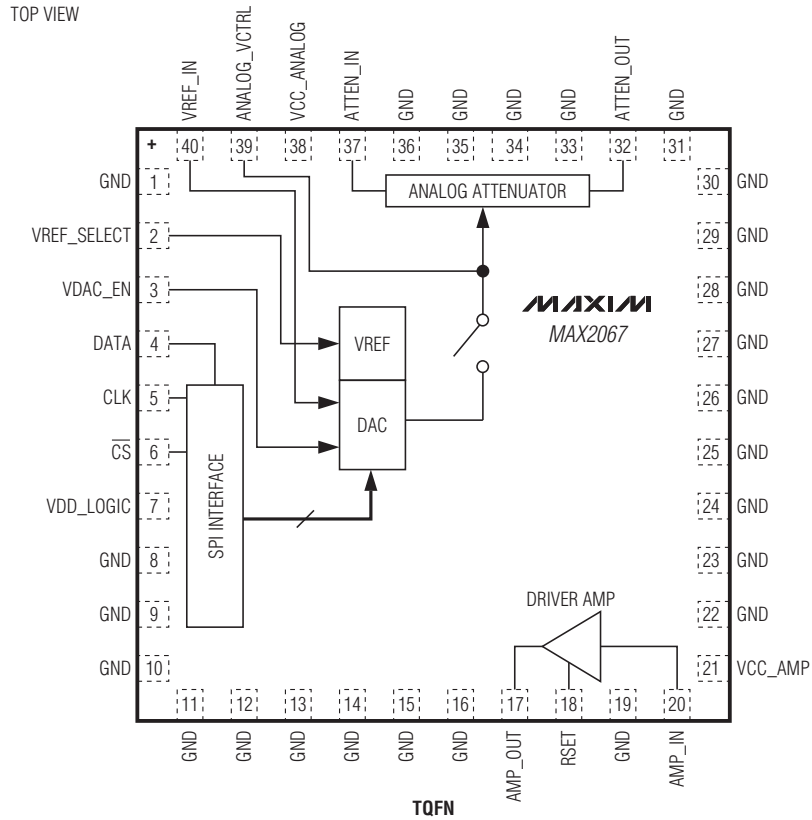


NOTE: REMOVE R4 AND C10 WHEN DRIVING ANALOG_VCTRL WITH AN EXTERNAL VOLTAGE.

*IN LC MODE, R1A IS A 10nF CAPACITOR. SEE TABLE 5 FOR DETAILS.

50MHz至1000MHz高线性度、可串行/模拟控制的VGA

引脚配置/功能框图



芯片信息

PROCESS: SiGe BiCMOS

封装信息

(如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

封装类型	封装代码	文档编号
40薄型QFN-EP	T4066-3	**21-0141**