19-0832; Rev 0; 6/07

可提供评估板

完备的直接变频调谐器，用于DVB-S和免费广播系统

MAX2120

概述

MAX2120低成本、直接变频调谐器IC设计用于卫星机顶盒和VSAT设备。该IC非常适合QPSK、数字视频广播(DVB-S)、DSS和免费广播设备。

MAX2120使用宽带I/Q下变频器直接将卫星信号从LNB变频至基带。工作频率范围为925MHz至2175MHz。

器件包含LNA、RF可变增益放大器、I/Q下变频混频器、具有可编程截止频率控制的基带低通滤波器和数字控制可变增益基带放大器。RF和基带可变增益放大器相结合，能够提供大于80dB的增益控制范围。该IC完全兼容于任何QPSK解调器。

MAX2120包含完整的单芯片VCO及频率合成器，另外，片内晶体振荡器具有缓冲输出，用于驱动附加的调谐器和解调器。通过2线串行接口实现合成器的编程和器件配置。该IC提供VCO自动选择(VAS)功能，自动选择适当的VCO。在多调谐器应用中，该器件可以配置为两个2线接口地址的一个。低功耗待机模式下关断信号通路，参考时钟振荡器、数字接口和缓冲器保持工作状态，为单调谐器、多调谐器应用提供了一个降低功耗的途径。

MAX2120是目前最先进的DBS调谐器，极低的噪声系数省去了外部LNA。仅需少量无源器件即可构建完整的DVB、DBS或VSAT RF前端方案。该调谐器提供小尺寸、28引脚薄型QFN封装。

应用

DirecTV和蝶形网络DBS

DVB-S

双向卫星通信系统

VSAT

免费广播设备

特性

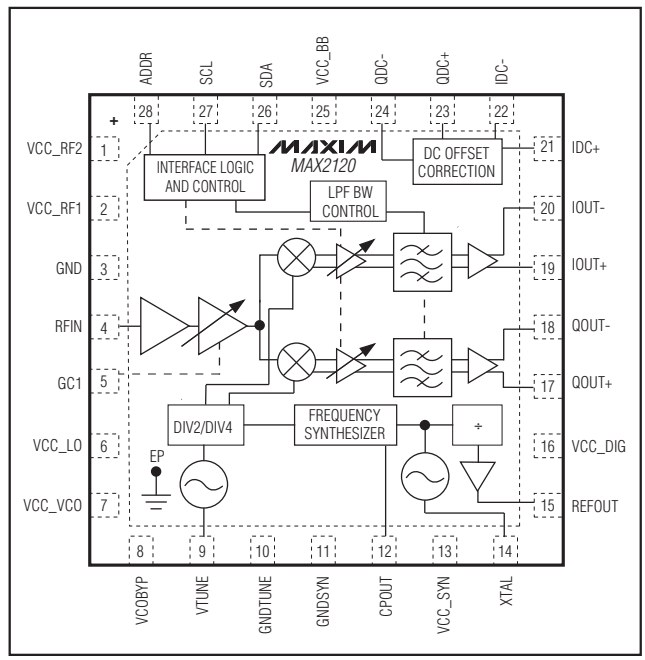
- ♦ 925MHz至2175MHz频率范围
- ♦ 单片VCO：无需校准
- ♦ -75dBm至0dBm高动态范围
- ♦ 集成4MHz至40MHz可调节带宽的低通滤波器
- ♦ 单电源+3.3V ±5%供电
- ♦ 低功耗待机模式
- ♦ 提供多个适合多调谐器应用的2线地址
- ♦ 差分I/Q接口
- ♦ I^2C 2线串行接口
- ♦ 微小的28引脚薄型QFN封装

定购信息

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX2120CTI+	0°C to +70°C	28 Thin QFN-EP*	T2855+3

EP = 裸焊盘。
+表示无铅封装。

引脚配置/功能框图



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ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +3.9V
All Other Pins to GND.....-0.3V to (V_{CC} + 0.3V)
RF Input Power: RFIN.....+10dBm
VCOBYP, CPOUT, REFOUT, XTAL, IOUT_, QOUT_, IDC_, and QDC_ Short-Circuit Protection.....10s

Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derated 34.5mW/°C above +70°C).....2.75W
Operating Temperature Range.....0°C to +70°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Soldering Temperature (10s) .....+260°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2120 Evaluation Kit: V_{CC} = +3.13V to +3.47V, V_{GC1} = +0.5V (max gain), T_A = 0°C to +70°C. No input signals at RF, baseband I/Os are open circuited, and LO frequency = 2150MHz. Default register settings except ICP = 1 and BBG[3:0] = 1011. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Voltage		3.13	3.3	3.47	V
Supply Current	Receive mode, bit STBY = 0		100	160	mA
	Standby mode, bit STBY = 1		3		
ADDRESS SELECT INPUT (ADDR)					
Digital Input-Voltage High, V_{IH}		2.4			V
Digital Input-Voltage Low, V_{IL}				0.5	V
Digital Input-Current High, I_{IH}				50	µA
Digital Input-Current Low, I_{IL}		-50			µA
ANALOG GAIN-CONTROL INPUTS (GC)					
Input Voltage Range	Maximum gain = 0.5V	0.5		2.7	V
Input Bias Current		-50		+50	µA
VCO TUNING VOLTAGE INPUT (VTUNE)					
Input Voltage Range		0.4		2.3	V
2-WIRE SERIAL INPUTS (SCL, SDA)					
Clock Frequency				400	kHz
Input Logic-Level High		0.7 x V_{CC}			V
Input Logic-Level Low				0.3 x V_{CC}	V
Input Leakage Current	Digital inputs = GND or V_{CC}		±0.1	±1	µA
2-WIRE SERIAL OUTPUT (SDA)					
Output Logic-Level Low	I_{SINK} = 1mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

(MAX2120 Evaluation Kit: V_{CC} = +3.13V to +3.47V, V_{GC1} = +0.5V (max gain), T_A = 0°C to +70°C. Default register settings except ICP = 1 and BBG[3:0] = 1011. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SIGNAL PATH PERFORMANCE					
Input Frequency Range	(Note 2)	925		2175	MHz
RF Gain-Control Range (GC1)	0.5V < V_{GC1} < 2.7V	65	73		dB
Baseband Gain-Control Range	Bits GC2 = 1111 to 0000	13	15		dB
In-Band Input IP3	(Note 3)		+2		dBm
Out-of-Band Input IP3	(Note 4)		+15		dBm
Input IP2	(Note 5)		+40		dBm
Adjacent Channel Protection	(Note 6)		25		dB
Noise Figure	V_{GC1} is set to 0.5V (maximum RF gain) and BBG[3:0] is adjusted to give a $1V_{P-P}$ baseband output level for a -75dBm CW input tone at 1500MHz		8		dB
	Starting with the same BBG[3:0] setting as above, V_{GC1} is adjusted to back off RF gain by 10dB (Note 7)		9	12	
Minimum RF Input Return Loss	925MHz < f_{RF} < 2175MHz, in 75Ω system		12		dB
BASEBAND OUTPUT CHARACTERISTICS					
Nominal Output Voltage Swing	R_{LOAD} = 2kΩ//10pF	0.5	1		V_{P-P}
I/Q Amplitude Imbalance	Measured at 500kHz; filter set to 22.27MHz			±1	dB
I/Q Quadrature Phase Imbalance	Measured at 500kHz; filter set to 22.27MHz			3.5	Degrees
Single-Ended I/Q Output Impedance	Real Z_O, from 1MHz to 40MHz		30		Ω
Output 1dB Compression Voltage	Differential		3		V_{P-P}
Baseband Highpass -3dB Frequency Corner	47nF capacitors at IDC_, QDC_		400		Hz
BASEBAND LOWPASS FILTERS					
Filter Bandwidth Range		4		40	MHz
Rejection Ratio	At 2 x f_{-3dB}		39		dB
Group Delay	Up to 1dB bandwidth		37		ns
Ratio of In-Filter-Band to Out-of-Filter-Band Noise	f_{INBAND} = 100Hz to 22.5MHz, $f_{OUTBAND}$ = 87.5MHz to 112.5MHz		25		dB
FREQUENCY SYNTHESIZER					
RF-Divider Frequency Range		925		2175	MHz
RF-Divider Range (N)		16		2175	
Reference-Divider Frequency Range		4		30	MHz
Reference-Divider Range (R)		1		31	
Phase-Detector Comparison Frequency		1		2	MHz

AC ELECTRICAL CHARACTERISTICS (continued)

MAX2120 Evaluation Kit: V_{CC} = +3.13V to +3.47V, V_{GC1} = +0.5V (max gain), T_A = 0°C to +70°C. Default register settings except ICP = 1 and BBG[3:0] = 1011. Typical values measured at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE-CONTROLLED OSCILLATOR AND LO GENERATION					
Guaranteed LO Frequency Range	T_A = 0°C to +70°C	925		2175	MHz
LO Phase Noise	f_{OFFSET} = 10kHz		-82		dBc/Hz
	f_{OFFSET} = 100kHz		-102		
	f_{OFFSET} = 1MHz		-122		
XTAL/REFERENCE OSCILLATOR INPUT AND OUTPUT BUFFER					
XTAL Oscillator Frequency Range	Parallel-resonance-mode crystal	4		8	MHz
Input Overdrive Level	AC-coupled sine wave input	0.5	1	2.0	V_{P-P}
XTAL Output-Buffer Divider Range		1		8	
XTAL Output Voltage Swing	4MHz to 30MHz, C_{LOAD} = 10pF	1	1.5	2	V_{P-P}
XTAL Output Duty Cycle			50		%

Note 1: Min/max values are production tested at T_A = +70°C. Min/max limits at T_A = 0°C and T_A = +25°C are guaranteed by design and characterization.

Note 2: Gain-control range specifications met over this band.

Note 3: In-band IIP3 test conditions: GC1 set to provide the nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband (f_{LO} = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -26dBm each are applied at 2174MHz and 2175MHz. The IM3 tone at 3MHz is measured at baseband, but is referred to the RF input.

Note 4: Out-of-band IIP3 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband (f_{LO} = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -20dBm each are applied at 2070MHz and 1975MHz. The IM3 tone at 5MHz is measured at baseband, but is referred to the RF input.

Note 5: Input IP2 test conditions: GC1 set to provide nominal baseband output drive when mixing down a -23dBm tone at 2175MHz to 5MHz baseband (f_{LO} = 2170MHz). Baseband gain is set to its default value (BBG[3:0] = 1011). Two tones at -20dBm each are applied at 925MHz and 1250MHz. The IM2 tone at 5MHz is measured at baseband, but is referred to the RF input.

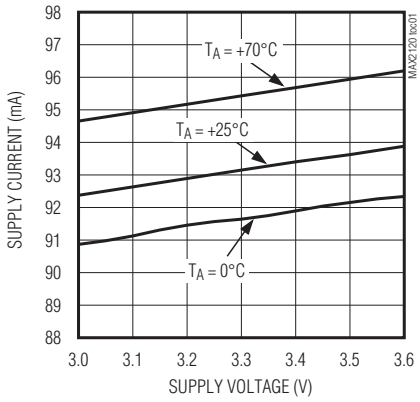
Note 6: Adjacent channel protection test conditions: GC1 is set to provide the nominal baseband output drive with a 2110MHz 27.5Mbaud signal at -55dBm. GC2 set for mid-scale. The test signal will be set for PR = 7/8 and SNR of -8.5dB. An adjacent channel at ±40MHz is added at -25dBm. DVB-S BER performance of 2E-4 will be maintained for the desired signal. GC2 may be adjusted for best performance.

Note 7: Guaranteed by design and characterization at T_A = +25°C.

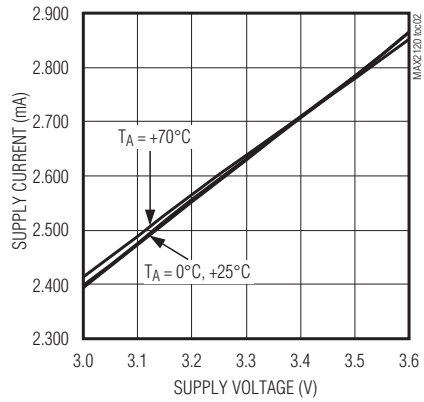
典型工作特性

(MAX2120 Evaluation Kit: V_{CC} = +3.3V, baseband output frequency = 5MHz; V_{GC1} = 1.2V; T_A = +25°C. Default register settings except ICP = 1 and BBG[3:0] = 1011.)

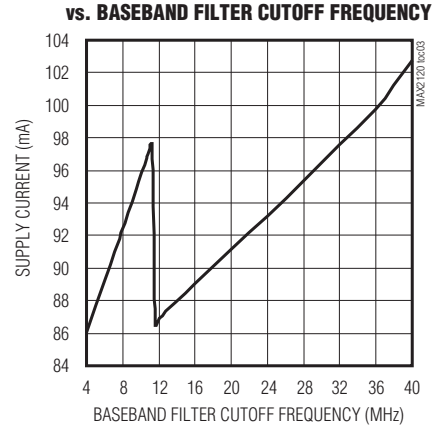
SUPPLY CURRENT vs. SUPPLY VOLTAGE



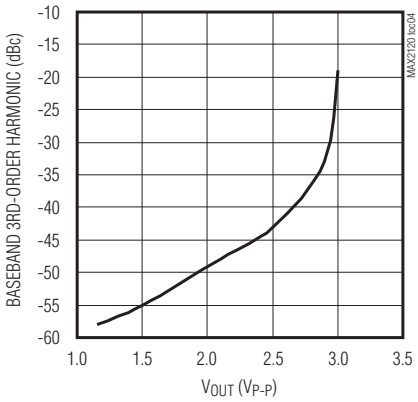
STANDBY MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



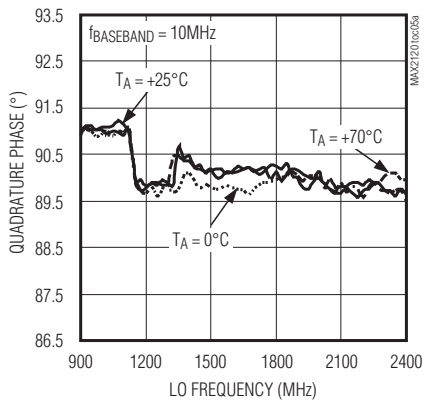
SUPPLY CURRENT vs. BASEBAND FILTER CUTOFF FREQUENCY



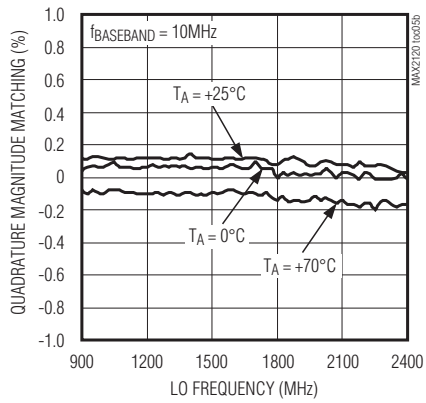
HD3 vs. OUTPUT VOLTAGE



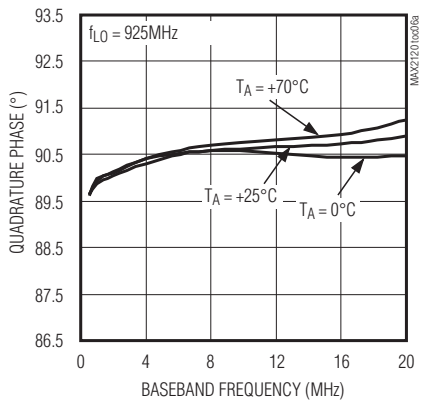
QUADRATURE PHASE vs. LO FREQUENCY



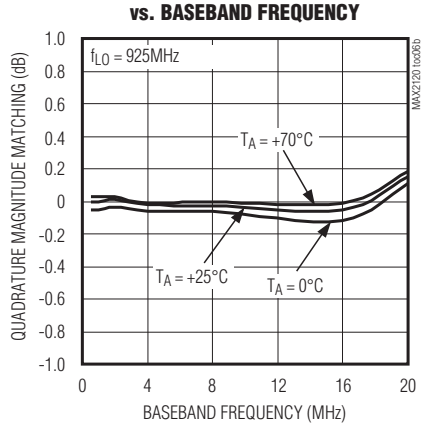
QUADRATURE MAGNITUDE MATCHING vs. LO FREQUENCY



QUADRATURE PHASE vs. BASEBAND FREQUENCY



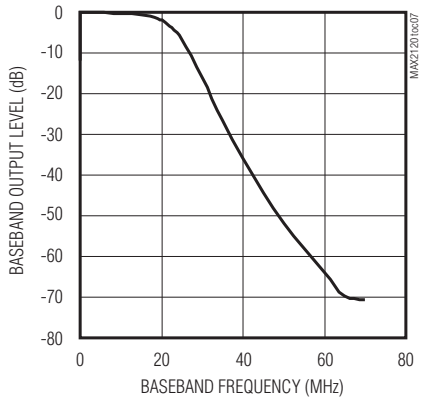
QUADRATURE MAGNITUDE MATCHING vs. BASEBAND FREQUENCY



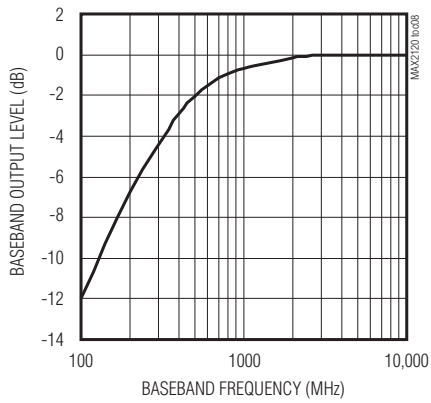
典型工作特性(续)

(MAX2120 Evaluation Kit: V_{CC} = +3.3V, baseband output frequency = 5MHz; V_{GC1} = 1.2V; T_A = +25°C. Default register settings except ICP = 1 and BBG[3:0] = 1011.)

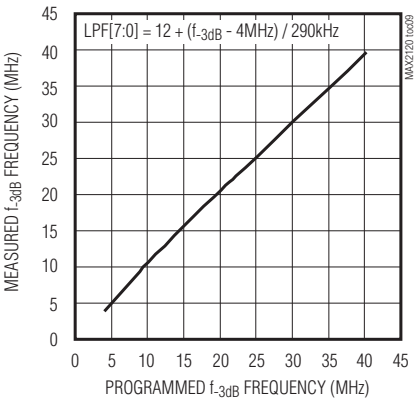
BASEBAND FILTER FREQUENCY RESPONSE



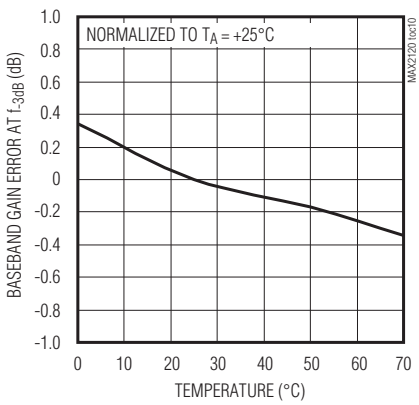
BASEBAND FILTER HIGHPASS FREQUENCY RESPONSE



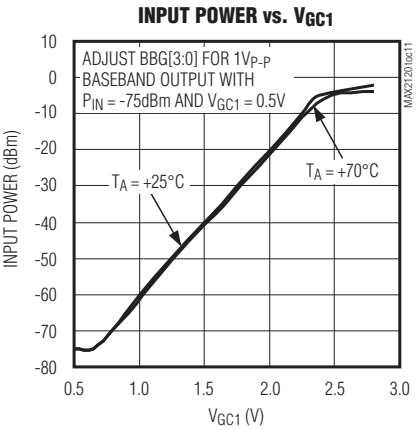
PROGRAMMED f_{-3dB} FREQUENCY vs. MEASURED f_{-3dB} FREQUENCY



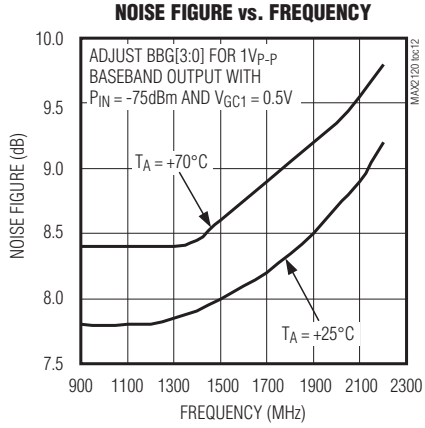
BASEBAND FILTER 3dB FREQUENCY vs. TEMPERATURE



INPUT POWER vs. V_{GC1}



NOISE FIGURE vs. FREQUENCY



典型工作特性(续)

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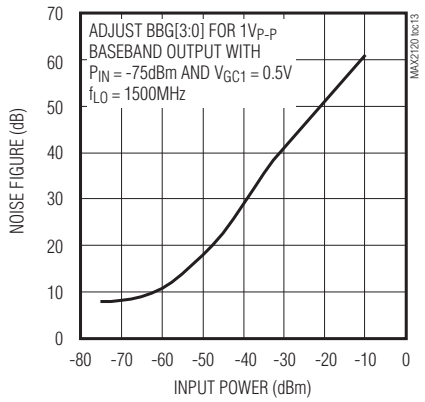
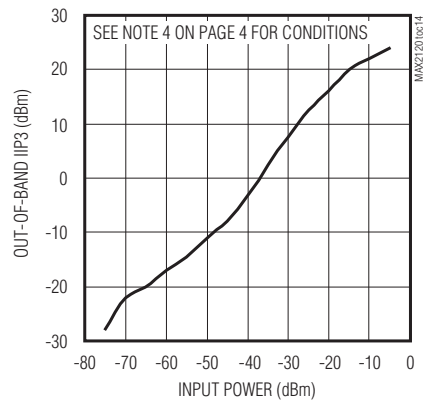
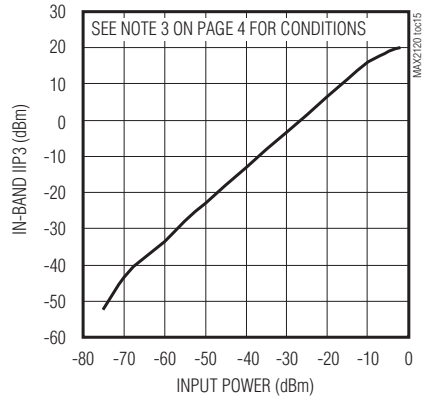
NOISE FIGURE vs. INPUT POWER



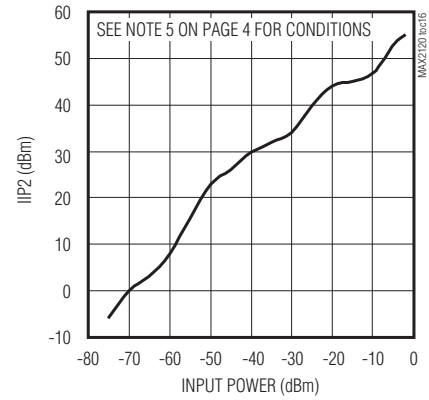
OUT-OF-BAND IIP3 vs. INPUT POWER



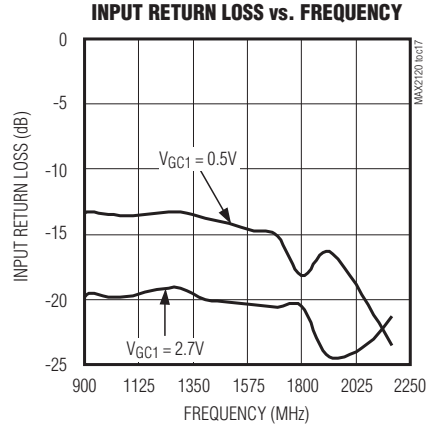
IN-BAND IIP3 vs. INPUT POWER



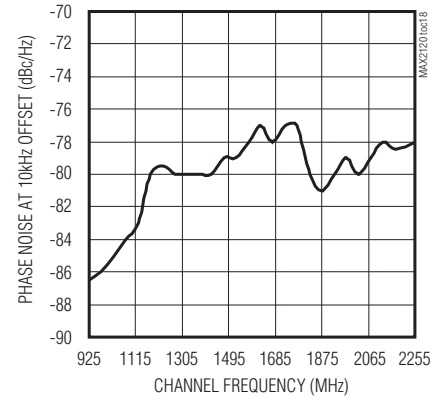
IIP2 vs. INPUT POWER



INPUT RETURN LOSS vs. FREQUENCY



PHASE NOISE AT 10kHz OFFSET vs. CHANNEL FREQUENCY



完备的直接变频调谐器，用于DVB-S和免费广播系统

典型工作特性(续)

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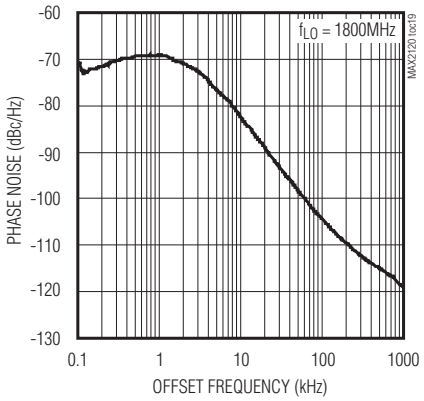
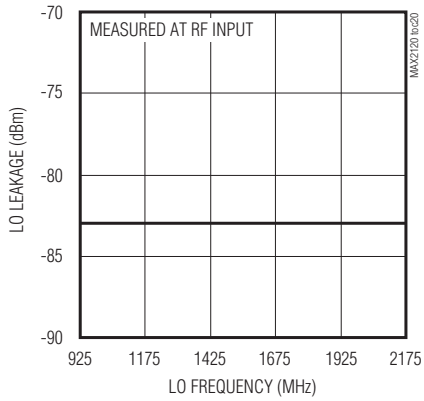
PHASE NOISE vs. OFFSET FREQUENCY



LO LEAKAGE vs. LO FREQUENCY



引脚说明

引脚	名称	说明
1	VCC_RF2	LNA的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
2	VCC_RF1	LNA的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
3	GND	地，连接到电路板的地层，以保证正常工作。
4	RFIN	宽带75Ω RF输入。通过一个隔直流电容连接RF信号源。
5	GC1	RF增益控制输入。高阻模拟输入，工作范围为0.5V至2.7V。V_{GC1} = 0.5V对应于最大增益设置。
6	VCC_LO	LO发生器的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
7	VCC_VCO	VCO电路的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
8	VCOBYP	内部VCO偏置旁路。通过100nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
9	VTUNE	高阻VCO调谐输入，该引脚直接连接到PLL环路滤波器输出，并使连线尽可能短。
10	GNDTUNE	VTUNE地，接PCB地层。
11	GNDSYN	频率合成器地，接PCB地层。
12	CPOUT	电荷泵输出，该输出接PLL环路滤波器输入，连线应尽可能短。

引脚说明(续)

引脚	名称	说明
13	VCC_SYN	频率合成器的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
14	XTAL	晶体振荡器连接端，采用一个外部并联谐振晶体串联一个1nF电容，请参考*典型工作电路*。
15	REFOUT	晶体振荡器缓冲输出，驱动外部电路时必须使用隔直流电容。
16	VCC_DIG	数字逻辑电路的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
17	QOUT+	正交基带差分输出，通过一个47nF电容交流耦合到解调器输入。
18	QOUT-	
19	IOUT+	同相基带差分输出，通过一个47nF电容交流耦合到解调器输入。
20	IOUT-	
21	IDC+	I通道基带直流失调校准，在IDC-和IDC+之间连接一个47nF陶瓷电容。
22	IDC-	
23	QDC+	Q通道基带直流失调校准，在QDC-和QDC+之间连接一个47nF陶瓷电容。
24	QDC-	
25	VCC_BB	基带电路的直流供电电源，连接到+3.3V低噪声电源。通过1nF电容旁路到地，电容应尽可能靠近引脚放置。不要与其它接地端共用电容接地过孔。
26	SDA	2线串行数据接口，需要通过2.7kΩ电阻上拉到V_{CC}。
27	SCL	2线串行时钟接口，需要通过2.7kΩ电阻上拉到V_{CC}。
28	ADDR	地址，ADDR没有连接时为逻辑高电平。
EP	EP	裸焊盘，均匀地焊接到电路板地层，以保证正常工作。

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详细说明

寄存器说明

MAX2120包括12个用户可配置的寄存器和2个只读寄存器。寄存器配置请参考表1，表1寄存器配置给出了所有寄存器位的名称和对应的使用信息。注意：所有寄存器必须在器件上电100µs之后才能进行写操作。

表1. 寄存器配置

REG NO	REGISTER NAME	READ/ WRITE	REG ADDRESS	MSB							LSB
				DATA BYTE							
				D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
1	N-Divider MSB	Write	0x00	X	N[14]	N[13]	N[12]	N[11]	N[10]	N[9]	N[8]
2	N-Divider LSB	Write	0x01	N[7]	N[6]	N[5]	N[4]	N[3]	N[2]	N[1]	N[0]
3	Charge Pump	Write	0x02	CPMP[1] 0	CPMP[0] 0	CPLIN[1] 0	CPLIN[0] 0	X	X	X	X
4	Not Used	Write	0x03	X	X	X	X	X	X	X	X
5	Not Used	Write	0x04	X	X	X	X	X	X	X	X
6	XTAL Divider/ R-Divider	Write	0x05	XD[2]	XD[1]	XD[0]	R[4]	R[3]	R[2]	R[1]	R[0]
7	PLL	Write	0x06	D24	CPS 0	ICP 1	X	X	X	X	X
8	VCO	Write	0x07	VCO[4]	VCO[3]	VCO[2]	VCO[1]	VCO[0]	VAS	ADL	ADE
9	LPF	Write	0x08	LP[7]	LP[6]	LP[5]	LP[4]	LP[3]	LP[2]	LP[1]	LP[0]
10	Control	Write	0x09	STBY	X	PWDN	X	BBG[3]	BBG[2]	BBG[1]	BBG[0]
11	Shutdown	Write	0x0A	X	PLL	DIV	VCO	BB	RFMIX	RFVG	FE
12	Test	Write	0x0B	CPTST[2] 0	CPTST[1] 0	CPTST[0] 0	X	TURBO 1	LD MUX[2] 0	LD MUX[1] 0	LD MUX[0] 0
13	Status Byte-1	Read	0x0C	POR	VASA	VASE	LD	X	X	X	X
14	Status Byte-2	Read	0x0D	VCOSBR[4]	VCOSBR[3]	VCOSBR[2]	VCOSBR[1]	VCOSBR[0]	ADC[2]	ADC[1]	ADC[0]

0 = 设置为“0”用于工厂测试。
1 = 设置为“1”用于工厂测试。
X = 无关。

表2. N分频器MSB寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7	X	Don’t care.
N[14:8]	6–0	0000011	Sets the most significant bits of the PLL integer-divide number (N). Default value is N = 950 decimal. N can range from 16 to 2175.

表3. N分频器LSB寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
N[7:0]	7–0	10110110	Sets the least significant bits of the PLL integer-divide number (N). Default value is N = 950 decimal. N can range from 16 to 2175.

表4. 电荷泵寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
CPMP[1:0]	7, 6	00	Charge-pump minimum pulse width. Users must program to 00 upon powering up the device.
CPLIN[1:0]	5, 4	00	Controls charge-pump linearity. 00 = Typically balanced charge and sink currents. Other values are not tested.
X	3–0	X	Don't care.

表5. XTAL缓冲器和参考时钟分频寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
XD[2:0]	7, 6, 5	000	Sets the crystal-divider setting. 000 = Divide by 1 (default) 001 = Divide by 2 011 = Divide by 3 100 = Divide by 4 101 through 110 = All divide values from 5 (101) to 7 (110) 111 = Divide by 8
R[4:0]	4–0	00100	Sets the PLL reference-divider (R) number. 00001 = Divide by 1 00010 = Divide by 2 00011 = Divide by 3 00100 = Divide by 4 (default) 00101 through 11110 = All divide values from 3 (00101) to 29 (11110) 11111 = Divide by 31

表6. PLL寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
D24	7	1	VCO divider setting. 0 = Divide by 2 1 = Divide by 4 (default)
CPS	6	1	Charge-pump current mode. Users must program to 0 upon powering up the device. 0 = Charge-pump current controlled by ICP bit 1 = Charge-pump current controlled by VCO autoselect (VAS)
ICP	5	0	Charge-pump current. 0 = 600µA typical 1 = 1200µA typical
X	4–0	X	Don't care.

表7. VCO寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
VCO[4:0]	7–3	11001	Controls which VCO is activated when using manual VCO programming mode. This also serves as the starting point for the VCO autoselect mode.
VAS	2	1	VCO Autoselection (VAS) Circuit 0 = Disable VCO selection must be program through I^2C 1 = Enable VCO selection controlled by autoselection circuit
ADL	1	0	Enables or disables the VCO tuning voltage ADC latch when the VCO autoselect mode (VAS) is disabled. 0 = Disables the ADC latch 1 = Latches the ADC value
ADE	0	0	Enables or disables VCO tuning voltage ADC read when the VCO autoselect mode (VAS) is disabled. 0 = Disables ADC read 1 = Enables ADC read

表8. 低通滤波器寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
LPF[7:0]	7–0	01001011	Sets the baseband lowpass filter 3dB corner frequency. 3dB corner frequency = 4MHz + (LPF[7:0] - 12) x 290kHz.

表9. 控制寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
STBY	7	0	Software standby control. 0 = Normal operation 1 = Disables the signal path and frequency synthesizer, leaving only the 2-wire bus, crystal oscillator, XTALOUT buffer, and XTALOUT buffer divider active
X	6	X	Don't care.
PWDN	5	0	Software power-down control. 0 = Normal operation 1 = Shuts down the entire chip, but leaves the 2-wire bus active and maintains the current register states
X	4	X	Don't care.
BBG[3:0]	3–0	0000	Baseband gain setting (1dB typical per step). 0000 = Minimum gain (0dB) … 1111 = Maximum gain (15dB typical)

表10. 关断寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
X	7	X	Don't care.
PLL	6	0	PLL enable. 0 = Normal operation 1 = Shuts down the PLL
DIV	5	0	Divider enable. 0 = Normal operation 1 = Shuts down the divider
VCO	4	0	VCO enable. 0 = Normal operation 1 = Shuts down the VCO
BB	3	0	Baseband enable. 0 = Normal operation 1 = Shuts down the baseband
RFMIX	2	0	RF mixer enable. 0 = Normal operation 1 = Shuts down the RF mixer
RFVGA	1	0	RF VGA enable. 0 = Normal operation 1 = Shuts down the RF VGA
FE	0	0	RF front-end enable. 0 = Normal operation 1 = Shuts down the RF front-end

表11. 测试寄存器

BIT NAME	BIT LOCATION (0 = LSB)	DEFAULT	FUNCTION
CPTST[2:0]	7, 6, 5	000	Charge-pump test modes. 000 = Normal operation (default) 001 = Crystal translator ECL to CMOS path 100 = Both source and sink currents enabled 101 = Source current enabled 110 = Sink current enabled 111 = High impedance (both source and sink current disabled)
X	4	X	Don't care.
TURBO	3	0	Charge-pump fast lock. Users must program to 1 upon powering up the device. 0 = Turbo mode off, used for CP test modes (default) 1 = Turbo mode on, used for LD function
LDMUX[2:0]	2, 1, 0	000	REFOUT output. 000 = Normal operation; other values are not tested

表12. 状态字节-1寄存器

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
POR	7	Power-on reset status. 0 = Chip status register has been read with a stop condition since last power-on 1 = Power-on reset (power cycle) has occurred, default values have been loaded in registers
VASA	6	Indicates whether VCO autoselection was successful. 0 = Indicates the autoselect function is disabled or unsuccessful VCO selection 1 = Indicates successful VCO autoselection
VASE	5	Status indicator for the autoselect function. 0 = Indicates the autoselect function is active 1 = Indicates the autoselect process is inactive
LD	4	PLL lock detector. 0 = Unlocked 1 = Locked
X	3–0	Don’t care.

表13. 状态字节-2寄存器

BIT NAME	BIT LOCATION (0 = LSB)	FUNCTION
VCOSBR[4:0]	7–3	VCO band readback.
ADC[2:0]	2, 1, 0	VAS ADC output readback. 000 = Out of lock 001 = Locked 010 = VAS locked 101 = VAS locked 110 = Locked 111 = Out of lock

2线串行接口

MAX2120采用2线I²C兼容串行接口，由串行数据线(SDA)和串行时钟线(SCL)组成。SDA和SCL简化了MAX2120和主控制器之间的双向通信，时钟频率可达400kHz。总线数据传输由主控制器启动，主控制器产生SCL信号进行数据传输。MAX2120为从器件，能够发送数据到主控制器并接收来自主控制器的数据。为了适应总线操作，SDA、SCL必须通过外部上拉电阻(1kΩ或更大)拉至高电平。

每个SCL时钟周期传输1位数据，MAX2120输入或输出1个字节的数据至少需要9个时钟周期(8位数据和1位ACK/NACK)。SCL时钟为高电平时，SDA数据必须保持稳定。当SCL固定为高电平时，SDA的变化将产生控制信号(请参考*START和STOP条件*部分)。总线空闲时，SDA、SCL都会保持高电平。

START和STOP条件

主控制器利用START条件(S)启动传输，SCL为高电平时，SDA从高电平跳变为低电平即产生START条件。主控制器在STOP条件(P)下终止传输，SCL为高电平时，SDA从低电平跳变到高电平即产生STOP条件。

应答和非应答条件

数据传输帧格式中带有一个应答位(ACK)或非应答位(NACK)。主控制器和MAX2120 (从器件)都会产生应答位，为了产生应答信号，接收器件必须在对应时钟(第九个脉冲)的上升沿之前将SDA拉低，并使其在时钟为高电平期间保持稳定的低电平。

为了产生非应答信号，接收机在对应的应答脉冲上升沿之前将SDA拉高，并且在时钟的高电平期间保持SDA为稳定的高电平。监测应答位可以检测到失败的数据传输。在接收器件忙或系统发生故障时，数据传输可能失效。数据传输失败后，总线主控制器必须在稍后重新尝试通信。

从地址

MAX2120有一个7位从地址，START条件启动通信后发送该地址，从地址由内部设置为1100000，7位地址之后的第8位(R/$\overline{W}$)决定读操作或写操作。

MAX2120连续等待START条件，从地址紧随START条件发送。当器件识别到其从地址后，将SDA拉低一个时钟周期进行应答；然后根据R/$\overline{W}$位准备接收或发送数据(图1)。

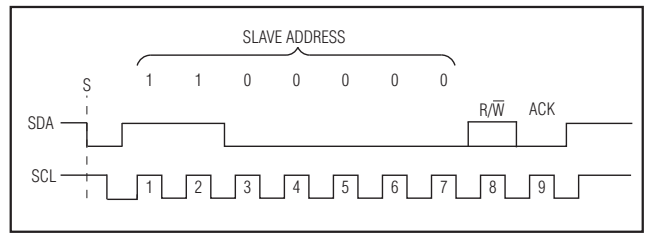

图1. MAX2120从地址字节

写周期

接收到写命令之后，MAX2120允许主控制器写一个寄存器或多个连续的寄存器。

写周期开始于总线主控制器发出的START条件和随后的7位从地址、1位写操作控制(R/$\overline{W}$ = 0)。MAX2120在成功接收从地址字节后发出ACK。然后，总线主控制器必须将其进行写操作的第一个寄存器地址发送到从器件(参考表1列出的寄存器地址)。如果从器件应答了该地址，那么主控制器将一个字节写入该指定地址的寄存器。数据从最高有效位开始写入。如果数据成功写入寄存器，MAX2120会再次发出ACK。主控制器可以在MAX2120应答每次成功传输后，连续将数据写入连续的内部寄存器，也可以产生STOP条件终止传输。在主控制器产生STOP条件后，写周期终止。

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图2所示分别将0x0E、0xD8和0xE1写入寄存器0-2。

读周期

主控制器只能读取MAX2120的两个寄存器，MAX2120接收到读命令后会将这两个寄存器(状态字节-1和状态字节-2)的内容发送到主控制器。

读周期开始于总线主控制器发出的START条件和7位从地址、1位读操作控制(R/$\overline{W}$ = 1)。MAX2120在成功接收从地址字节后发出ACK。然后主控制器从最高有效位开始读取状态字节-1寄存器的内容，并在成功接收后发出应答。随后，主控制器读取状态字节-2寄存器的内容。这时，主控制器可以产生ACK、NACK或STOP条件来终止读周期。

图3所示是主控制器读取寄存器的例子。

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	WRITE REGISTER ADDRESS	ACK	WRITE DATA TO REGISTER 0x00	ACK	WRITE DATA TO REGISTER 0x01	ACK	WRITE DATA TO REGISTER 0x02	ACK	STOP
	1100000	0	—	0x00	—	0x0E	—	0xD8	—	0x0E1	—	

图2. 例：分别将0x0E、0xD8和0xE1写入寄存器0-2

START	WRITE DEVICE ADDRESS	R/$\overline{W}$	ACK	READ FROM STATUS BYTE-1 REGISTER	ACK	READ FROM STATUS BYTE-2 REGISTER	ACK/ NACK	STOP
	1100000	1	—	—	—	—	—	

图3. 例：从寄存器读取数据

应用信息

MAX2120把925MHz至2175MHz范围的RF信号直接下变频到基带I/Q信号，该器件适用于数字DBS调谐器应用。

RF输入

MAX2120的RF输入由内部匹配到75Ω，只需要一个隔直流电容，请参考*典型工作电路*。

RF增益控制

MAX2120具有一个可变增益低噪声放大器，可以提供73dB的RF增益范围。电压控制(VGC)范围为0.5V (最小衰减)到2.7V (最大衰减)。

基带可变增益放大器

可变增益基带接收放大器提供15dB的可编程增益范围，步长1dB。VGA增益可通过SPI™接口设置控制寄存器的BBG[3:0]进行配置。

基带低通滤波器

MAX2120包含一个可编程7阶巴特沃斯滤波器，该基带滤波器的-3dB角频率可通过设置低通寄存器的LPF[7:0]进行配置，LPF[7:0]的数值由下式决定：

$$LPF[7:0]dec = \frac{(f_{-3dB} - 4MHz)}{0.29MHz} + 12,$$

其中f_{-3dB}的单位为MHz。

该滤波器角频率可以在4MHz到40MHz范围调节，器件总电源电流取决于滤波器的带宽设置，电流会随着-3dB带宽的增大而增加。

消除直流失调

为了保证I/Q输出的动态范围，需要消除直流失调。在IDC+和IDC-之间连接一个外部电容，构成I通道高通滤波器，在QDC+和QDC-之间连接一个电容构成Q通道高通滤波器。保持外部电容值小于47nF，组成一个角频率为400Hz左右的高通滤波器。

XTAL振荡器

MAX2120内置参考时钟振荡器、参考时钟输出分频器和输出缓冲器。用1nF电容与晶体串联，选择ESR小于150Ω的4MHz晶体，典型输入电容为40pF。如果不使用4MHz晶体，请联系工厂了解更多信息。

VCO自动选择(VAS)

MAX2120包括24个VCO，本振频率通过配置VCO寄存器的VCO[4:0]位选择。所选VCO记录在状态字节-2寄存器(见表13)。

MAX2120还可以将VCO寄存器的VAS置为逻辑高电平来自动选择VCO，一旦装载N分频LSB寄存器(REG2)，即可启动VAS程序。

如果只改变R分频寄存器或N分频MSB寄存器，N分频LSB寄存器必须最后写入，以启动VCO自动选择功能。VCO[4:0]寄存器中写入的VCO数值作为VCO自动选择的起点。

选择过程中，状态字节-1寄存器的VASE位清0，表明自动选择功能已经生效。成功操作后，VASE和VASA置位，所选择的VCO记录到状态字节-2寄存器(见表13)。如果搜索失败，VASA清0，VASE置位。表明搜索已经结束但没有找到合适的VCO，这种情况发生在试图调谐到VCO指定频率范围以外的情况下。

更多信息请参考MAX2112/MAX2120 VAS应用笔记。

SPI是Motorola, Inc.的商标。

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3位ADC

MAX2120有一个内部3位ADC连接到VCO调谐引脚(VTUNE)。这个ADC用于检查VCO的锁定状态。

表14概括了ADC的数值和VCO锁定指示。VCO自动选择程序在“VAS锁定”范围内只选择一个VCO，使VCO可以在一定温漂条件下保持有效的“锁定”范围。

ADC必须首先通过置位VCO寄存器的ADE位使能。通过对ADC锁存位编程(ADL = 1)锁存ADC读数，ADC数值会记录在状态字节-2寄存器(见表13)。

表14. ADC数值和锁定状态

ADC[2:0]	LOCK STATUS
000	Out of Lock
001	Locked
010	VAS Locked
101	VAS Locked
110	Locked
111	Out of Lock

掉电和待机模式

MAX2120可通过I^2C接口设置标准工作模式、掉电模式和待机模式。将控制寄存器的PWDN位置为逻辑高电平时，使能掉电模式。这种模式下，除了2线接口，所有电路都被关断，但依然能够配置MAX2120寄存器。

将控制寄存器的STBY位置为逻辑高电平，器件进入待机模式。这种模式下只有2线接口、晶体振荡器、XTAL缓冲器和XTAL缓冲分频器处于工作状态。

任何情况下，器件在进入掉电模式之前都需要保存寄存器配置，以便在器件切换到正常工作模式时恢复工作。默认的寄存器值仅仅为方便用户使用，用户在器件上电100µs后才可以配置寄存器，表15总结了不同的掉电模式。

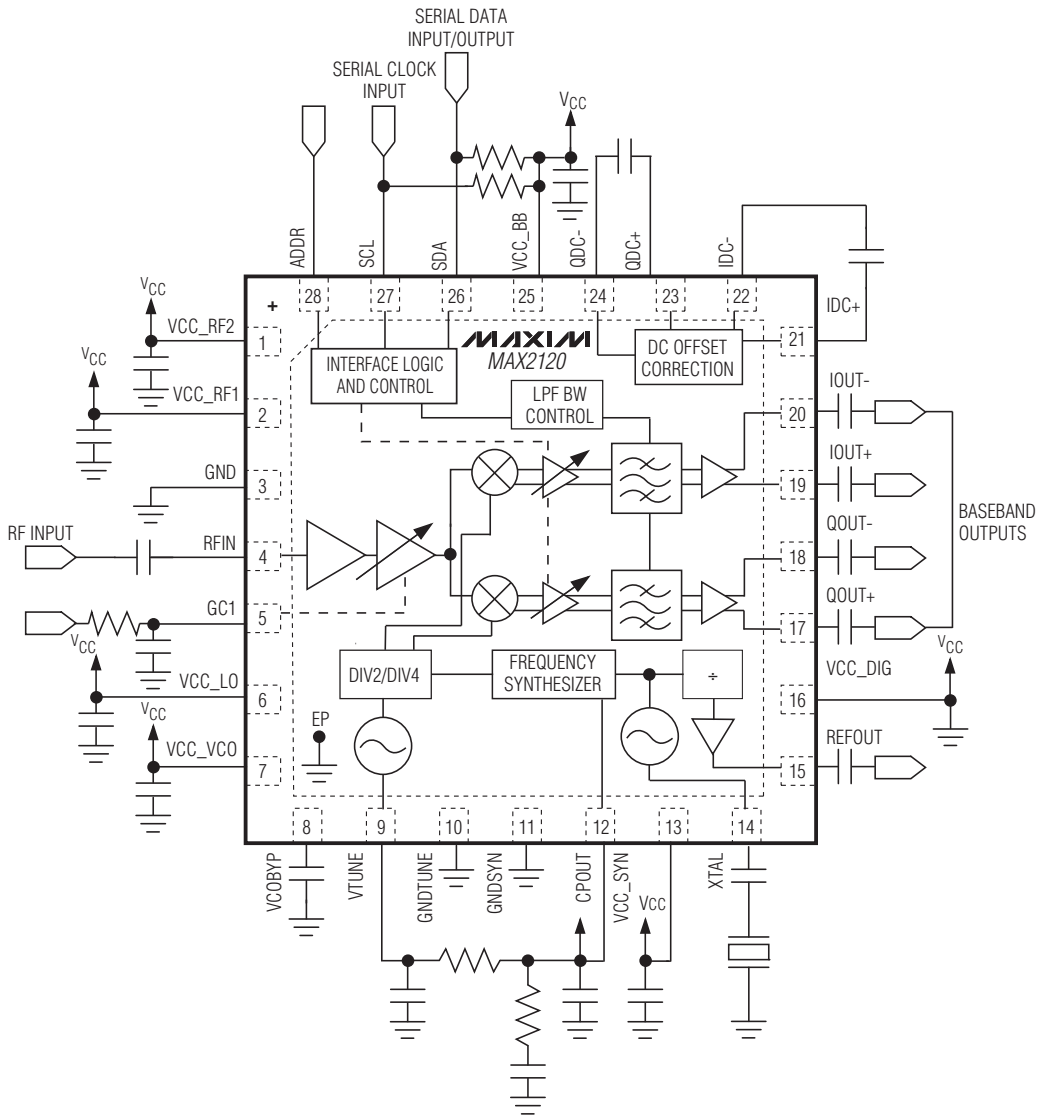
布板考虑

PCB布局可参考MAX2120评估板，RF信号线要尽可能短，以减小损耗和辐射。所有高频引线使用阻抗受控的传输线，为了保证正常工作，裸焊盘必须均匀地焊接到电路板的地层。在裸焊盘下使用多个过孔，以达到最佳散热效果。在RF引线之间采用多个接地过孔，降低信号耦合。每个V_{CC}引脚都需要在尽可能靠近引脚的位置放置一个1nF的旁路电容。

表15. 掉电模式

MODE	POWER-DOWN CONTROL		CIRCUIT STATES			DESCRIPTION
	PWDN BIT	STBY BIT	SIGNAL PATH	2-WIRE INTERFACE	XTAL	
Normal	0	0	On	On	On	All circuits active.
Power-Down	1	0	Off	On	Off	2-wire interface is active.
Standby	0	1	Off	On	On	2-wire interface, XTAL, and XTAL buffer/divider are active.

典型工作电路



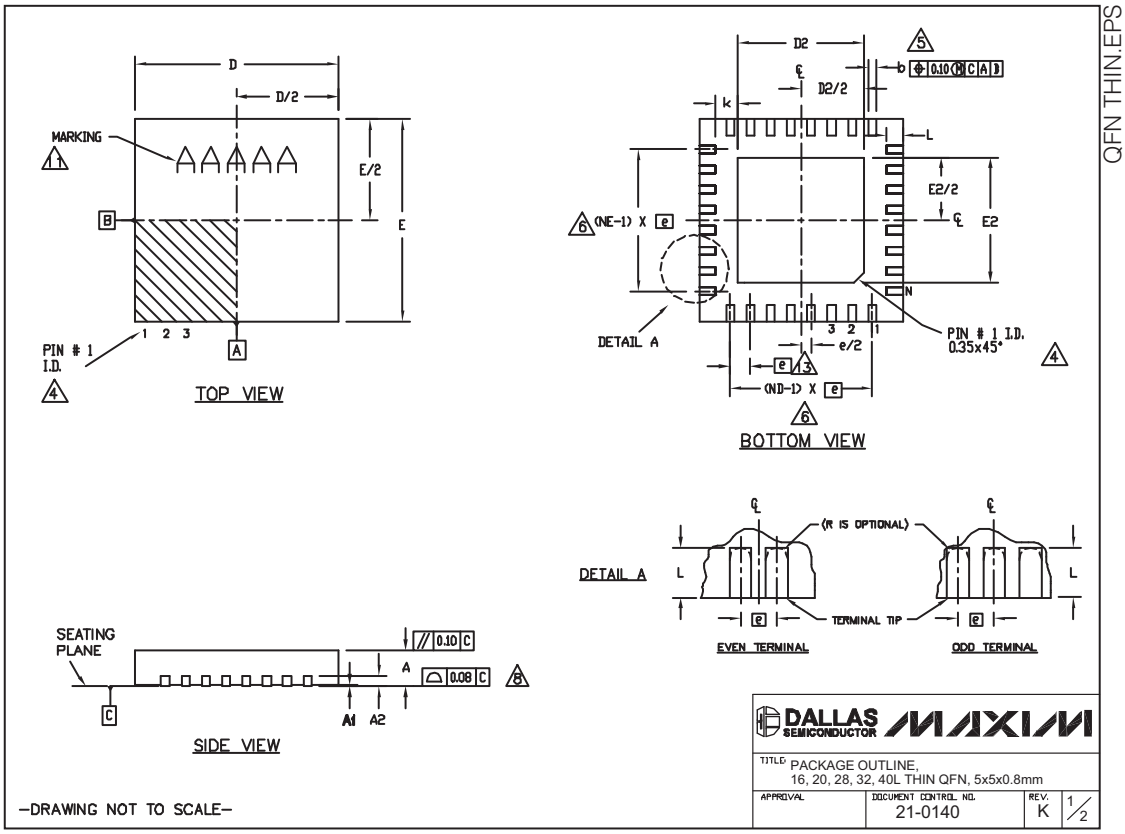
芯片信息

PROCESS: BiCMOS

完备的直接变频调谐器，用于DVB-S和免费广播系统

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)



封装信息(续)

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 **www.maxim-ic.com.cn/packages**。)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055M-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	K	2/2

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