



DisplayPort/PCIE 无源开关

MAX4928A/MAX4928B

概述

MAX4928A/MAX4928B 高速无源开关可在台式机或笔记本电脑的两个接收端之间切换 PCI Express® (PCIe) 数据和/或 DisplayPort™ 信号。MAX4928A 设计用于台式机的 ATX 主板、MAX4928B 设计用于 BTX 主板。

MAX4928A/MAX4928B 是六路双刀/双掷 (6 x DPDT) 开关。MAX4928A/MAX4928B 具有一个数字控制输入 (SEL)，用于切换信号路径；还提供一个锁存输入 (LE)，用于将开关保持在指定状态。

MAX4928A/MAX4928B 采用 +3.3V (典型值) 单电源供电；MAX4928A/MAX4928B 提供工业标准 5mm x 11mm、56 引脚 TQFN 封装；这两款器件均工作在 -40°C 至 +85°C 扩展级温度范围。

应用

- 台式 PC
- 笔记本 PC

PCI Express 是 PCI-SIG 的注册商标。

DisplayPort 是 Video Electronics Standards Association (VESA) 的商标。

特性

- ◆ +3.3V 单电源供电
- ◆ 支持 PCIe Gen I、Gen II 以及 DisplayPort 数据速率高于 5Gbps
- ◆ 优异的回波损耗指标：2.5GHz 时大于 12dB
- ◆ 集成六路双向开关对在单芯片中实现所有切换
- ◆ 低电源电流：800µA (最大值)
- ◆ 小尺寸 5mm x 11mm、56 引脚 TQFN 封装
- ◆ 引脚排列兼容于工业标准产品

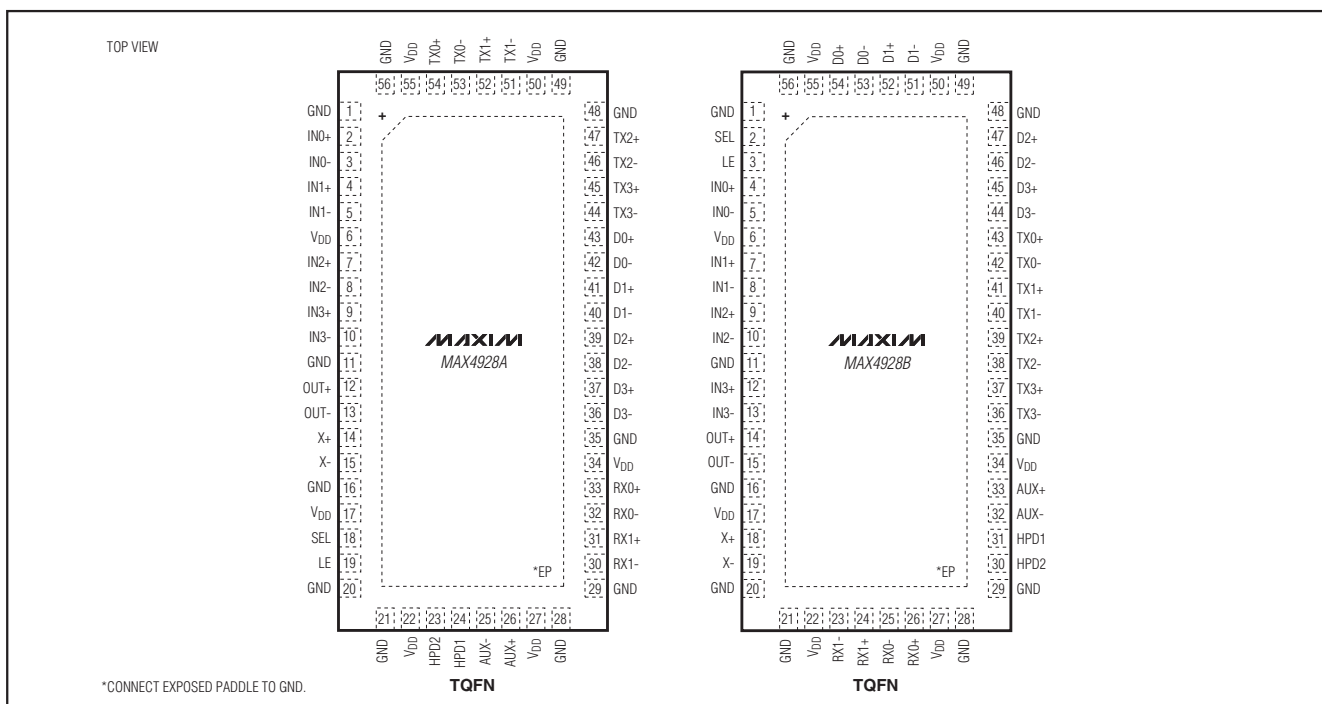
订购信息

PART	PIN-PACKAGE	PKG CODE
MAX4928AETN+	56 TQFN-EP	T56511-1
MAX4928BETN+	56 TQFN-EP	T56511-1

注：所有器件工作在 -40°C 至 +85°C 温度范围。
+ 表示无铅封装。
EP = 裸焊盘。

典型工作电路在数据资料的最后给出。

引脚配置



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V _{DD}	-0.3V to +4V
LE, SEL, IN ₋ , X ₋ , OUT ₋ , D ₋ , TX ₋ , HPD ₋ , RX ₋ , AUX ₋ (Note 1).....	-0.3V to + (V _{DD} + 0.3V)
IV _{IN₋} - V _{TX₋} I, IV _{IN₋} - V _{D₋} I, IV _{X₋} - V _{HPD₋} I, IV _{X₋} - V _{RX1₋} I, IV _{OUT₋} - V _{AUX₋} I, IV _{OUT₋} - V _{RX0₋} I (Note 1).....	0 to +2V
Continuous Current (IN ₋ to D ₋ /TX ₋ , X ₋ to HPD ₋ /RX1 ₋ , OUT ₋ to AUX ₋ /RX0 ₋).....	±70mA
Peak Current (IN ₋ to D ₋ /TX ₋ , X ₋ to HPD ₋ /RX1 ₋ , OUT ₋ to AUX ₋ /RX0 ₋) (pulsed at 1ms, 10% duty cycle).....	±70mA
Continuous Current (LE, SEL).....	±30mA

Peak Current (LE, SEL)

(pulsed at 1ms, 10% duty cycle).....	±70mA
Continuous Power Dissipation (T _A = +70°C) for Multilayer Board 56-Pin TQFN (derate 41.0mW/°C above +70°C).....	3279mW
Operating Temperature Range.....	-40°C to +85°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Package Junction-to-Ambient Thermal Resistance (θ _{JA}) (Note 2).....	24.4°C/W
Package Junction-to-Case Thermal Resistance (θ _{JC}) (Note 2).....	1.5°C/W
Lead Temperature (soldering).....	+300°C

Note 1: Signals on IN₋, X₋, OUT₋, D₋, TX₋, HPD₋, RX₋, or AUX₋, LE, SEL exceeding V_{DD} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, see www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG SWITCH						
Analog Signal Range	IN ₋ , X ₋ , OUT ₋ , D ₋ , TX ₋ , HPD ₋ , RX ₋ , AUX ₋		-0.1		(V _{DD} - 1.8)	V
Voltage Between IN and D/TX, X and HPD/RX1, and OUT and AUX/RX0	IV _{IN₋} - V _{TX₋} I, IV _{IN₋} - V _{D₋} I, IV _{X₋} - V _{HPD₋} I, IV _{X₋} - V _{RX1₋} I, IV _{OUT₋} - V _{AUX₋} I, IV _{OUT₋} - V _{RX0₋} I		0		1.8	V
On-Resistance	R _{ON}	I _{IN₋} = I _{X₋} = I _{OUT₋} = 15mA, V _{D₋} , V _{TX₋} , V _{HPD₋} , V _{AUX₋} , or V _{RX₋} = 0V, +1.2V		8		Ω
On-Resistance Match Between Pairs of Same Channel	ΔR _{ON}	V _{DD} = +3.0V, I _{IN₋} = I _{X₋} = I _{OUT₋} = 15mA, V _{D₋} , V _{TX₋} , V _{HPD₋} , V _{AUX₋} , or V _{RX₋} = 0V (Notes 4, 5)		0.1	1	Ω
On-Resistance Match Between Channels	ΔR _{ON}	V _{DD} = +3.0V, I _{IN₋} = I _{X₋} = I _{OUT₋} = 15mA, V _{D₋} , V _{TX₋} , V _{HPD₋} , V _{AUX₋} , or V _{RX₋} = 0V (Notes 4, 5)		1.5	4	
On-Resistance Flatness	R _{FLAT(ON)}	V _{DD} = +3.0V, I _{IN₋} = I _{X₋} = I _{OUT₋} = 15mA, V _{D₋} , V _{TX₋} , V _{HPD₋} , V _{AUX₋} , or V _{RX₋} = 0V, +1.2V (Notes 5, 6)		3	1.5	Ω

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D ₋ or TX ₋ / HPD ₋ or RX1 ₋ / AUX ₋ or RX0 ₋ Off-Leakage Current	I _{D-} (OFF) I _{TX-} (OFF) I _{HPD-} (OFF) I _{RX1-} (OFF) I _{AUX-} (OFF) I _{RX0-} (OFF)	V _{DD} = +3.6V, V _{IN-} = V _{X-} = V _{OUT-} = 0V, +1.2V; V _{D-} or V _{TX-} , V _{HPD-} or V _{RX1-} , V _{AUX-} or V _{RX0-} = +1.2V, 0V	-1		+1	μA
IN ₋ /X ₋ /OUT ₋ On-Leakage Current	I _{IN-} (ON) I _{X-} (ON) I _{OUT-} (ON)	V _{DD} = +3.6V, V _{IN-} = V _{X-} = V _{OUT-} = 0V, +1.2V; V _{D-} or V _{TX-} = V _{IN-} or unconnected, V _{HPD-} or V _{RX1-} = V _{X-} or unconnected, V _{AUX-} or V _{RX0-} = V _{OUT-} or unconnected	-1		+1	
DIGITAL SIGNALS						
SEL to Switch Turn-On Time	t _{ON_SEL}	V _{D-} or V _{TX-} = +1.0V, R _L = 50Ω, V _{HPD-} or V _{RX1-} = +1.0V, R _L = 50Ω, V _{AUX-} or V _{RX0-} = +1.0V, R _L = 50Ω, LE = V _{DD} , C _L = 100pf (Figure 1)		55	120	ns
SEL to Switch Turn-Off Time	t _{OFF_SEL}	V _{D-} or V _{TX-} = +1.0V, R _L = 50Ω, V _{HPD-} or V _{RX1-} = +1.0V, R _L = 50Ω, V _{AUX-} or V _{RX0-} = +1.0V, R _L = 50Ω, LE = V _{DD} , C _L = 100pf (Figure 1)		8	50	ns
LE Setup Time SEL to LE	t _{SU}	V _{D-} or V _{TX-} = +1.0V, R _L = 50Ω, V _{HPD-} or V _{RX1-} = +1.0V, R _L = 50Ω, V _{AUX-} or V _{RX0-} = +1.0V, R _L = 50Ω (Figure 1)		2		ns
LE Hold Time SEL to LE	t _{HOLD}	V _{D-} or V _{TX-} = +1.0V, R _L = 50Ω, V _{HPD-} or V _{RX1-} = +1.0V, R _L = 50Ω, V _{AUX-} or V _{RX0-} = +1.0V, R _L = 50Ω, (Figure 1)		2		ns
LE Minimum Pulse-Width Low	t _w	V _{D-} or V _{TX-} = +1.0V, R _L = 50Ω, V _{HPD-} or V _{RX1-} = +1.0V, R _L = 50Ω, V _{AUX-} or V _{RX0-} = +1.0V, R _L = 50Ω (Figure 1)	40			ns
Differential Insertion Loss (Figure 2)	S _{DD21}	f = 2.5GHz		-1.5		dB
		f = 5.0GHz		-3.3		
		f = 7.5GHz		-4.9		
Differential Crosstalk (Figure 2)	S _{DDCTK}	f = 2.5GHz		-40		dB
		f = 5.0GHz		-23		
		f = 7.5GHz		-28		
Differential Off-Isolation	S _{DD21_OFF}	f = 3.0GHz		-22		dB
Differential Return Loss (Figure 2)	S _{DD11}	f = 2.8GHz		-21		dB
		f = 5.0GHz		-8		
		f = 7.5GHz		-7		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal Data Rate	BR	R _S = R _L = 100Ω balanced		10		Gbps
Differential -3dB Bandwidth	DBW	R _S = R _L = 100Ω balanced		5		GHz
LOGIC INPUT (LE, SEL)						
Input Logic-High	V _{IH}		1.4			V
Input Logic-Low	V _{IL}				0.5	V
Input Logic Hysteresis	V _{HYST}			100		mV
Input Leakage Current	I _{IN}	V _{IN} = 0 or V _{DD}	-1		+1	μA
POWER SUPPLY						
Power Supply Range	V _{DD}		3.0		3.6	V
V _{DD} Supply Current	I _{DD}	V _{IN} = 0 or V _{DD}			850	μA

Note 3: All units are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

Note 4: ΔR_{ON} = R_{ON} (MAX) - R_{ON} (MIN).

Note 5: Guaranteed by design. Not production tested.

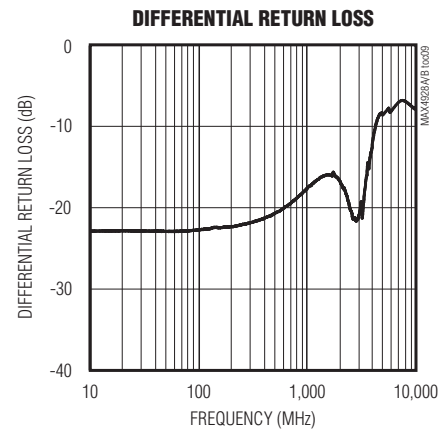
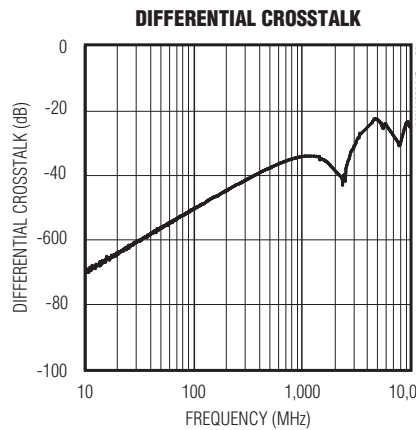
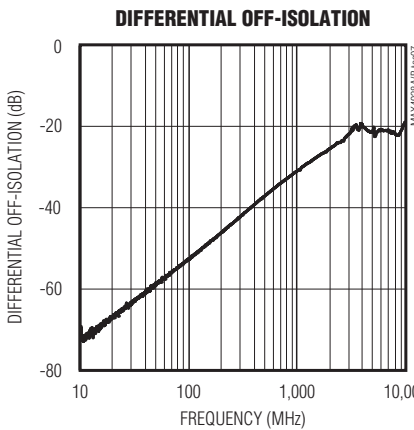
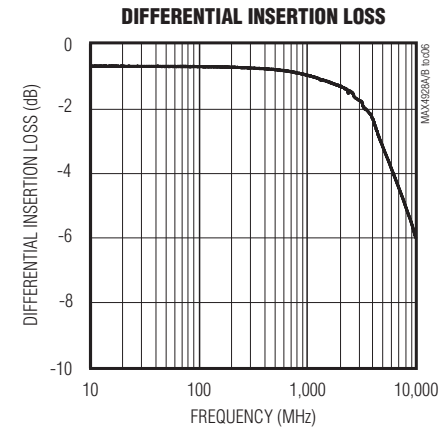
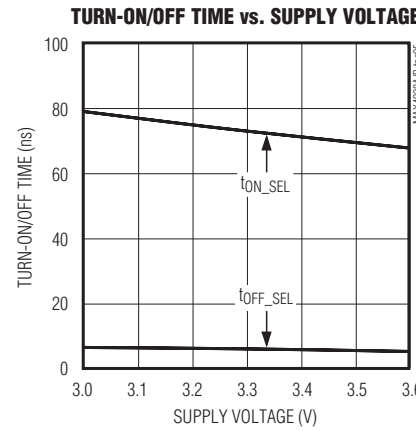
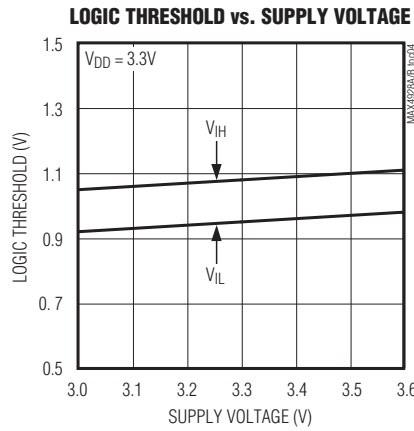
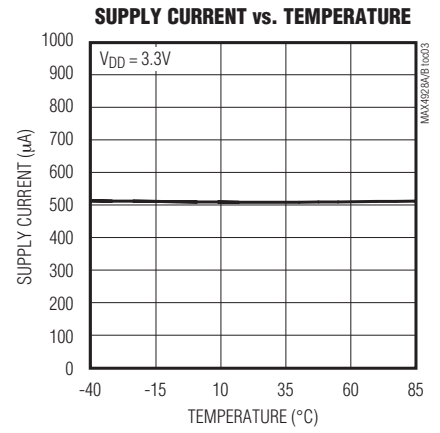
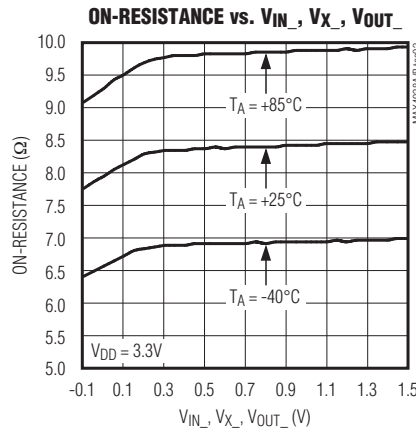
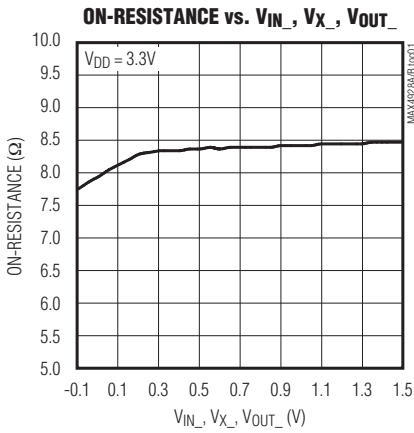
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

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典型工作特性

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

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测试电路/时序图

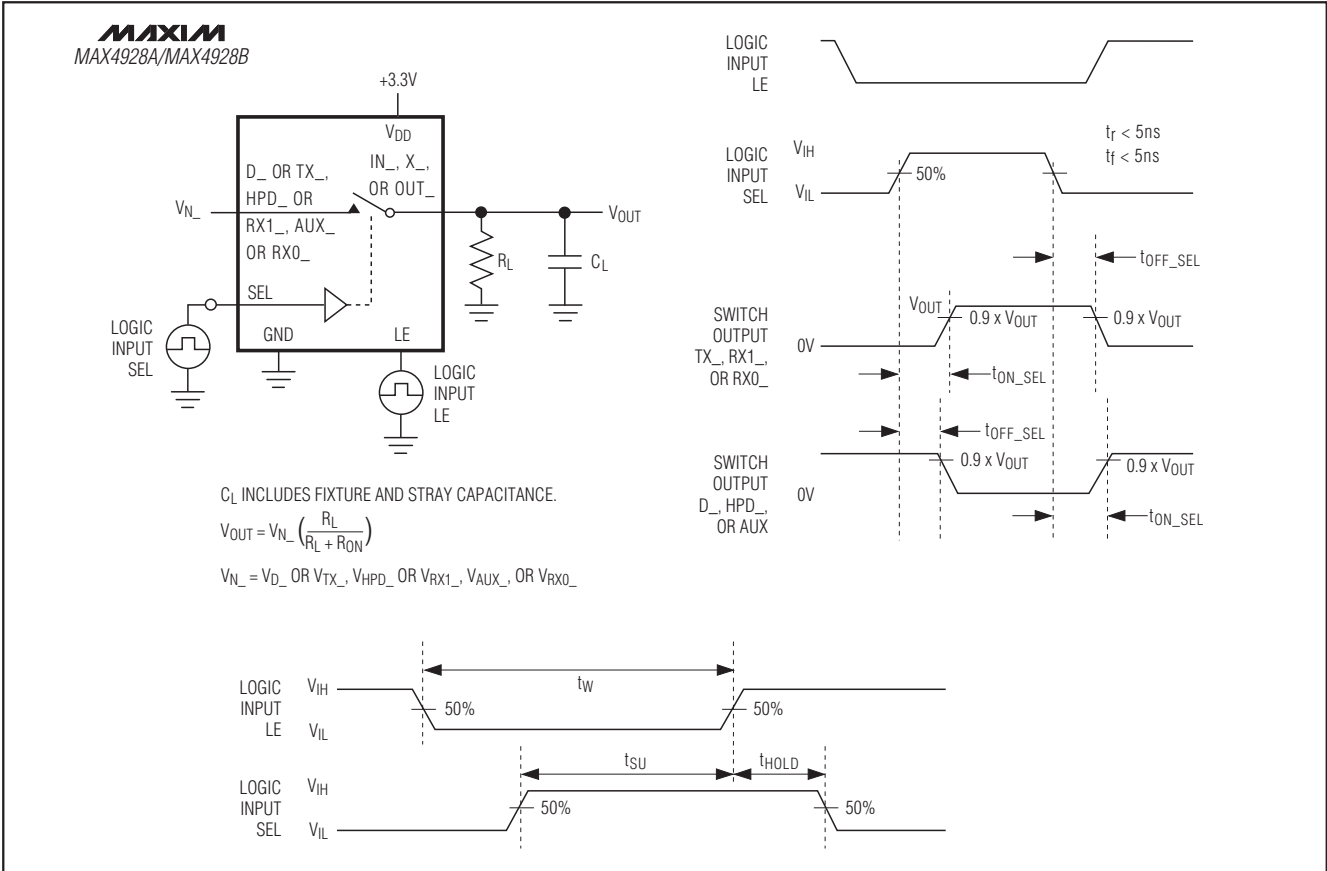


图1. 开关时间

DisplayPort/PCIE 无源开关

测试电路/时序图(续)

MAX4928A/MAX4928B

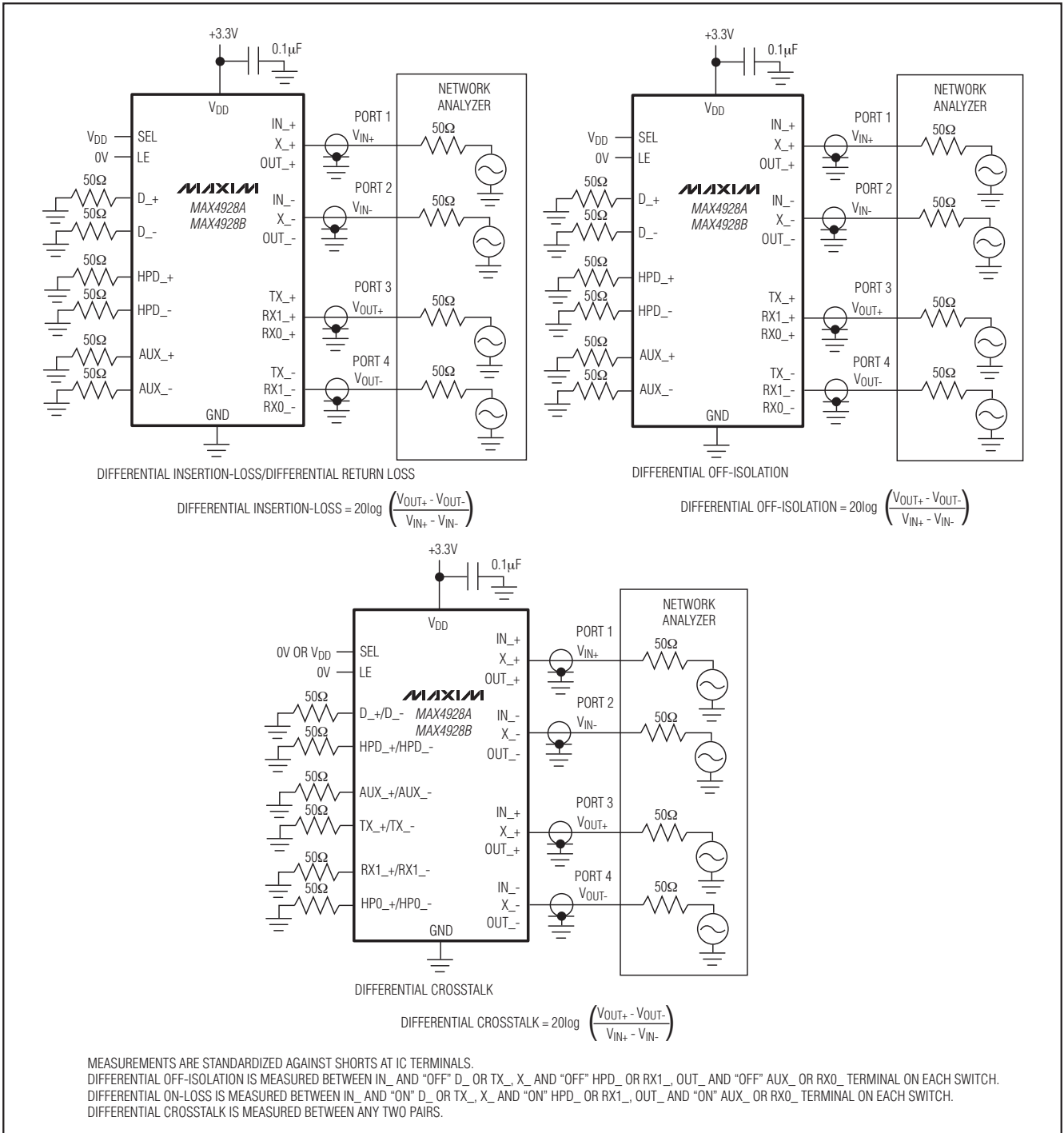


图2. 差分导通损耗、差分关断隔离和差分串扰

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引脚说明

MAX4928A/MAX4928B

引脚		名称	功能
MAX4928A	MAX4928B		
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	地。
2	4	IN0+	模拟开关1—公共正端。
3	5	IN0-	模拟开关1—公共负端。
4	7	IN1+	模拟开关2—公共正端。
5	8	IN1-	模拟开关2—公共负端。
6, 17, 22, 27, 34, 50, 55	6, 17, 22, 27, 34, 50, 55	V _{DD}	正电源电压输入，将V _{DD} 连接到+3.0V至+3.6V电源。通过0.1μF陶瓷电容将V _{DD} 旁路至GND，并尽量靠近器件放置电容，请参考电路板布局部分。
7	9	IN2+	模拟开关3—公共正端。
8	10	IN2-	模拟开关3—公共负端。
9	12	IN3+	模拟开关4—公共正端。
10	13	IN3-	模拟开关4—公共负端。
12	14	OUT+	模拟开关5—公共正端。
13	15	OUT-	模拟开关5—公共负端。
14	18	X+	模拟开关6—公共正端。
15	19	X-	模拟开关6—公共负端。
18	2	SEL	控制信号输入。
19	3	LE	锁存使能输入。
23	30	HPD2	模拟开关6—常开负端。
24	31	HPD1	模拟开关6—常开正端。
25	32	AUX-	模拟开关5—常开负端。
26	33	AUX+	模拟开关5—常开正端。
30	23	RX1-	模拟开关6—常闭负端。
31	24	RX1+	模拟开关6—常闭正端。
32	25	RX0-	模拟开关5—常闭负端。
33	26	RX0+	模拟开关5—常闭正端。
36	44	D3-	模拟开关4—常开负端。
37	45	D3+	模拟开关4—常开正端。
38	46	D2-	模拟开关3—常开负端。
39	47	D2+	模拟开关3—常开正端。
40	51	D1-	模拟开关2—常开负端。
41	52	D1+	模拟开关2—常开正端。
42	53	D0-	模拟开关1—常开负端。
43	54	D0+	模拟开关1—常开正端。
44	36	TX3-	模拟开关4—常闭负端。
45	37	TX3+	模拟开关4—常闭正端。
46	38	TX2-	模拟开关3—常闭负端。

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引脚说明(续)

引脚		名称	功能
MAX4928A	MAX4928B		
47	39	TX2+	模拟开关3—常闭正端。
51	40	TX1-	模拟开关2—常闭负端。
52	41	TX1+	模拟开关2—常闭正端。
53	42	TX0-	模拟开关1—常闭负端。
54	43	TX0+	模拟开关1—常闭正端。
—	—	EP	裸焊盘。连接EP至GND。裸焊盘内部连接至GND。

MAX4928A/MAX4928B

详细说明

MAX4928A/MAX4928B高速无源开关可在两个接收端之间切换PCI Express (PCIe)数据和/或DisplayPort信号。MAX4928A/MAX4928B可理想用于图形存储控制中心(GMCH)以及DisplayPort或PCIe连接器之间的信号切换。

MAX4928A/MAX4928B提供一个数字控制输入(SEL),用于控制信号路径,还提供锁存输入(LE),能够将开关保持至指定状态。

数字控制输入(SEL)

MAX4928A/MAX4928B提供单个数字控制输入(SEL),在IN_和D_/TX_、X_和HPD_/RX1_、OUT_和AUX_/RX0_通道之间选择信号路径。MAX4928A/MAX4928B对应的真值表在功能框图/真值表中给出。满幅驱动SEL可使功耗最低。

锁存控制输入(LE)

MAX4928A/MAX4928B提供一个控制输入(LE),用于锁存IN_和D_/TX_、X_和HPD_/RX1_、OUT_和AUX_/RX0_通道之间的信号路径。当LE拉高时,无论输入信号SEL如何,开关将保持原来的状态不变。满幅驱动LE可使功耗最低。

模拟信号幅度

MAX4928A/MAX4928B接收标准PCIe信号,最高电平可达($V_{DD} - 1.8V$)。IN_+通道的信号切换至D_+或TX_+通道,X_+通道的信号切换至HPD1或RX1+通道,OUT_+通道的信号切换至AUX_+或RX0+通道。IN_-通道的信号切换至D_-

或TX_-通道,X-通道的信号切换至HPD2或RX1-通道,OUT-通道的信号切换至AUX-或RX0-通道。MAX4928A/MAX4928B为双向开关,IN_、X_、OUT_、D_、TX_、HPD_、RX_和AUX_均可用作输入或输出。

应用信息

DisplayPort/PCIe切换

MAX4928A/MAX4928B主要用于GMCH与DisplayPort或PCIe连接器之间的切换。MAX4928A/MAX4928B内置n通道开关,允许在PCIe Gen II插槽或DisplayPort连接器之间选择差分信号。每个器件能够处理多达六对信号,DisplayPort信号为交流耦合的8b/10b编码差分信号,速率高达2.7Gbps;PCIe Gen I和Gen II信号为交流耦合的8b/10b编码差分信号,速率高达5.0Gbps。

电路板布局

高速开关需要适当的布局和设计,以优化系统性能。设计中,须使用阻抗受控的PCB引线并保持尽可能短的连线,或按照PCIe规范的阻抗布局。保证电源旁路电容尽量靠近器件放置,推荐使用多个旁路电容。所有地和裸焊盘连接到大的接地平面。

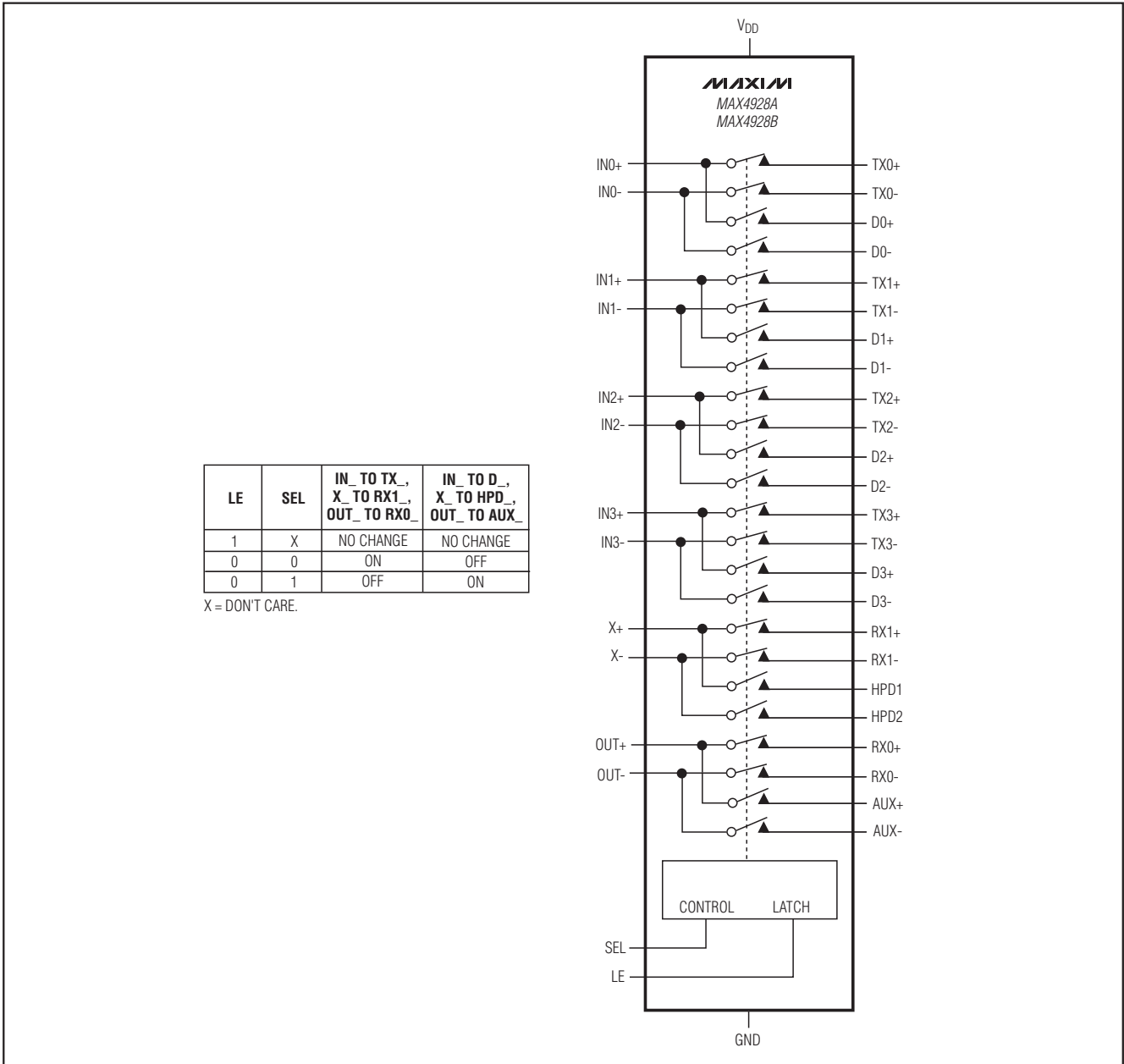
芯片信息

PROCESS: CMOS

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MAX4928A/MAX4928B

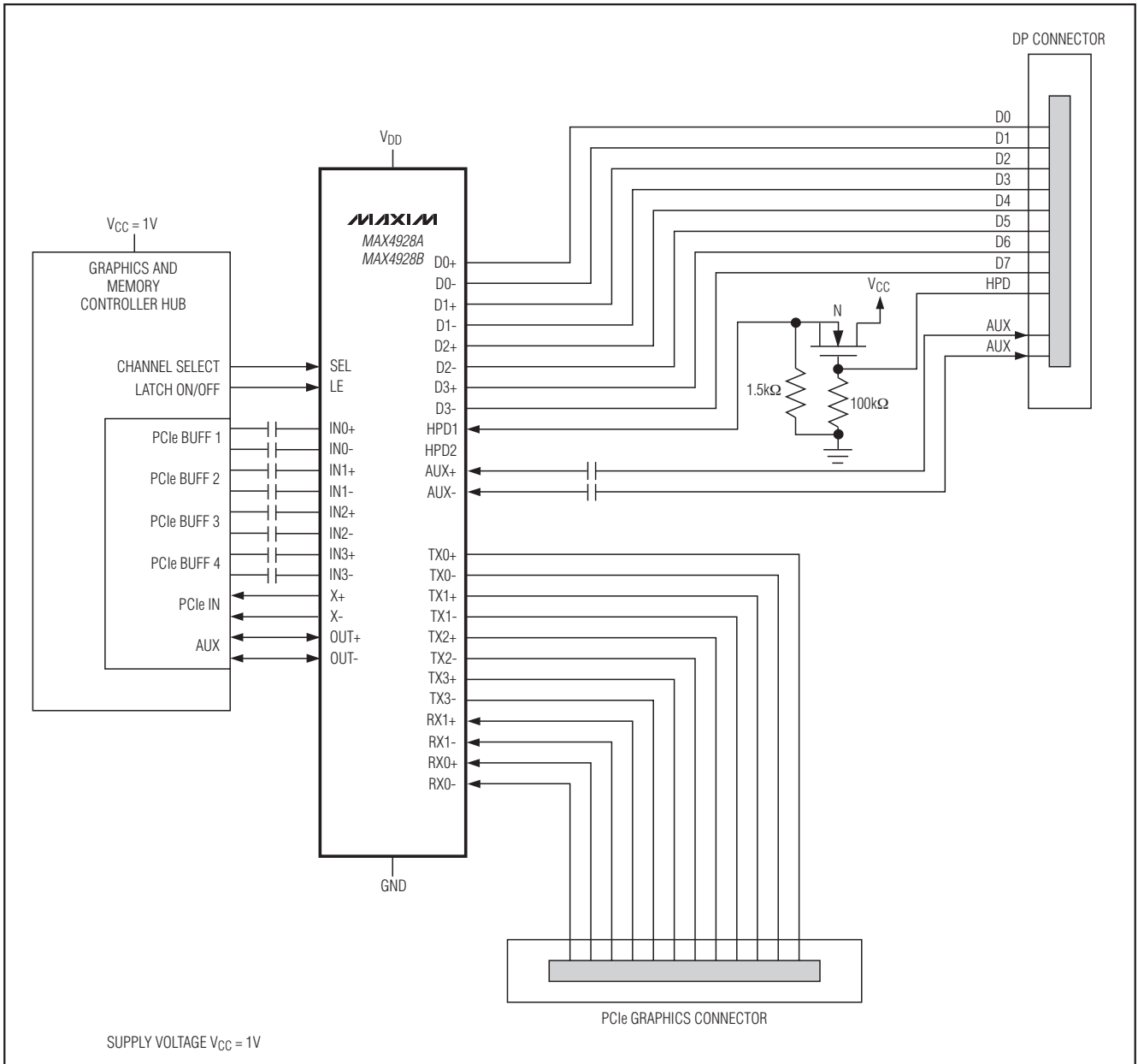
功能框图/真值表



DisplayPort/PCIE 无源开关

典型工作电路

MAX4928A/MAX4928B

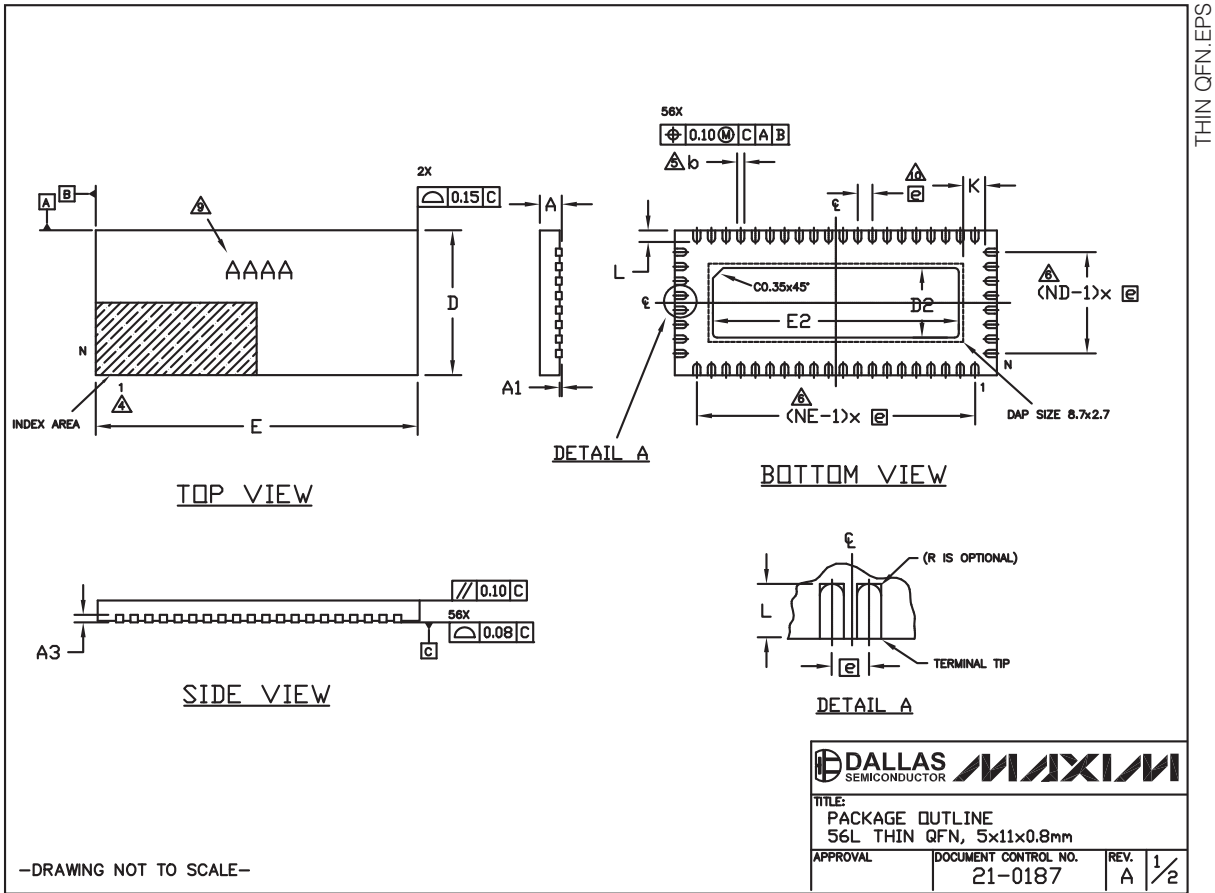


DisplayPort/PCIE 无源开关

MAX4928A/MAX4928B

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外形信息，请查询 www.maxim-ic.com.cn/packages.)



DisplayPort/PCIE 无源开关

封装信息(续)

(本数据资料提供的封装图可能不是最近的规格, 如需最近的封装外形信息, 请查询 www.maxim-ic.com.cn/packages.)

MAX4928A/MAX4928B

COMMON DIMENSIONS				
REF.	MIN.	NOM.	MAX.	NOTE
A	0.70	0.75	0.80	
A1	0	-	0.05	
A3	0.20 REF.			
b	0.20	0.25	0.30	
D	4.90	5.00	5.10	
E	10.90	11.00	11.10	
e	0.50 BSC.			
k	0.25	-	-	
L	0.30	0.40	0.50	
N	56			
ND	8			
NE	20			

PKG. CODE	EXPOSED PAD VARIATIONS					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T56511-1	2.30	2.40	2.50	8.30	8.40	8.50

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
- WARPAGE SHALL NOT EXCEED 0.10mm.
- MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
- LEAD CENTERLINES TO BE AT DEFINED BY DIMENSION e ±0.05.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 56L THIN QFN, 5x11x0.8mm	
APPROVAL	DOCUMENT CONTROL NO. 21-0187
REV. A	2/2

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