19-3389; Rev 0; 8/04

双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

MAX9969

概述

MAX9969为双通道、低功耗、高速、引脚电子驱动器/比较器IC，带有35mA负载。每通道包括三电平引脚驱动器、双路比较器、可调箝位电路和有源负载。附加的差分比较器可对两个通道进行比较。驱动器具有较宽的电压范围和高速工作特性，具备高阻和有源端接 (第3级驱动) 工作模式，在低电压摆幅下仍可保持高线性。双路比较器在各种输入条件下都能够保持很低的偏差 (时序变化)，并提供差分输出。器件配置为高阻接收器时，箝位电路为高速被测器件 (DUT) 波形提供阻尼衰减。负载可编程，提供最大35mA源出电流和吸入电流。可方便实现接触/连续测试、全速IOH和IOL参数测试，以及对高输出阻抗器件的上拉。MAX9969A为驱动器和比较器提供精确的失调匹配。

MAX9969提供兼容于LVPECL、LVDS和GTL的高速差分控制输入，具有可选择的内部端接电阻。比较器提供具有可选内部上拉电阻的集电极开路输出。这些功能可显著减少电路板分立元件数量。

MAX9969的低泄漏、限摆率和三态/端接工作模式通过3线、低压、CMOS兼容串口编程设置。

MAX9969的工作电压范围为-1.5V至+6.5V，每通道功耗仅为1.4W。器件可提供100引脚、14mm x 14mm面积、0.5mm引脚间距的TQFP封装。封装顶部的8mm x 8mm裸露焊盘可提高散热效率。管芯温度在+60°C至+100°C范围以内时器件可正常工作，具有管芯温度监视输出。

应用

高性能混合信号/片上系统ATE

高性能存储器ATE

特性

- 低功耗：每通道1.4W (典型值)
- 大大降低负载换流时的功耗
- 高速：3V_{P-P}时1200Mbps，1V_{P-P}时1800Mbps
- 可编程35mA有源负载电流
- 低时序偏差
- -1.5V至+6.5V宽工作电压范围
- 有源端接 (第3级驱动)
- 低泄漏模式：15nA
- 集成箝位电路
- 集成差分比较器
- 能够灵活地与多种逻辑电平接口
- 数字设置摆率
- 内部端接电阻
- 低失调误差
- 与MAX9967引脚兼容

定购信息

PART	TEMP RANGE	PIN-PACKAGE
MAX9969ADCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969AGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969ALCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969ARCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969BDCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969BGCCQ*	0°C to +70°C	100 TQFP-EPR**
MAX9969BLCCQ	0°C to +70°C	100 TQFP-EPR**
MAX9969BRCCQ	0°C to +70°C	100 TQFP-EPR**

*未来产品—供货信息请与厂商联系。
**EPR = 倒置裸露焊盘 (顶部)。

引脚配置和选择指南在数据资料的最后部分给出。

双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11V
V_{EE} to GND .....-5.75V to +0.3V
V_{CC} - V_{EE} .....-0.3V to +16.75V
GS to GND .....±1V
DUT_ to GND .....-2.75V to +7.5V
LDH_, LDL_ to GND .....-0.3V to +6V
DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_ to GND .....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_, LDEN_ to NLDEN_ .....±1.5V
TDATA_, TRCV_, TLDEN_ to GND .....-2.5V to +5V
DATA_, NDATA_, to TDATA_ .....±2V
RCV_, NRCV_, to TRCV_ .....±2V
LDEN_, NLDEN_ to TLDEN_ .....±2V
$V_{CCO\_}$ to GND .....-0.3V to +5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND .....-1V to +5V
DHV_, DLV_, DTV_, CHV_, CLV_, COM_ to GND .....-2.5V to +7.5V
CPHV_ to GND .....-1V to +8.5V
CPLV_ to GND .....-3.5V to +6V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_ .....±10V
CHV_ or CLV_ to DUT_ .....±10V
CH_, NCH_, CL_, NCL_ to GND .....-1V to +5V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current .....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V .....Continuous
Continuous Power Dissipation (T_A = +70°C)
MAX9969_ _CCQ (derate 167mW/°C above +70°C) ...13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+125°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-5.25	-4.75	-4.50	V
Positive Supply Current (Note 2)	I_{CC}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0, R_L ≥ 10MΩ		165	185	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		245	275	
Negative Supply Current (Note 2)	I_{EE}	$V_{LDH\_}$ = $V_{LDL\_}$ = 0, R_L ≥ 10MΩ		-235	-260	mA
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = -1V, load enabled, driver = high impedance		-315	-350	
Power Dissipation (Notes 2, 3)	P_D	$V_{LDH\_}$ = $V_{LDL\_}$ = 0		2.8	3.2	W
		$V_{LDH\_}$ = $V_{LDL\_}$ = 3.5V, R_L = 0, $V_{COM\_}$ = 1.5V, load enabled, driver = high impedance		3.3	3.7	
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 4)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±3	µA
Leakage Current in Low-Leakage Mode		LLEAK = 1; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±15	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		3	5	pF
		Driver in high-impedance mode		5	6	
Low-Leakage Enable Time		(Notes 5, 6)		20		µs
Low-Leakage Disable Time		(Notes 6, 7)		0.1		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Note 7)		4		µs
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_, CHV_, CLV_, CPHV_, CPLV_, COM_, LDH_, LDL_)						
Input Bias Current	I_{BIAS}	MAX9969_RCCQ			±25	µA
Settling Time		To 0.1% of full scale change (Note 7)		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_, LDEN_, NLDEN_)						
Input High Voltage	V_{IH}		0		3.5	V
Input Low Voltage	V_{IL}		-0.2		+3.1	V
Differential Input Voltage	V_{DIFF}	Between differential inputs	±0.15		±1.00	V
		Between a differential input and its termination voltage (Note 7)			±1.9	
Input Bias Current		MAX9969_DCCQ, MAX9969_RCCQ			±25	µA
Input Termination Voltage	$V_{TDATA\_}$ $V_{TRCV\_}$ $V_{TLDEN\_}$	MAX9969_GCCQ, MAX9969_LCCQ and MAX9969_RCCQ	0		+3.5	V
Input Termination Resistor		MAX9969_GCCQ, MAX9969_LCCQ, and MAX9969_RCCQ between signal and corresponding termination voltage input	47.5		52.5	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 5)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}			3.5			ns
DIN to SCLK High Setup	t_{DS}			3.5			ns
DIN to SCLK High Hold	t_{DH}			3.5			ns
$\overline{CS}$ Pulse Width High	t_{CSWH}			20			ns
TEMPERATURE MONITOR (TEMP)							
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ			3.33		V
Temperature Coefficient					+10		mV/°C
Output Resistance					20		kΩ
DRIVERS (Note 8)							
DC OUTPUT CHARACTERISTICS (R_L ≥ 10MΩ)							
DHV_, DLV_, DTV_, Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V	MAX9969A			±15	mV
			MAX9969B			±100	
DHV_, DLV_, DTV_, Output Offset Temperature Coefficient					+200		µV/°C
DHV_, DLV_, DTV_, Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V		0.960		1.001	V/V
DHV_, DLV_, DTV_, Gain Temperature Coefficient					-50		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 9)				±5	mV
		Full range (Notes 9, 10)				±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V				±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V				±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V				±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V				±2	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V				±2	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 11)				±18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$			±40		±80	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 12)		49	50	51	Ω
DC Output Resistance Variation	$\_R_{DUT\_}$	$I_{DUT\_}$ = ±1mA, ±8mA			0.5	1	Ω
		$I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA			0.75	1.5	
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)							
AC Drive Current				±80			mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V			15	22	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			110	130	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V			210	370	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Drive-Mode Undershoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V			4	11	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			20	65	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V			30	185	
Term-Mode Overshoot		(Note 13)	$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps 10% to 90%		60	150	mV
			$V_{DUT\_}$ = 3.0V_{P-P}, t_R = t_F = 500ps 10% to 90%		0		
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0			180	250	mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V			180	250	
High-Impedance Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0			100		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V			100		
Settling Time to within 25mV		3V step (Note 14)			4		ns
Settling Time to within 5mV		3V step (Note 14)			40		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 15)							
Prop Delay, Data to Output	t_{PDD}			1.5	1.7	2.0	ns
Prop Delay Match, t_{LH} vs. t_{HL}		3V_{P-P}			±40	±80	ps
Prop Delay Match, Drivers within Package		(Note 16)			40		ps
Prop Delay Temperature Coefficient					+1.6		ps/°C
Prop Delay Change vs. Pulse Width		0.2V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±70		ps
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±25	±50	
		1V_{P-P}, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±70		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±25	±50	
		3V_{P-P}, 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±80		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±35	±60	
		5V_{P-P}, Z_L = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width	MAX9969_DCCQ		±100		
			MAX9969_GCCQ MAX9969_LCCQ MAX9969_RCCQ		±100		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		50	75	ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	2.0	2.3	2.6	ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	3.0	3.4	3.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{PDZD}			-1.3	-1.1	-0.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{LH}			0.4	0.6	0.8	ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.7	2.0	2.3	ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	2.0	2.3	2.7	ns
Prop Delay Match, t_{PDDT} vs. t_{PDTD}			0.5	0.3	0.1	ns
Prop Delay Match, t_{PDDT} vs. t_{LH}			0.1	0.3	0.5	ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 10% to 90%	300	350	400	ps
		$1V_{P-P}$, 10% to 90%	330	390	450	
		$3V_{P-P}$, 10% to 90%	500	650	750	
		$5V_{P-P}$, Z_L = 500Ω, 10% to 90%	800	1000	1200	
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±50		ps
SC1 = 0, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	63	70	77	%
SC1 = 1, SC0 = 0 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	40	47	55	%
SC1 = 1, SC0 = 1 Slew Rate		Percent of full speed (SC0 = SC1 = 0), $3V_{P-P}$, 20% to 80%	18	25	32	%
Minimum Pulse Width		(Note 17) $0.2V_{P-P}$		550		ps
		(Note 17) $1V_{P-P}$		550	630	
		(Note 17) $3V_{P-P}$		850	1000	
		(Note 17) $5V_{P-P}$, Z_L = 500Ω		1300		
Data Rate		(Note 18) $0.2V_{P-P}$		1800		Mbps
		(Note 18) $1V_{P-P}$		1800		
		(Note 18) $3V_{P-P}$		1200		
		(Note 18) $5V_{P-P}$, Z_L = 500Ω		800		
Dynamic Crosstalk		(Note 19)		12		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 20)	0.6	1.0	1.3	ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 20)	0.6	1.0	1.3	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATORS (Note 8)							
DC CHARACTERISTICS							
Input Voltage Range	V_{IN}	(Note 4)		-1.5		+6.5	V
Differential Input Voltage	V_{DIFF}			±8			V
Hysteresis	V_{HYST}				0		mV
Input Offset Voltage	V_{OS}	$V_{DUT\_}$ = 1.5V	MAX9969A			±20	mV
			MAX9969B			±100	
Input Offset Voltage Temperature Coefficient					±10		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = -1.5V, +6.5V (Note 21)			±0.25	±2	mV/V
Linearity Error		(Note 10)	$V_{DUT\_}$ = 1.5V, 3V			±3	mV
			$V_{DUT\_}$ = -1.5V, +6.5V			±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = 1.5V (Note 11)			±0.035	±2	mV/V
AC CHARACTERISTICS (Note 22)							
Bandwidth		Term mode, t_R = t_F = 150ps		2	3		GHz
		High-impedance mode		0.65	0.75		
Minimum Pulse Width	$t_{PW(MIN)}$	(Note 23)	MAX9969_LCCQ and MAX9969_RCCQ		500	650	ps
			MAX9969_DCCQ and MAX9969_GCCQ		600		
Prop Delay	t_{PDL}			1.0	1.3	1.6	ns
Prop Delay Temperature Coefficient					+1.7		ps/°C
Prop Delay Match, High/Low vs. Low/High					±10	±50	ps
Prop Delay Match High vs. Low Comparator					±50		ps
Prop Delay Match, Comparators within Package		(Note 16)			±80		ps
Prop Delay Dispersion vs. Common-Mode Input		$V_{CHV\_}$ = $V_{CLV\_}$ = -1.4V to +6.4V (Note 24)			40	60	ps
Prop Delay Dispersion vs. Overdrive		$V_{CHV\_}$ = $V_{CLV\_}$ = 0.1V to 0.9V, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point			±40	±60	ps
		$V_{CHV\_}$ = $V_{CLV\_}$ = 40mV to 160mV, $V_{DUT\_}$ = $0.2V_{P-P}$, t_R = t_F = 150ps, 10% to 90% relative to timing at 50% point			±40	±60	
Prop Delay Dispersion vs. Pulse Width		0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width			±30	±50	ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prop Delay Dispersion vs. Slew Rate		0.5V/ns to 6V/ns slew rate, relative to 4V/ns slew rate			±30	±60	ps
Waveform Tracking 10% to 90%		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point, term mode			±40	±60	ps
		$V_{DUT\_}$ = 1.0V_{P-P}, t_R = t_F = 250ps, 10% to 90% relative to timing at 50% point, high-impedance mode			±190	±250	
		$V_{DUT\_}$ = 3V_{P-P}, t_R = t_F = 500ps, 10% to 90% relative to timing at 50% point, high-impedance mode			±150	±200	
DUT_ Slew-Rate Tracking		Term mode			6		V/ns
		High-impedance mode			5		
LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)							
$V_{CCO\_}$ Voltage Range	$V_{VCCO\_}$			0		3.5	V
$V_{CCO\_}$ Current	$I_{VCCO\_}$				32		mA
Output Low Voltage Compliance		Set by I_{OL}, R_{TERM}, and $V_{CCO\_}$			-0.5		V
Output High Current	I_{OH}	MAX9969_DCCQ, MAX9969_GCCQ		-0.1		+0.3	mA
Output Low Current	I_{OL}	MAX9969_DCCQ, MAX9969_GCCQ			8		mA
Output Current Swing		MAX9969_DCCQ, MAX9969_GCCQ		7.6		8.4	mA
Output High Voltage	V_{OH}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ		$V_{CCO\_}$ - 0.05	$V_{CCO\_}$ - 0.005	$V_{CCO\_}$ + 0.01	V
Output Low Voltage	V_{OL}	$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ			$V_{CCO\_}$ - 0.4		V
Output Voltage Swing		$I_{CH\_}$ = $I_{NCH\_}$ = $I_{CL\_}$ = $I_{NCL\_}$ = 0, MAX9969_LCCQ, MAX9969_RCCQ		380	400	420	mV
Output Termination Resistor	R_{TERM}	Single-ended measurement from $V_{CCO\_}$ to CH_, NCH_, CL_, NCL_, MAX9969_LCCQ, MAX9969_RCCQ		48		52	Ω
Differential Rise and Fall Times	t_R, t_F	20% to 80%	MAX9969_DCCQ, MAX9969_GCCQ, R_{TERM} = 50Ω at end of line		240		ps
			MAX9969_LCCQ, MAX9969_RCCQ		190	230	
CLAMPS							
High Clamp Input Voltage Range	$V_{CPH\_}$			0		+7.5	V
Low Clamp Input Voltage Range	$V_{CPL\_}$			-2.5		+5.0	V
Clamp Offset Voltage	V_{OS}	At DUT_ with $I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0				±100	mV
		At DUT_ with $I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0				±100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Offset-Voltage Temperature Coefficient					±250		µV/°C
Clamp Power-Supply Rejection Ratio	PSRR	(Note 11)	$I_{DUT\_}$ = 1mA, $V_{CPHV\_}$ = 0		±10		mV/V
			$I_{DUT\_}$ = -1mA, $V_{CPLV\_}$ = 0		±10		
Voltage Gain	A_V			0.960		1.005	V/V
Voltage-Gain Temperature Coefficient					-30		ppm/°C
Clamp Linearity		$I_{DUT\_}$ = 1mA, $V_{CPLV\_}$ = -1.5V, $V_{CPHV\_}$ = 0 to 6.5V			±10		mV
		$I_{DUT\_}$ = -1mA, $V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = -1.5V to +5V			±10		
Short-Circuit Output Current	$I_{SCDUT\_}$	$V_{CPHV\_}$ = 0, $V_{CPLV\_}$ = -1.5V, $V_{DUT\_}$ = 6.5V		40		80	mA
		$V_{CPHV\_}$ = 6.5V, $V_{CPLV\_}$ = 5V, $V_{DUT\_}$ = -1.5V		-80		-40	
Clamp DC Impedance	R_{OUT}	$V_{CPHV\_}$ = 3V, $V_{CPLV\_}$ = 0, $I_{DUT\_}$ = ±5mA and ±15mA		50		55	Ω
Clamp DC Impedance Variation		$V_{CPHV\_}$ = 2.5V; $V_{CPLV\_}$ = -1.5V; $I_{DUT\_}$ = 10mA, 20mA, 30mA			1.5		Ω
		$V_{CPHV\_}$ = 6.5V; $V_{CPLV\_}$ = 2.5V; $I_{DUT\_}$ = -10mA, -20mA, -30mA			1.5		
ACTIVE LOAD ($V_{COM\_}$ = 1.5V, R_L > 1MΩ, driver in high-impedance mode unless otherwise noted)							
COM_ Voltage Range	$V_{COM\_}$			-1		+6	V
Differential Voltage Range		$V_{DUT\_}$ - $V_{COM\_}$		-7.5		+7.5	V
COM_ Offset Voltage	Vos	I_{SOURCE} = I_{SINK} = 20mA				±100	mV
Offset-Voltage Temperature Coefficient					+100		µV/°C
COM_ Voltage Gain	A_V	$V_{COM\_}$ = 0, 4.5V; I_{SOURCE} = I_{SINK} = 20mA		0.98		1.00	V/V
Voltage-Gain Temperature Coefficient					-10		ppm/°C
COM_ Linearity Error		$V_{COM\_}$ = -1V, +6V; I_{SOURCE} = I_{SINK} = 20mA			±3	±15	mV
COM_ Output Voltage Power-Supply Rejection Ratio	PSRR	$V_{COM\_}$ = 2.5V, I_{SOURCE} = I_{SINK} = 20mA				±10	mV/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Resistance, Sink or Source	Ro	$V_{DUT\_}$ = 3V, 6.5V with $V_{COM\_}$ = -1V and $V_{DUT\_}$ = -1.5V, +2V with $V_{COM\_}$ = 6V	I_{SOURCE} = I_{SINK} = 35mA	30			kΩ
			I_{SOURCE} = I_{SINK} = 1mA	500			
Output Resistance, Linear Region	Ro	$I_{DUT\_}$ = ±33.25mA, I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 2.5V verfied by deadband test			11	15	Ω
Deadband		$V_{COM\_}$ = 2.5V, 95% I_{SOURCE} to 95% I_{SINK}			700	800	mV
SOURCE CURRENT ($V_{DUT\_}$ = 4.5V)							
Maximum Source Current		$V_{LDL\_}$ = 3.8V		36		40	mA
Source Programming Gain	A_{TC}	$V_{LDL\_}$ = 0.2V, 3V; $V_{LDH\_}$ = 0.1V		9.75	10	10.25	mA/V
Source Current Offset (Combined Offset of LDL_ and GS)	I_{OS}	$V_{LDL\_}$ = 200mV		-1000		0	µA
Source-Current Temperature Coefficient		I_{SOURCE} = 35mA			-15		µA/°C
Source-Current Power-Supply Rejection Ratio	PSRR	I_{SOURCE} = 25mA				±60	µA/V
		I_{SOURCE} = 35mA				±84	
Source Current Linearity		(Note 25)	$V_{LDL\_}$ = 100mV, 1V, 2.25V			±60	µA
			$V_{LDL\_}$ = 3V			±130	
SINK CURRENT ($V_{DUT\_}$ = -1.5V)							
Maximum Sink Current		$V_{LDH\_}$ = 3.8V		-40		-36	mA
Sink Programming Gain	A_{TC}	$V_{LDH\_}$ = 0.2V, 3V; $V_{LDL\_}$ = 0.1V		-10.25	-10	-9.75	mA/V
Sink-Current Offset (Combined Offset of LDH_ and GS)	I_{OS}	$V_{LDH\_}$ = 200mV		0		1000	µA
Sink-Current Temperature Coefficient		I_{SINK} = 35mA			+8		µA/°C
Sink-Current Power-Supply Rejection Ratio	PSRR	I_{SINK} = 25mA				±60	µA/V
		I_{SINK} = 35mA				±84	
Sink-Current Linearity		(Note 25)	$V_{LDH\_}$ = 100mV, 1V, 2.25V			±60	µA
			$V_{LDH\_}$ = 3V			±130	
GROUND SENSE							
GS Voltage Range	V_{GS}	Verified by GS common-mode error test		±250			mV
GS Common-Mode Error		$V_{DUT\_}$ = -1.5V, V_{GS} = ±250mV, $V_{LDH\_}$ - V_{GS} = 0.2V				±20	µA
		$V_{DUT\_}$ = +4.5V, V_{GS} = ±250mV, $V_{LDL\_}$ - V_{GS} = 0.2V				±20	
GS Input Bias Current		V_{GS} = 0				±25	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS (Z_L = 50Ω to GND)							
Enable Time	t_{EN}	(Note 26)	I_{SOURCE} = 10mA, $V_{COM\_}$ = -1V	3	3.5	4	ns
			I_{SINK} = 10mA, $V_{COM\_}$ = 1V	3	3.5	4	
Disable Time	t_{DIS}	(Note 26)	I_{SOURCE} = 10mA, $V_{COM\_}$ = 1V	1.7	2	2.3	ns
			I_{SINK} = 10mA, $V_{COM\_}$ = -1V	1.7	2	2.3	
Current Settling Time on Commutation		I_{SOURCE} = I_{SINK} = 1mA (Note 27)	To 10%		15		ns
			To 1.5%		50		
		I_{SOURCE} = I_{SINK} = 20mA (Note 27)	To 10%		3	5	
			To 1.5%		15		
Spike During Enable/Disable Transition		I_{SOURCE} = I_{SINK} = 35mA, $V_{COM\_}$ = 0			200	300	mV

Note 1: All minimum and maximum DC and driver 3V rise- and fall-time test limits are 100% production tested. All other test limits are guaranteed by design. Tests are performed at nominal supply voltages, unless otherwise noted.
Note 2: Total for dual device at worst-case setting.
Note 3: Does not include above ground internal dissipation of the comparator outputs. Additional power dissipation is typically (32mA x $V_{VCCO\_}$)
Note 4: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.
Note 5: Transition time from LLEAK being asserted to leakage current dropping below specified limits.
Note 6: Based on simulation results only.
Note 7: Transition time from LLEAK being deasserted to output returning to normal operating mode.
Note 8: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
Note 9: Specifications measured at the endpoints of the full range. Full range is -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V.
Note 10: Relative to straight line between 0 and 4.5V.
Note 11: Change in offset voltage with power supplies independently set to their minimum and maximum values.
Note 12: Nominal target value is 50Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.
Note 13: $V_{DTV\_}$ = midpoint of voltage swing, R_S = 50Ω. Measurement is made using the comparator.
Note 14: Measured from the crossing point of DATA_ inputs to the settling of the driver output.
Note 15: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ are 250ps (10% to 90%).
Note 16: Rising edge to rising edge or falling edge to falling edge.
Note 17: Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.
Note 18: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.
Note 19: Crosstalk from either driver to the other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.
Note 20: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_}$ < $V_{DTV\_}$ < $V_{DHV\_}$. If $V_{DTV\_}$ < $V_{DLV\_}$ or $V_{DTV\_}$ > $V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.
Note 21: Change in offset voltage over the input range.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, $V_{CCO\_}$ = +2.5V, SC1 = SC0 = 0, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, $V_{LDH\_}$ = $V_{LDL\_}$ = 0, V_{GS} = 0, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

Note 22: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 250ps, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = +0.5V. Comparator outputs are terminated with 50Ω to 1.25V and $V_{CCO\_}$ = 2.5V. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 23: At this pulse width, the output reaches at least 90% of its DC voltage swing. The pulse width is measured at the crossing points of the differential outputs.

Note 24: $V_{DUT\_}$ = 200mV_{P-P}. Overdrive = 100mV.

Note 25: Relative to segmented interpolations between 200mV, 2V, 2.5V, and 3.5V.

Note 26: Measured from crossing of LDEN_ inputs to the 50% point of the output current change.

Note 27: V_{COM} = 1V, R_S = 50Ω, driving voltage = 1.55V to 0.45V transition and 0.45V to 1.55V transition (at 1mA) or +2.5V to -0.5V transition and -0.5V to +2.5V transition (at 20mA). Settling time is measured from $V_{DUT\_}$ = 1V to I_{SINK}/I_{SOURCE} settling within specified tolerance.

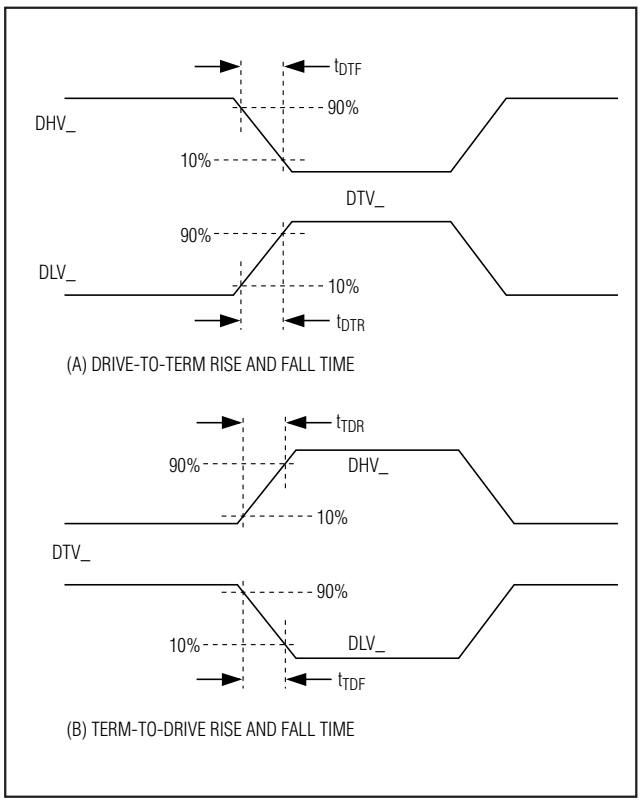
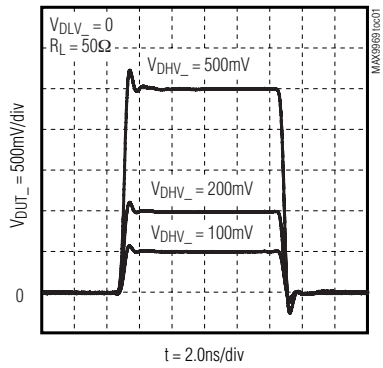


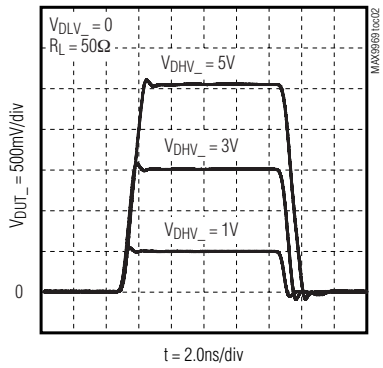
图1. 驱动至终端、终端至驱动的上升和下降时间

(T_A = +25°C, unless otherwise noted.)

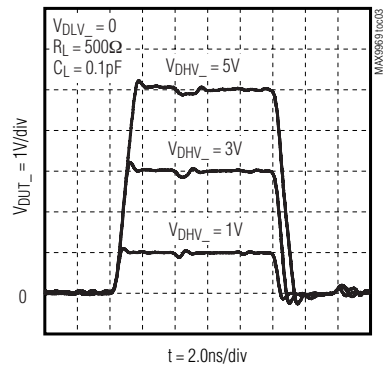
DRIVER SMALL-SIGNAL RESPONSE



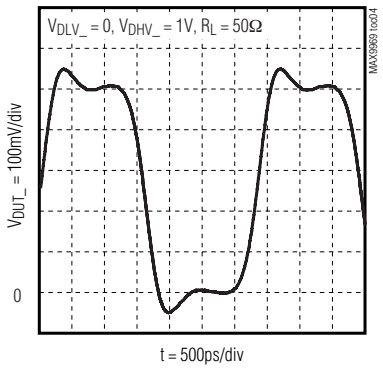
DRIVER LARGE-SIGNAL RESPONSE



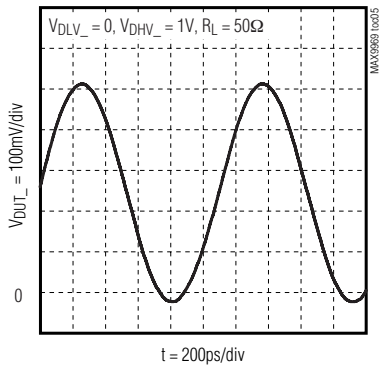
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



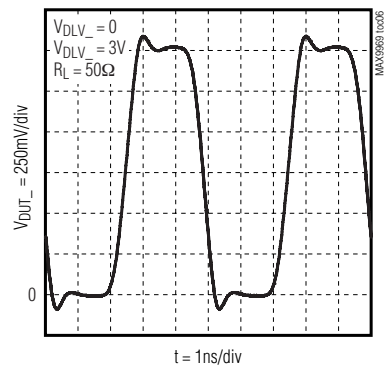
DRIVER 1V 600Mbps SIGNAL RESPONSE



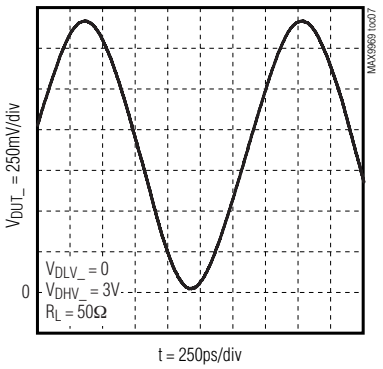
DRIVER 1V 1800Mbps SIGNAL RESPONSE



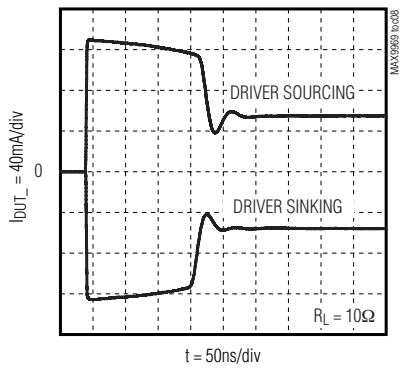
DRIVER 3V 400Mbps SIGNAL RESPONSE



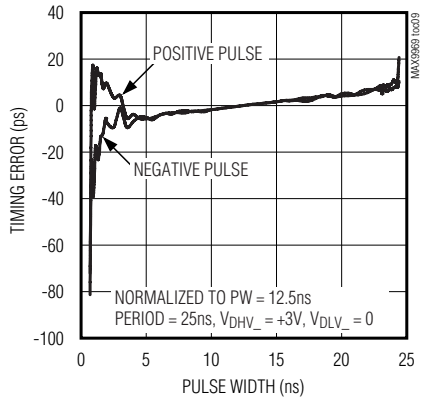
DRIVER 3V 1200Mbps SIGNAL RESPONSE



DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



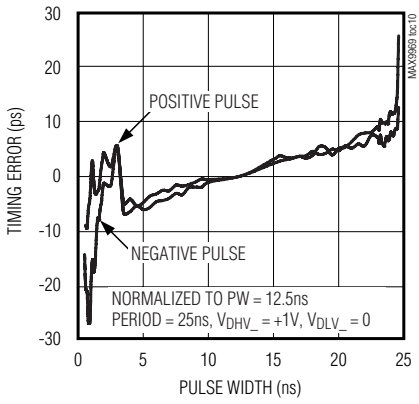
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



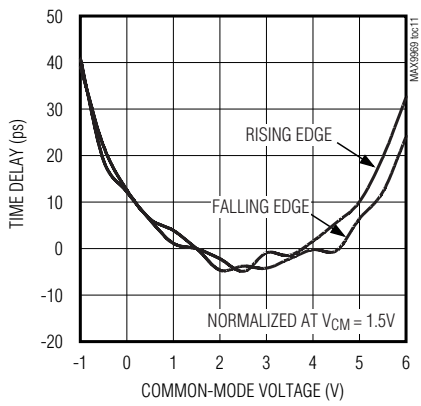
典型工作特性 (续)

(T_A = +25°C, unless otherwise noted.)

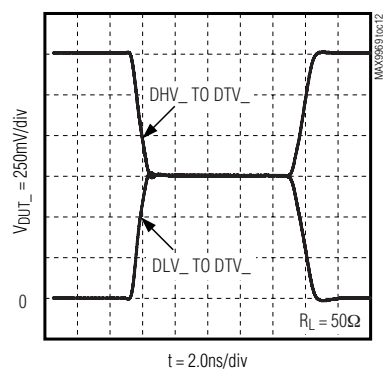
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



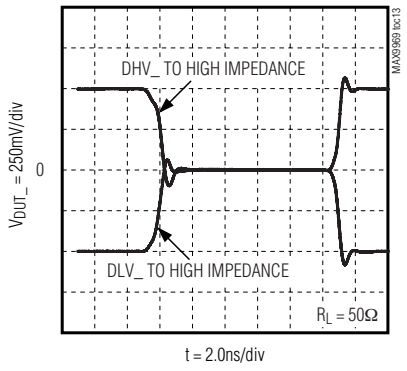
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



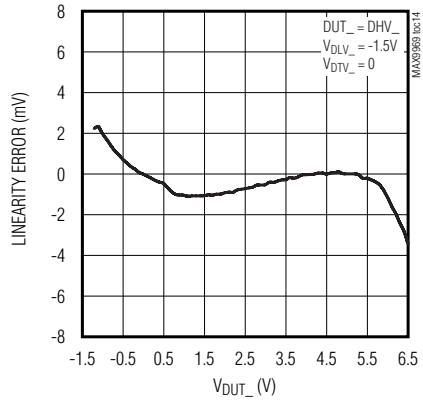
DRIVE-TO-TERM TRANSITION



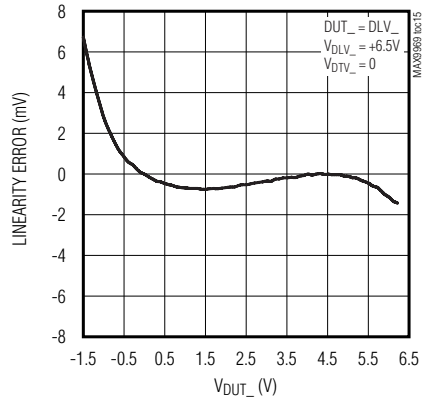
DRIVE TO HIGH-IMPEDANCE TRANSITION



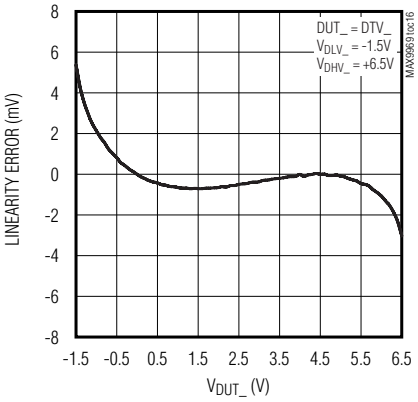
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



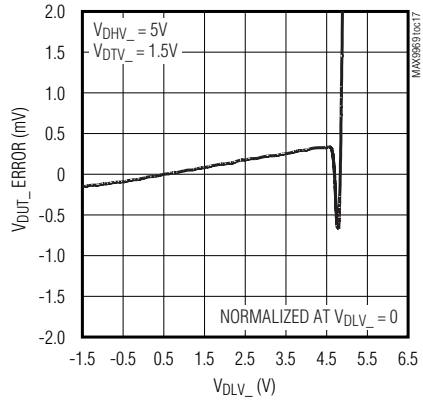
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



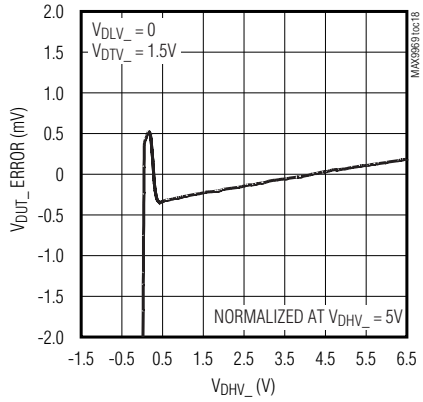
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_

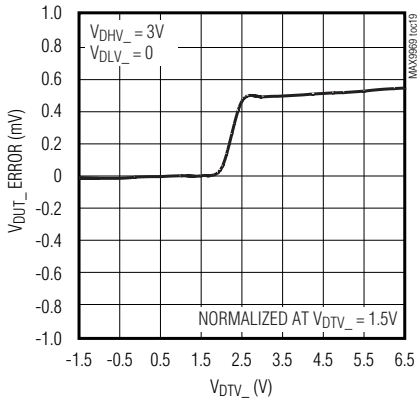


CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_

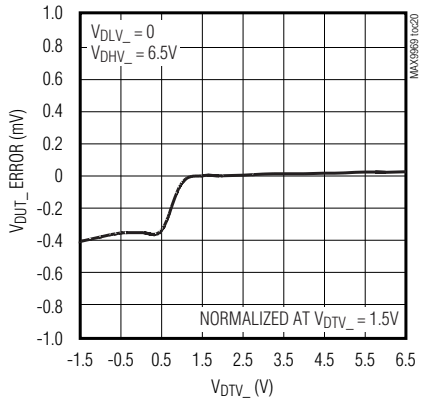


(T_A = +25°C, unless otherwise noted.)

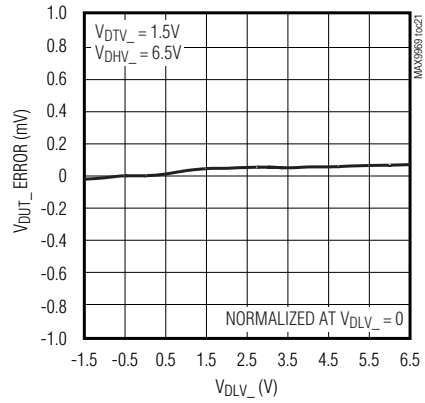
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



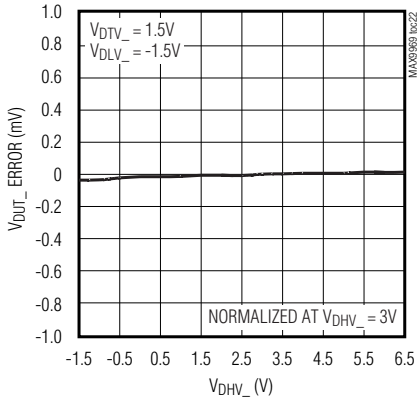
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



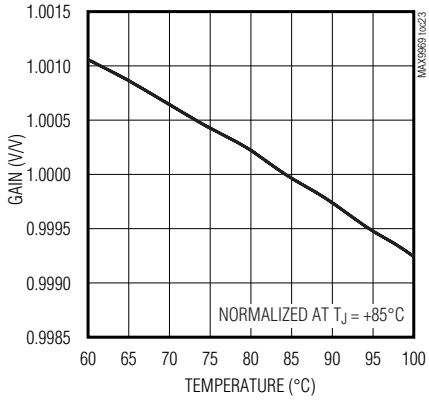
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



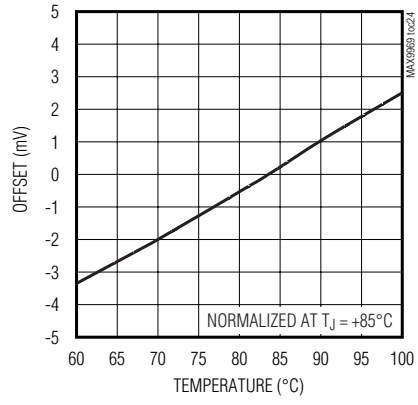
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



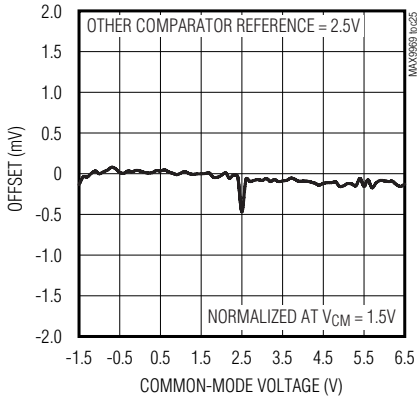
DRIVER GAIN vs. TEMPERATURE



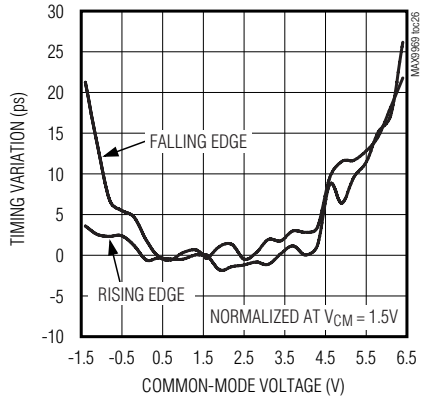
DRIVER OFFSET vs. TEMPERATURE



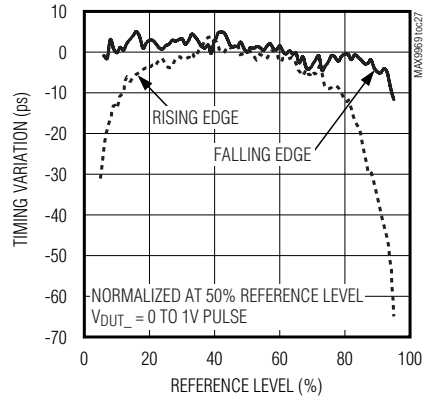
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE



COMPARATOR WAVEFORM TRACKING

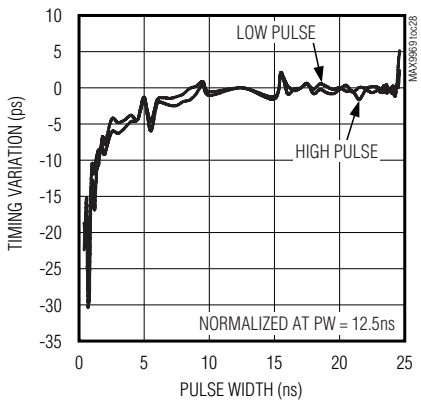


双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

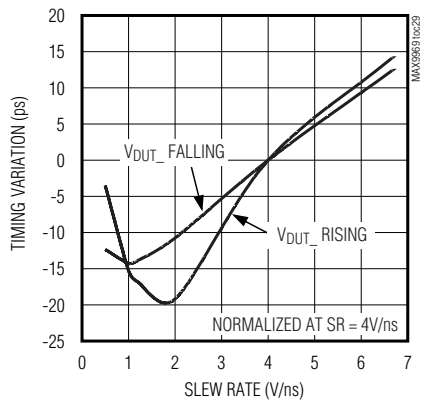
典型工作特性 (续)

(T_A = +25°C, unless otherwise noted.)

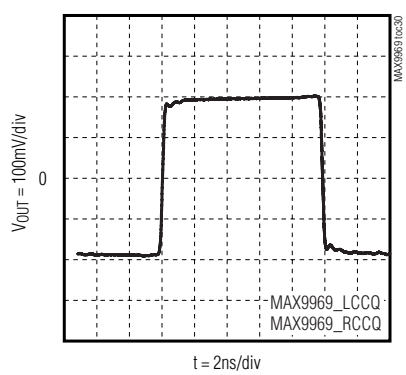
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE

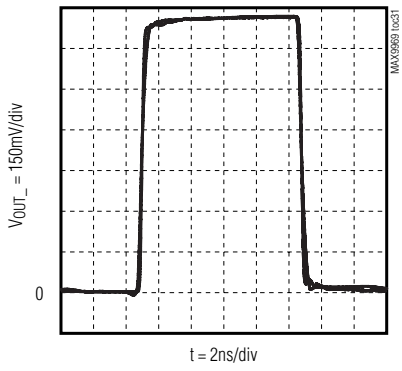


COMPARATOR DIFFERENTIAL OUTPUT RESPONSE



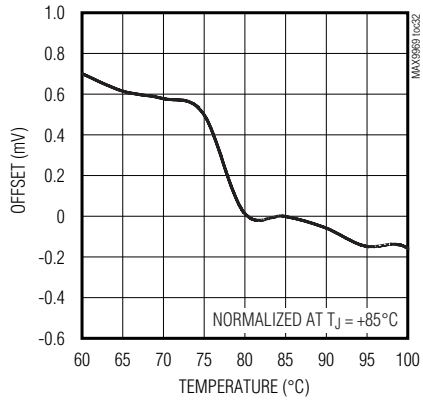
$V_{DUT\_}$ = 0 TO 3V PULSE
$V_{CHV\_} = V_{CLV\_}$ = 1.5V
EXTERNAL LOAD = 50Ω

COMPARATOR RESPONSE TO HIGH SLEW RATE OVERDRIVE

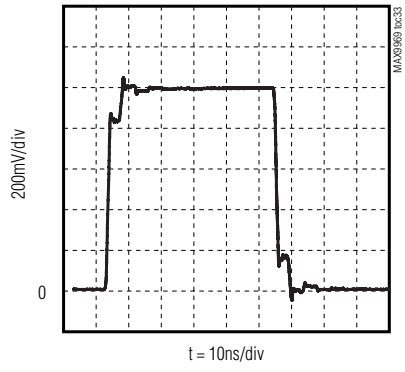


INPUT SLEW RATE = 4V/ns
HIGH IMPEDANCE

COMPARATOR OFFSET vs. TEMPERATURE

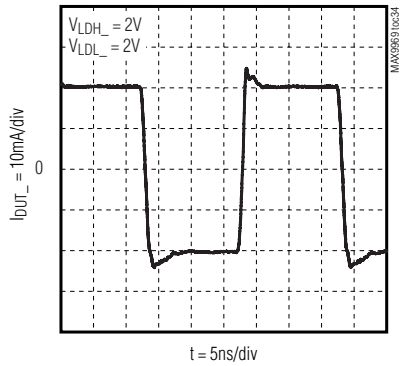


CLAMP RESPONSE AT SOURCE

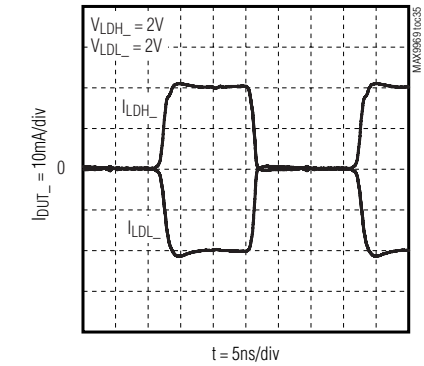


$V_{DUT\_}$ = 0 TO 1V SQUARE WAVE
R_S = 10Ω
$V_{CPLV\_}$ = -0.1V, $V_{CPHV\_}$ = +1.1V

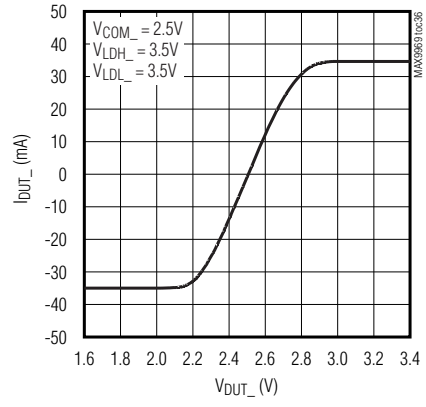
ACTIVE-LOAD COMMUTATION SIGNAL RESPONSE



ACTIVE-LOAD ENABLE SIGNAL RESPONSE



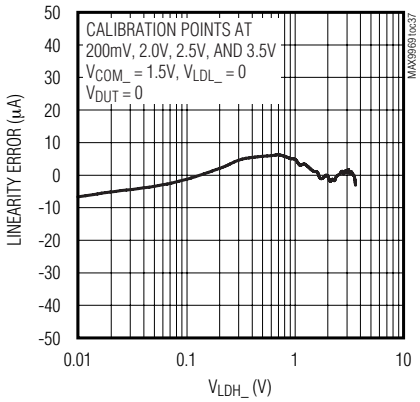
ACTIVE-LOAD CURRENT vs. LOAD VOLTAGE



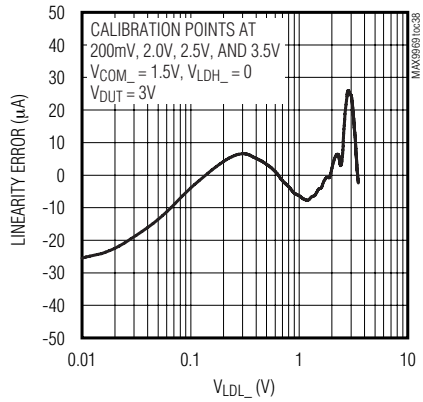
典型工作特性 (续)

(T_A = +25°C, unless otherwise noted.)

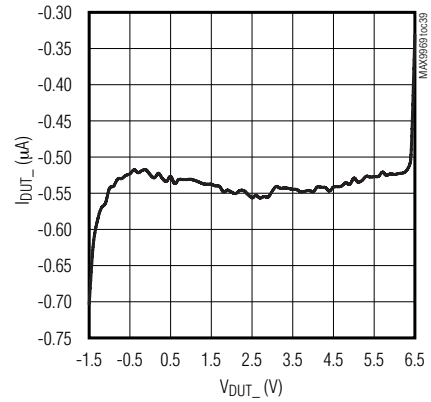
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. $V_{LDH\_}$



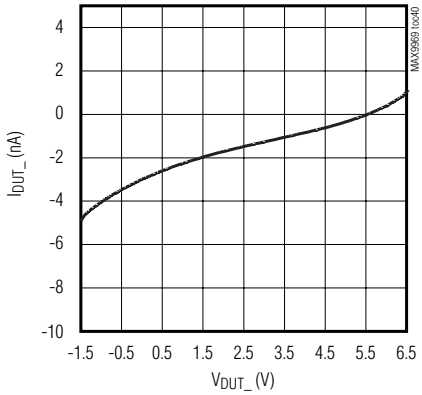
ACTIVE-LOAD LINEARITY ERROR $I_{DUT\_}$ vs. $V_{LDL\_}$



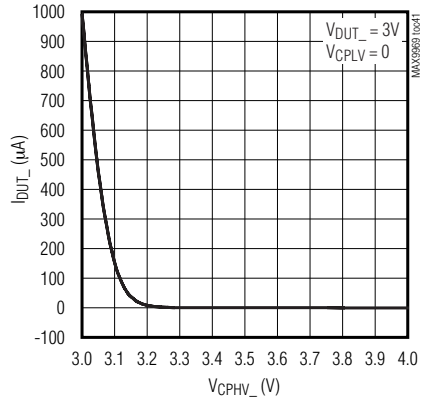
HIGH-IMPEDANCE CURRENT vs. DUT_ VOLTAGE



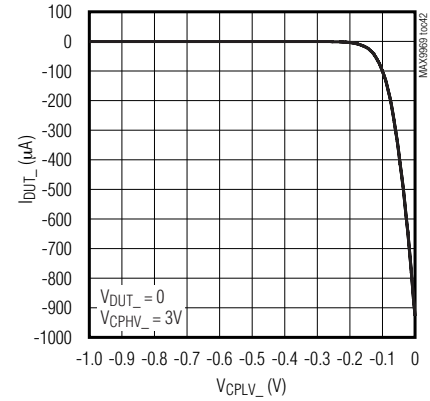
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



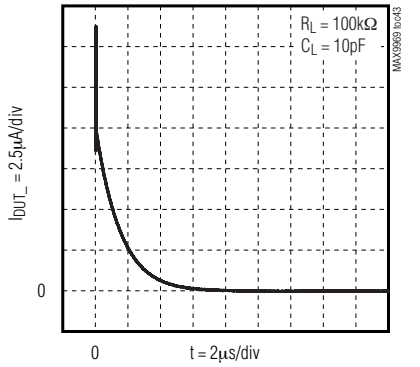
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



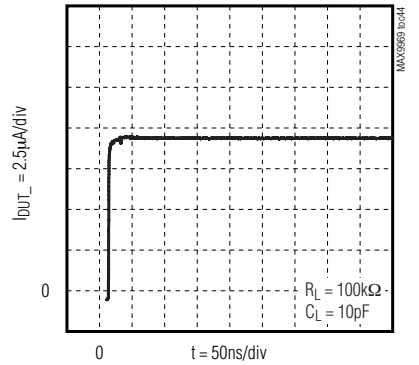
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



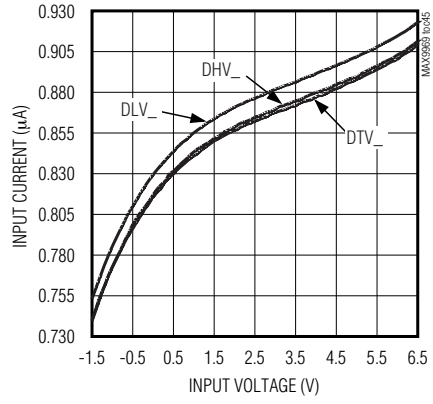
DRIVE 1V TO LOW-LEAKAGE TRANSITION



LOW-LEAKAGE TO DRIVE 1V TRANSITION



DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE

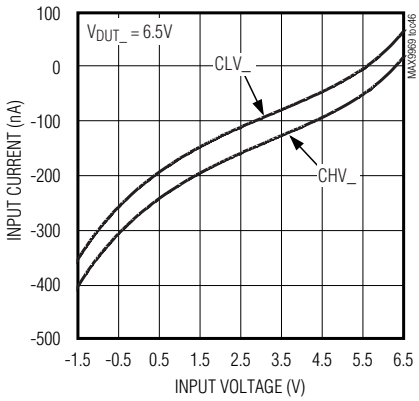


双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

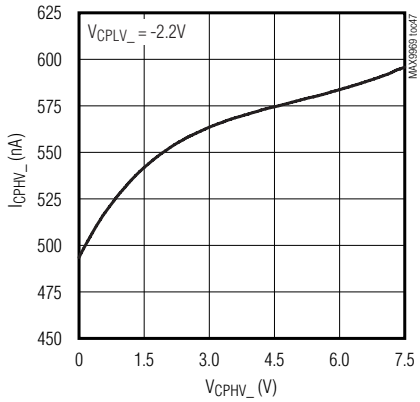
典型工作特性 (续)

(T_A = +25°C, unless otherwise noted.)

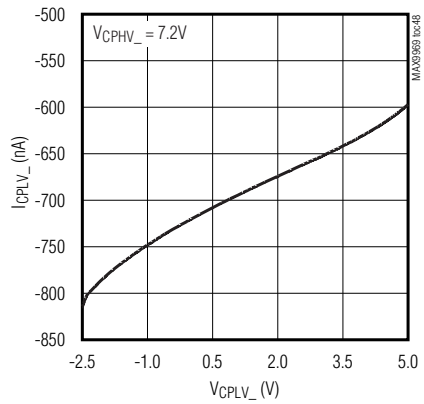
COMPARATOR REFERENCE CURRENT vs. INPUT VOLTAGE



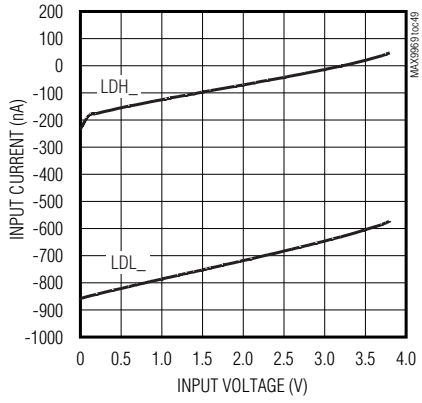
INPUT CURRENT vs. INPUT VOLTAGE, CPHV_



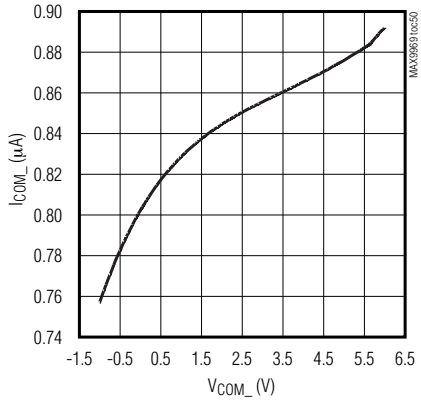
INPUT CURRENT vs. INPUT VOLTAGE, CPLV_



LOAD REFERENCE INPUT CURRENT vs. INPUT VOLTAGE



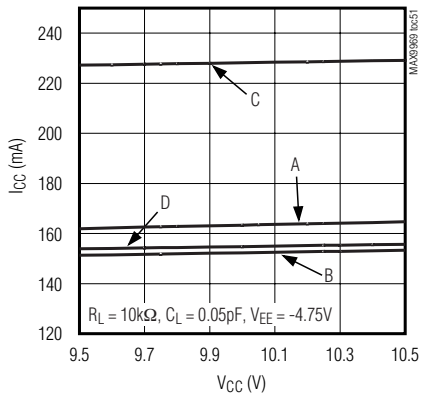
INPUT CURRENT vs. INPUT VOLTAGE, COM_



典型工作特性 (续)

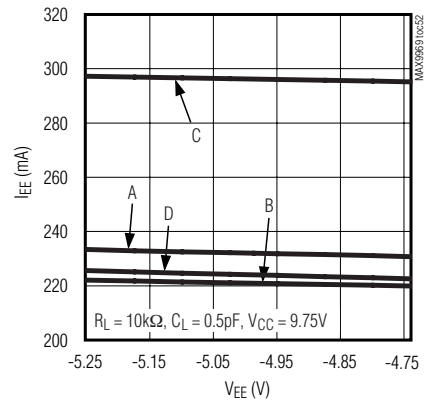
(T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT I_{CC} vs. V_{CC}



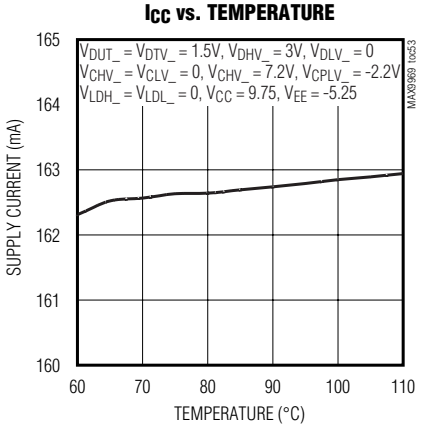
A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$
$V_{CHV\_} = V_{CLV\_} = 0$, $V_{CPHV\_} = 7.2V$, $V_{CPLV\_} = -2.2V$
$V_{LDH\_} = V_{LDL\_} = 0$, $I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$, $V_{COM\_} = 1.5V$, RL = 0
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

SUPPLY CURRENT I_{EE} vs. V_{EE}

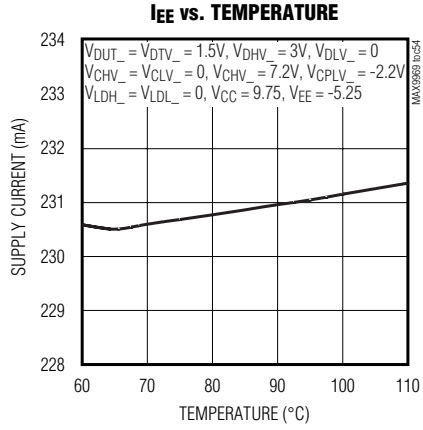


A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$
$V_{CHV\_} = V_{CLV\_} = 0$, $V_{CPHV\_} = 7.2V$, $V_{CPLV\_} = -2.2V$
$V_{LDH\_} = V_{LDL\_} = 0$, $I_{SOURCE} = I_{SINK} = 0$
B: SAME AS A EXCEPT DRIVER DISABLED HIGH-Z AND LOAD ENABLED
C: SAME AS B EXCEPT $I_{SOURCE} = I_{SINK} = 35mA$, $V_{COM\_} = -1V$, $R_L = 0$
D: SAME AS C EXCEPT LOW-LEAKAGE MODE ASSERTED

I_{CC} vs. TEMPERATURE



I_{EE} vs. TEMPERATURE



引脚说明

引脚	名称	功能
1	TEMP	温度监视输出。
2, 9, 12, 14, 17, 24, 35, 45, 46, 60, 80, 81, 91	V_{EE}	负电源输入。
3, 5, 10, 16, 21, 23, 25, 34, 43, 44, 82, 83, 92	GND	接地端。
4, 11, 15, 22, 33, 41, 42, 66, 84, 85, 93	V_{CC}	正电源输入。
6, 8, 18, 20, 50, 76	N.C.	无连接。不要连接。
7	DUT1	通道1 DUT输入/输出。多功能组合I/O用于驱动器、比较器、箝位电路和负载。
13	GS	地检测端。GS是LDH_和LDL_的地参考端。
19	DUT2	通道2 DUT输入/输出。多功能组合I/O用于驱动器、比较器、箝位电路和负载。
26	CLV2	通道2低端比较器基准输入。
27	CHV2	通道2高端比较器基准输入。
28	DLV2	通道2驱动器低端基准输入。
29	DTV2	通道2驱动器端接基准输入。
30	DHV2	通道2驱动器高端基准输入。
31	CPLV2	通道2低端箝位基准输入。
32	CPHV2	通道2高端箝位基准输入。
36	NCH2	通道2高端比较器输出。通道2高端比较器差分输出。
37	CH2	
38	V_{CCO2}	通道2集电极电压输入。通道2比较器输出端接电阻的电压输入。为输出端接电阻提供上拉电压和电流。对于内部没有端接电阻的器件，内部未连接。
39	NCL2	通道2低端比较器输出。通道2低端比较器差分输出。
40	CL2	
47	COM2	通道2有源负载换流电压基准输入。

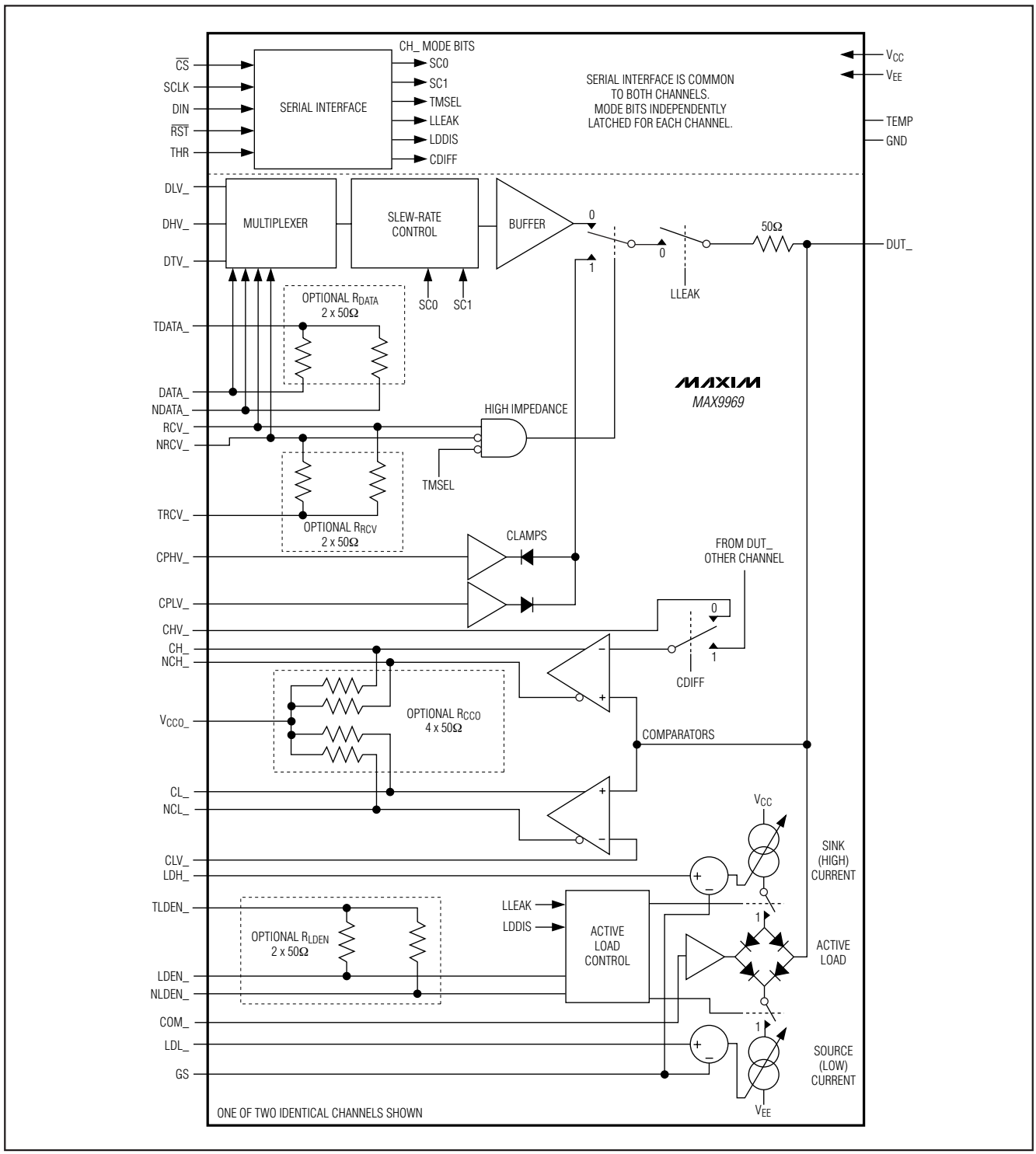
引脚说明 (续)

引脚	名称	功能
48	LDL2	通道2有源负载源出电流基准输入。
49	LDH2	通道2有源负载吸入电流基准输入。
51	TDATA2	通道2数据端接电压输入。DATA2和NDATA2差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
52	NDATA2	通道2多路复用器控制输入。通过差分控制输入DATA2和NDATA2选择DHV2或DLV2作为驱动器2的输入。DATA2高于NDATA2时选择DHV2；NDATA2高于DATA2时选择DLV2。
53	DATA2	
54	TRCV2	通道2 RCV端接电压输入。RCV2和NRCV2差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
55	NRCV2	通道2多路复用器控制输入。差分控制输入RCV2和NRCV2可将通道2置为接收模式。RCV2高于NRCV2时，通道2进入接收模式；NRCV2高于RCV2时，通道2进入驱动模式。
56	RCV2	
57	TLDEN2	通道2负载使能端接电压输入。LDEN2和NLDEN2差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
58	NLDEN2	通道2多路复用器控制输入。差分控制输入LDEN2和NLDEN2用来使能/禁用有源负载。LDEN2高于NLDEN2时，使能通道2有源负载；NLDEN2高于LDEN2时，禁用通道2有源负载。
59	LDEN2	
61	$\overline{RST}$	复位输入。串行寄存器异步复位输入。$\overline{RST}$低电平有效。
62	$\overline{CS}$	片选输入。串行端口使能输入。$\overline{CS}$低电平有效。
63	THR	单端逻辑门限。THR开路时，门限设置为+1.25V，也可将THR加载到所需的门限电压。
64	SCLK	串行时钟输入。串行端口时钟。
65	DIN	数据输入。串行端口数据输入。
67	LDEN1	通道1多路复用器控制输入。差分控制输入LDEN1和NLDEN1用于使能/禁用有源负载。LDEN1高于NLDEN1时，使能通道1有源负载；NLDEN1高于LDEN1时，禁用通道1有源负载。
68	NLDEN1	
69	TLDEN1	通道1负载使能端接电压输入。LDEN1和NLDEN1差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。

引脚说明 (续)

引脚	名称	功能
70	RCV1	通道1多路复用器控制输入。差分控制输入RCV1和NRCV1可将通道1置为接收模式。RCV1高于NRCV1时，通道1进入接收模式；NRCV1高于RCV1时，通道1进入驱动模式。
71	NRCV1	
72	TRCV1	通道1 RCV端接电压输入。RCV1和NRCV1差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
73	DATA1	通道1多路复用器控制输入。通过差分控制输入DATA1和NDATA1选择DHV1或者DLV1作为驱动器1的输入。DATA1高于NDATA1时选择DHV1；NDATA1高于DATA1时选择DLV1。
74	NDATA1	
75	TDATA1	通道1数据端接电压输入。DATA1和NDATA1差分输入的端接电压输入。对于没有内部端接电阻的器件，内部未连接。
77	LDH1	通道1有源负载吸入电流基准输入。
78	LDL1	通道1有源负载源出电流基准输入。
79	COM1	通道1有源负载换流电压基准输入。
86	CL1	通道1低端比较器输出。通道1低端比较器差分输出。
87	NCL1	
88	V_{CCO1}	通道1集电极电压输入。通道1比较器输出端接电阻的电压输入。为输出端接电阻提供上拉电压和电流。对于没有内部端接电阻的器件，内部未连接。
89	CH1	通道1高端比较器输出。通道1高端比较器差分输出。
90	NCH1	
94	CPHV1	通道1高端箝位基准输入。
95	CPLV1	通道1低端箝位基准输入。
96	DHV1	通道1驱动器高端基准输入。
97	DTV1	通道1驱动器端接基准输入。
98	DLV1	通道1驱动器低端基准输入。
99	CHV1	通道1高端比较器基准输入。
100	CLV1	通道1低端比较器基准输入。

功能框图



双通道、低功耗、1200Mbps ATE驱动器/比较器，带有35mA负载

详细说明

MAX9969为双通道、低功耗、高速、引脚电子DCL IC，每个通道都包括三电平引脚驱动器、双路比较器、可调箝位电路和有源负载。附加的比较器可对两个通道进行比较。驱动器可工作在-1.5V至+6.5V范围内，具有高速工作特性，它包括高阻和有源端接 (第3级驱动) 模式，在低电压摆幅下仍可保持高线性。双路比较器在各种输入条件下都具有较低的偏差 (时序变化)，并提供差分输出。器件配置为高阻接收器时，箝位电路为高速DUT波形提供阻尼衰减。负载可编程，提供最大35mA源出电流和吸入电流。可方便实现接触/连续测试、全速IOH和IOL参数测试、以及对高输出阻抗器件的上拉。MAX9969A为驱动器和比较器提供精确的失调匹配。

高速输入端口具有可选择的内部电阻，使器件能够兼容于LVPECL、LVDS和GTL接口。将端接电压输入 (TDATA_、TRCV_、TLDEN_) 连接至合适的电压，以实现与LV_PECL、GTL或其它逻辑电平的匹配连接。对于100Ω差分LVDS终端电阻，则保持输入悬空。另外，比较器提供具有可选内部上拉电阻的集电极开路输出。这些功能可显著减少电路板分立元件数量。

由3线、低压、CMOS兼容串口编程设置MAX9969的低泄漏、负载禁用、摆率、差分/窗口比较器和三态/端接运行模式。

输出驱动器

驱动器输入是一个高速多路复用器，可选择DHV_、DLV_或DTV_三个电压之一作为输入。该选择切换由高速输入DATA_、RCV_以及模式控制位TMSEL (表1) 进行控制。摆率电路控制缓冲器输入的摆率。可根据表2在四种摆率中进行选择。内部多路复用器速率设置为100%驱动器摆率 (*参考典型工作特性*中的Driver Large-Signal Response曲线)。

DUT_可在缓冲器输出和高阻模式之间高速转换，也可置为低泄漏模式 (见图2和表1)。高阻模式下，接入了箝位电路。高速输入RCV_和模式控制位TMSEL、LLEAK控制该切换。高阻模式下，DUT_的偏置电流在0至3V电压范围内小于3µA，而节点仍然能够跟踪高速信号。低泄漏模式下，DUT_的偏置电流进一步降至15nA以下，信号跟踪能力变慢。更多细节请参考*低泄漏模式*，*LLEAK*部分。

驱动器输出阻抗标称值为50Ω。若需45Ω至51Ω范围内的不同电阻值，请与厂商联系。

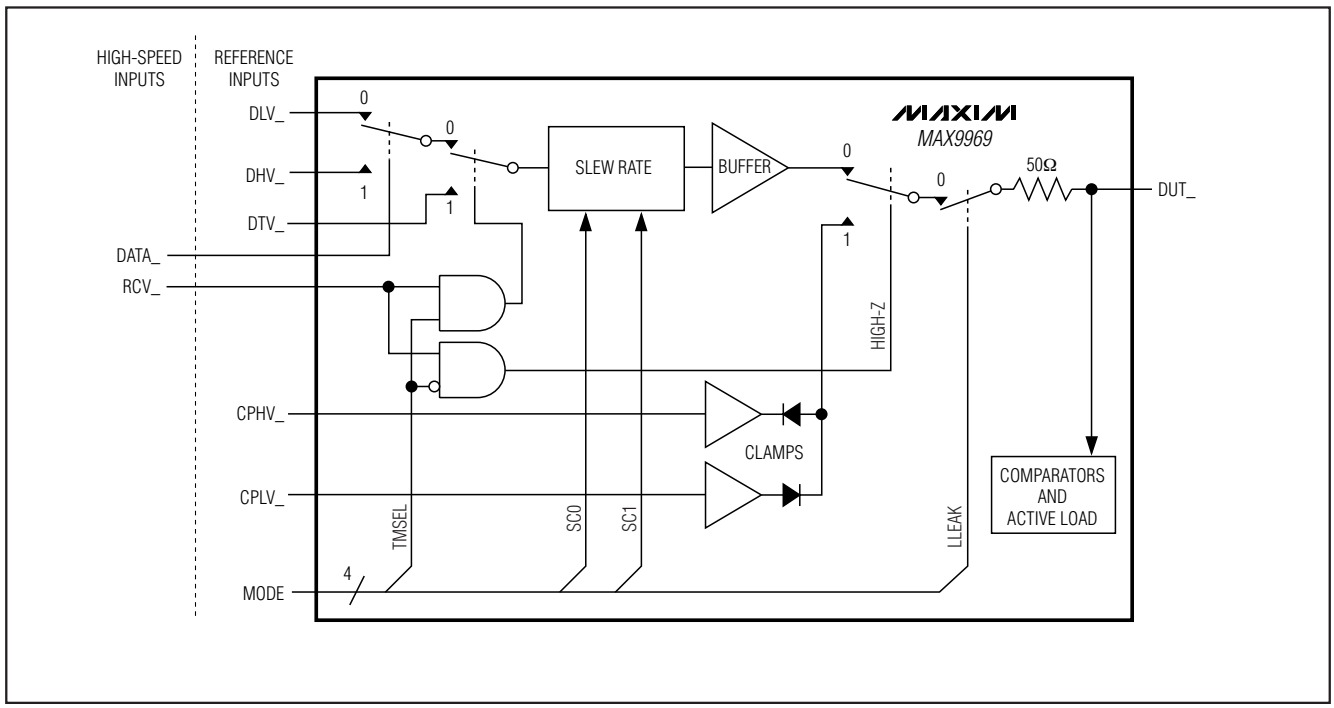


图2. 驱动器通道简图

表1. 驱动器控制逻辑

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA	RCV	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-Z)
X	X	X	1	Low-leakage mode

表2. 摆率控制逻辑

SC1	SC0	DRIVER SLEW RATE (%)
0	0	100
0	1	75
1	0	50
1	1	25

箝位电路

当通道配置为高阻接收器时，应设置电压箝位 (高电平和低电平) 以限制DUT_上的电压并抑制反射。箝位电路如同连接至大电流缓冲器输出的二极管。内部电路对1mA箝位电流的二极管压降进行补偿。使用外部连接端CPHV_和CPLV_设置箝位电压。箝位电路仅在驱动器处于高阻模式时有效 (图2)。为实现瞬态抑制，需设置箝位电压近似等于所需的最小和最大DUT_电压。最佳箝位电压取决于应用情况，需要根据经验确定。如果不需要箝位，应将箝位电压设置在超出所需DUT_电压范围的0.7V以外；没有加载DUT_时，过压保护电路仍然保持工作状态。

表3a. 比较器逻辑，CDIFF = 0

DUT_ > CHV_	DUT_ > CLV_	CL_, NCL_	CH_, NCH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

表3b. 比较器逻辑，CDIFF = 1

DUT1 > DUT2	DUT_ > CLV_	CL_, NCL_	CH_, NCH_
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1

比较器

MAX9969的每一个通道都含有两个独立的高速比较器。每个比较器的一个输入内部连接至DUT_，另一个输入连接至CHV_或者CLV_ (*参考功能框图*)。如表3a和表3b所示，比较器输出为输入的逻辑运算结果。

比较器差分输出采用集电极开路输出结构，很容易与多种逻辑电平接口。器件带有或不带内部端接电阻，在两个输出之间切换一个8mA电流源 (图3)。可选的端接电阻连接输出至电压输入$V_{CCO_}$。对于没有内部端接电阻的器件，则不要连接$V_{CCO_}$，并加入所需的外部电阻。这些典型值为50Ω的电阻连接至输出走线接收端的上拉电压。在不超出*Absolute Maximum Ratings*的条件下，也可以使用不同的配置结构。对于具有内部端接的器件，连接$V_{CCO_}$至所需的V_{OH}电压。每路输出提供标称值为400mV_{P-P}的摆幅和50Ω源终端匹配电阻。

高端比较器可配置为LVDS和其它差分DUT_信号接收器。当模式位CDIFF置位时，两个通道的高端比较器输入都切换至DUT_输出。

双通道、低功耗、1200Mbps ATE驱动器/比较器，带有35mA负载

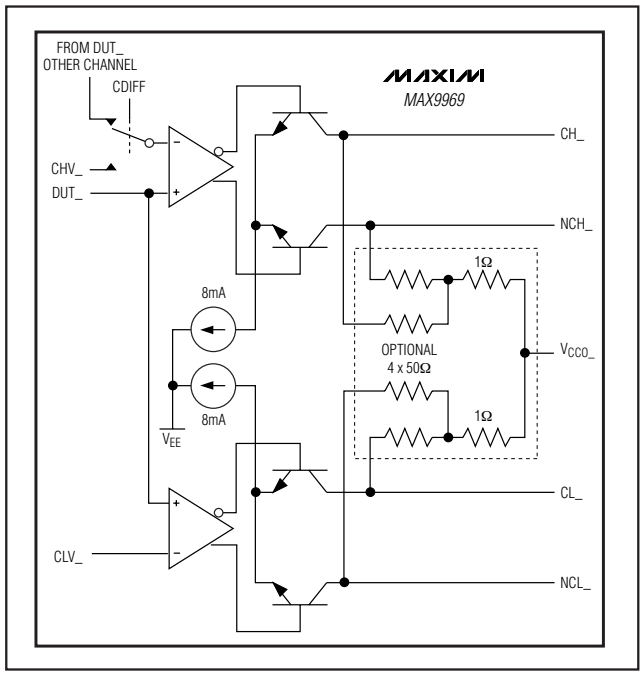


图3. 比较器集电极开路输出

有源负载

有源负载由线性可编程的AB类源出和吸入电流源、一个换流缓冲器和一个二极管桥 (*参考功能框图*) 组成。模拟控制输入LDH_和LDL_，分别在0至35mA范围内编程设置吸入和源出电流。模拟基准输入COM_设置换流缓冲器的输出电压。源出和吸入相对DUT而言。流出MAX9969的电流称为吸入电流，而流入MAX9969的电流称为源出电流。与常规的有源负载电路相比，MAX9969的AB类负载可提供更高的效率。

所设置的源出 (低) 电流在$V_{DUT_} > V_{COM_}$时，加载DUT。所设置的吸入 (高) 电流在$V_{DUT_} < V_{COM_}$时，加载DUT。

高速差分输入LDEN_以及控制字的2位 (LDDIS和LLEAK) 对负载进行控制 (表4)。当负载使能后，内部源出和吸入电流源连接至二极管桥。负载禁用后，内部电流源旁路至地，二极管桥的两端浮空 (*参考功能框图*)。LLEAK将负载置为低泄漏模式，优先级高于LDEN_。更多详细信息请参考*低泄漏模式，LLEAK*部分。

表4. 设置有源负载

EXTERNAL CONNECTIONS	INTERNAL CONTROL REGISTER		MODE
LDEN_	LDDIS	LLEAK	
0	0	0	Normal operating mode, load disabled
1	0	0	Normal operating mode, load enabled
X	1	0	Load disabled
X	X	1	Low-leakage mode

LDDIS

在一些测试仪配置中，负载使能由驱动器高阻信号 (RCV_) 的置反信号驱动，因此禁用驱动器将会使能负载，反之亦然。无论LDEN_为何状态 (表4)，LDDIS信号都可以禁用负载。

GS输入

GS输入允许使用MAX5631或MAX5734单电平设置DAC对MAX9969的有源负载、驱动器、比较器和箝位电路进行编程设置。尽管所有DAC电平通常由V_{GS}进行偏置，相对于有源负载电流而言，MAX9969的地检测输入消除了这种偏置影响。连接GS至DAC所使用的地参考端。($V_{LDL\_}$ - V_{GS}) 以+10mA/V的比率设置源出电流。($V_{LDH\_}$ - V_{GS}) 以-10mA/V的比率设置吸入电流。

为在GS变化时仍可维持8V的电压范围，DHV_、DLV_、DTV_、CPHV_、CPLV_和COM_范围由GS进行偏置。GS发生变化时，电源必须保持足够的余量，即确保：

$$V_{CC} \geq 9.5V + Max(V_{GS})$$

$$V_{EE} \leq -4.5V + Min(V_{GS})$$

低泄漏模式，LLEAK

通过串行端口将LLEAK置位，或者利用$\overline{RST}$可使MAX9969进入低泄漏状态 (*参考Electrical Characteristics*)。LLEAK置位时，比较器速度降低，并且禁用驱动器、箝位电路和有源负载。该模式不需要输出断开继电器，即可方便进行IDDQ和PMU测量。对于每个通道，LLEAK可独立编程设置。

双通道、低功耗、1200Mbps ATE驱动器/比较器，带有35mA负载

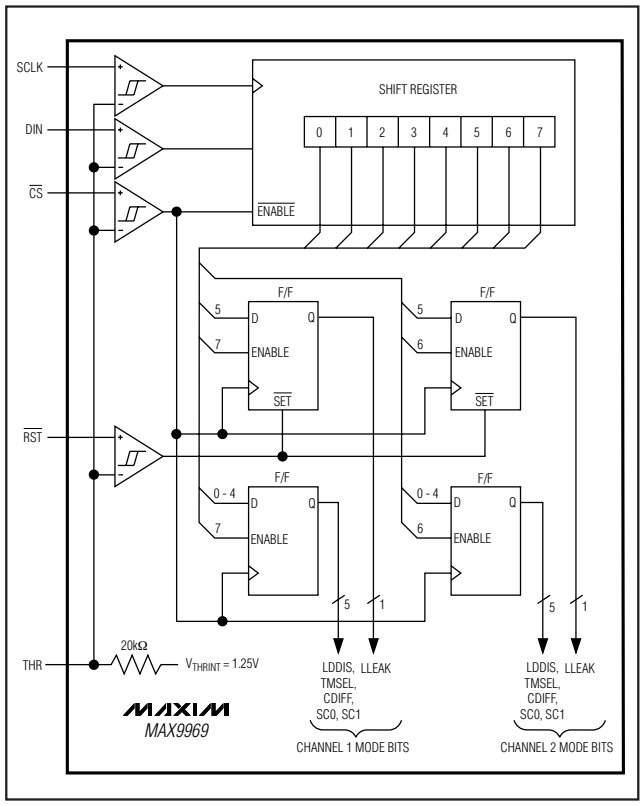


图4. 串口

当DUT_由高速信号驱动，而LLEAK置位时，泄漏电流会瞬间增加并超过正常工作所规定的限制值。*Electrical Characteristics*表中的低泄漏恢复指标给出了器件在这种条件下的运行状态。

串口和器件控制

CMOS兼容串行接口控制MAX9969的工作模式 (见图4和表5)。如图5所示，控制数据进入一个8位移位寄存器(MSB在前)，并在$\overline{CS}$变为高电平时锁存该数据。锁存器为双引脚驱动器的每个通道提供6个控制位。来自移位寄存器的数据装入其中一个或所有两个锁存器，具体由D6和D7决定。CDIFF = 1时，与D6、D7无关。控制位同外部输入DATA_和RCV_一起管理每个通道的功能，如表1和表2所示。$\overline{RST}$将所有两个通道设置为LLEAK = 1，强制它们进入低泄漏模式。其它所有位不受影响。上电时，在V_{CC}和V_{EE}稳定之前，$\overline{RST}$需保持低电平。

模拟控制输入THR用于设置输入逻辑电平的门限，允许与低至0.9V的CMOS逻辑电平接口。THR悬空时，会产生来自内部基准的1.25V门限电压，并与2.5V至3.3V逻辑电平兼容。

与MAX9967的兼容性

MAX9969与MAX9967引脚兼容，功能只有很少的差异。

- MAX9969没有PMU加载/检测端
- 控制输入具有不同的共模范围
- MAX9967的比较器输出还支持射极开路输出
- 不同的串行接口位结构

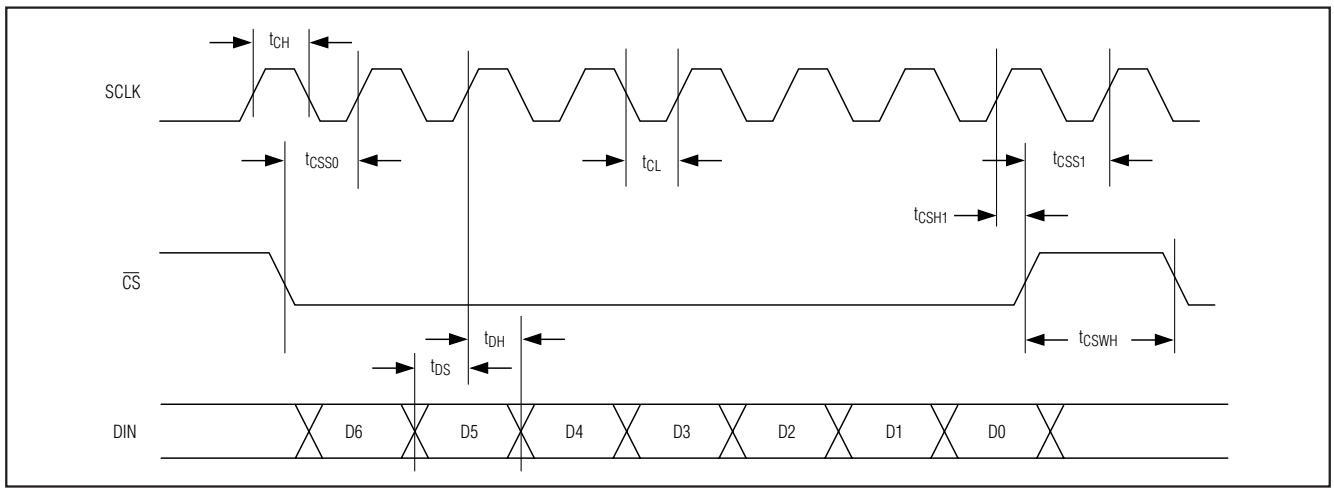


图5. 串口时序

双通道、低功耗、1200Mbps ATE驱动器/比较器，带有35mA负载

表5. 移位寄存器功能

BIT	NAME	DESCRIPTION
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.
D5	LLEAK	Low-Leakage Select. Set to 1 to put driver, load, and clamps in low-leakage mode. Comparators remain active in low-leakage mode, but at reduced speed. Set to 0 for normal operation.
D4	TMSEL	Termination Select. Driver Termination Select Bit. Set to 1 to force the driver output to the DTV_ voltage when RCV_ = 1 (term mode). Set to 0 to place the driver into high-impedance mode when RCV_ = 1 (high-Z). See Table 1.
D3	SC1	Driver Slew Rate Select. SC1 and SC0 set the driver slew rate. See Table 2.
D2	SC0	
D1	CDIFF	Differential Comparator Enable. Set to 1 to enable the differential comparators and disable the CH_ window comparators. Set to 0 to enable the CH_ window comparators and disable the differential comparators. See Tables 3a and 3b.
D0	LDDIS	Load Disable. Set LDDIS to 1 to disable the load. Set to 0 for normal operation. See Table 4.

温度监视

MAX9969提供温度输出信号TEMP，在管芯温度为+70°C (343K) 时输出标称值为3.33V的电压。此输出电压以10mV/°C的比率随温度变化。

散热

在正常环境下，MAX9969需要采用外部散热器并通过裸露焊盘进行散热。裸露焊盘与V_{EE}等电势，必需连接至V_{EE}或者进行隔离处理。

功耗与具体应用密切相关。*Electrical Characteristics*表给出了源出电流和吸入电流设置为0mA时器件的功耗情况。当源出和吸入电流都达到35mA，$V_{DUT_}$处于电压范围(-1.5V或+6.5V)的极限值，并且二极管桥换流达到满摆幅时，功耗最大。在这些条件下，增加的功耗 (每个通道) 为：

如果DUT_源出电流：

$$P_D = (V_{DUT\_} - V_{EE}) \times I_{SOURCE}$$

如果DUT_吸入电流：

$$P_D = (V_{CC} - V_{DUT\_}) \times I_{SINK}$$

当$V_{DUT_} > V_{COM_}$时，DUT_源出(低)所设置的电流。电流路径为从DUT_开始，流经二极管桥的外侧、源出 (低) 电流源，到达V_{EE}。AB类负载结构使所设置的吸入电流大大降低。

当$V_{DUT_} < V_{COM_}$时，DUT_吸入(高)所设置的电流。电流路径从V_{CC}开始，流经吸电流 (高) 电流源、二极管桥外侧，到达DUT_。AB类结构使所设置的源出电流大大降低。

带裸露焊盘的封装θ_{JC}很低，大约为1°C/W至2°C/W。因此管芯温度很大程度上取决于应用中使用的散热方案。在以下条件下产生最大总功耗：

- V_{CC} = +10.5V
- V_{EE} = -5.25V
- 所有两个通道：$I_{SOURCE} = I_{SINK}$ = 35mA
- 负载使能
- $V_{DUT\_}$ = -1.5V
- $V_{COM\_}$ = +0.5V

在这些极限条件下，总功耗典型值为3.9W，最大值为4.4W。如果在这些条件下管芯温度不能维持在可以接受的水平，使用软件箝位限制负载输出电流至较低值和/或降低电源电压。

电源注意事项

用0.01µF电容旁路所有V_{CC}和V_{EE}电源输入引脚，并对每路电源使用至少10µF的大容量电容进行旁路。

芯片信息

TRANSISTOR COUNT: 5284

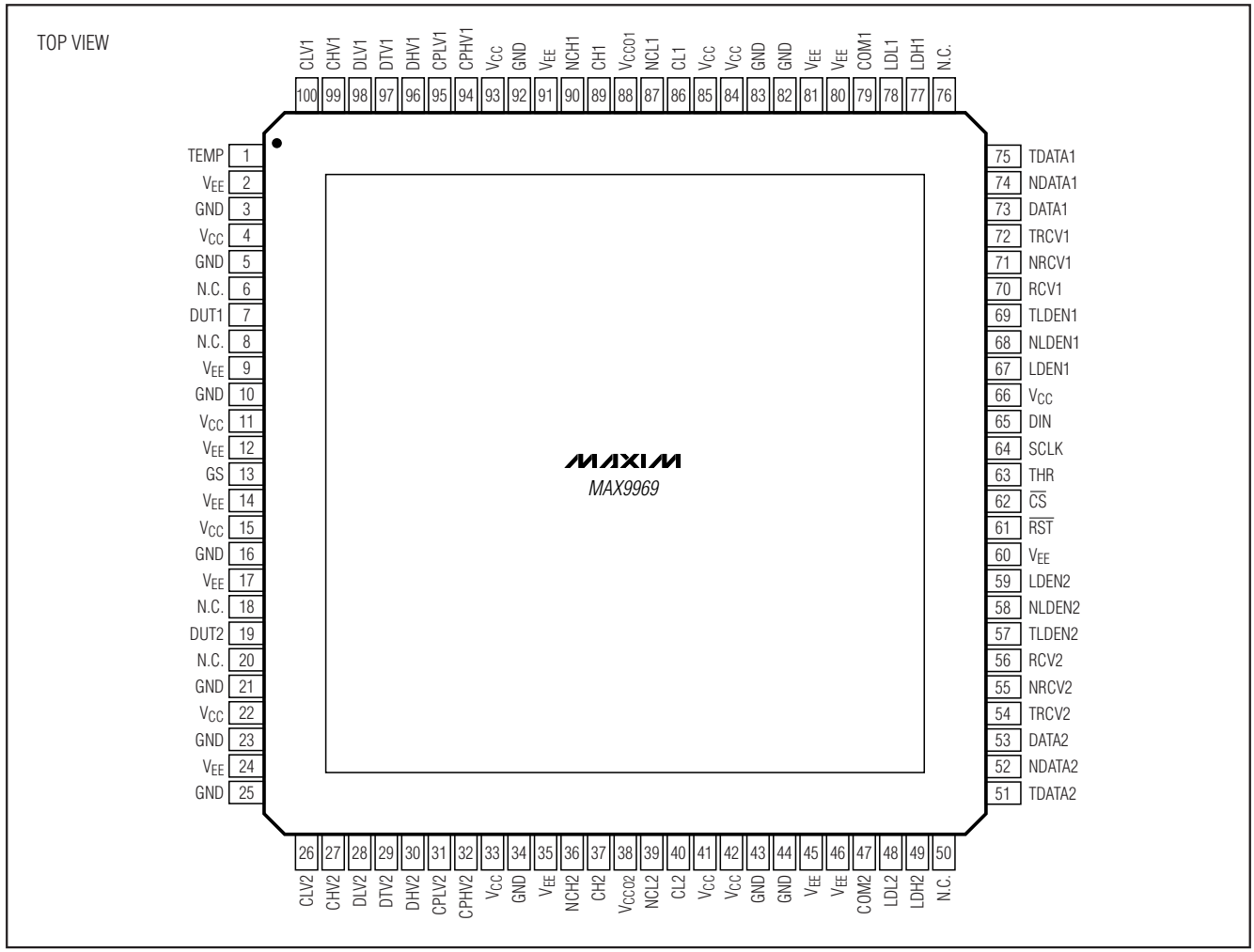
PROCESS: Bipolar

双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

选择指南

PART	ACCURACY GRADE	COMPARATOR OUTPUT TERMINATION	HIGH-SPEED DIGITAL INPUT TERMINATION (Ω)			HEAT EXTRACTION
			RCV_	DATA_	LDEN_	
MAX9969ADCCQ	A	None	None	None	None	Top
MAX9969AGCCQ	A	None	100	100	100	Top
MAX9969ALCCQ	A	50Ω to VCCO_	100	100	100	Top
MAX9969ARCCQ	A	50Ω to VCCO_	None	100	100	Top
MAX9969BDCCQ	B	None	None	None	None	Top
MAX9969BGCCQ	B	None	100	100	100	Top
MAX9969BLCCQ	B	50Ω to VCCO_	100	100	100	Top
MAX9969BRCCQ	B	50Ω to VCCO_	None	100	100	Top

引脚配置

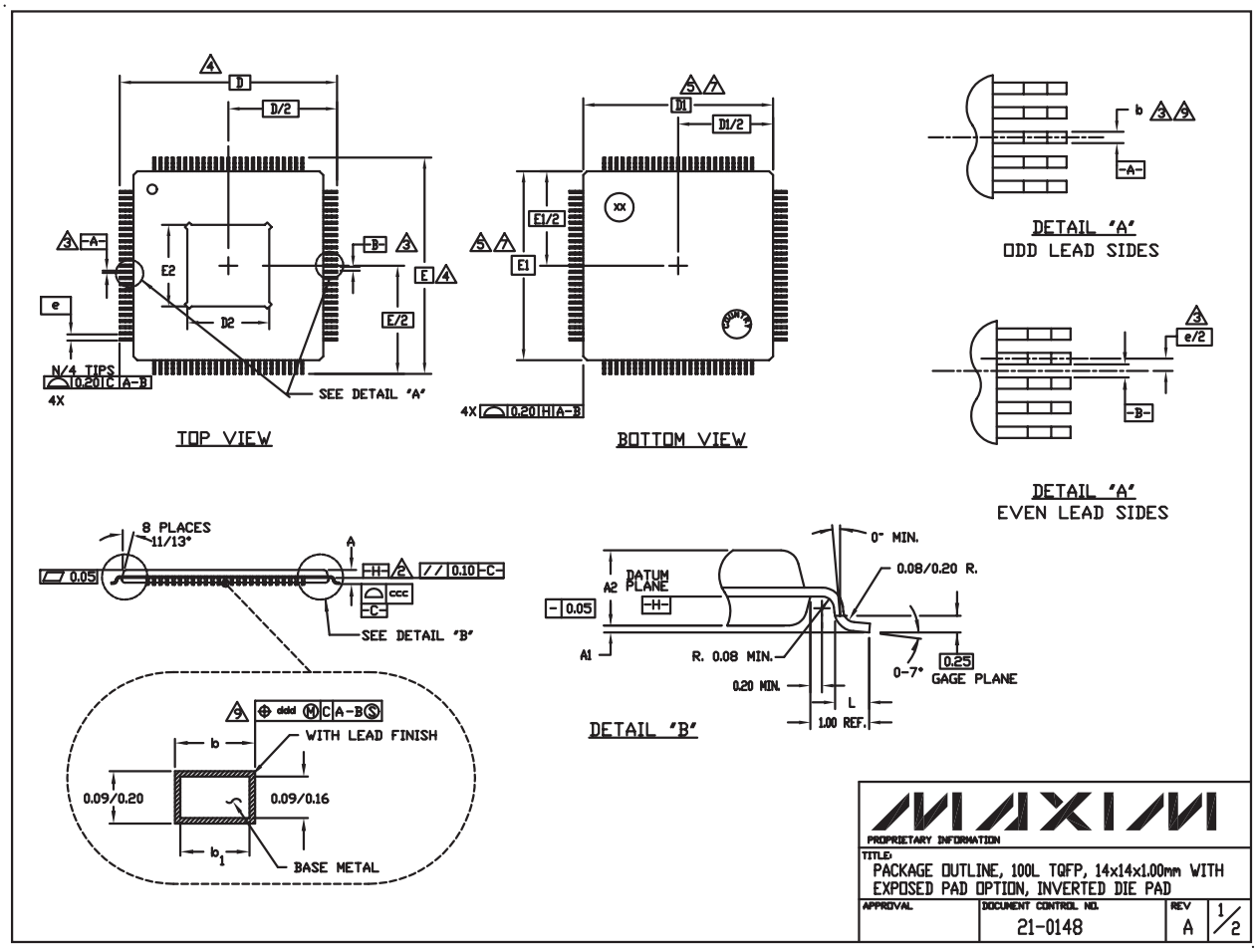


双通道、低功耗、1200Mbps ATE 驱动器/比较器，带有35mA负载

封装信息

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages.)

TQFP 14x14.EPS



封装信息（续）

(本数据资料提供的封装图可能不是最近的规格，如需最近的封装外型信息，请查询 www.maxim-ic.com.cn/packages。)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUM A-B TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.
9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.50mm.
12. THIS OUTLINE IS NOT YET JEDEC REGISTERED.
13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
14. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.
15. METAL AREA OF EXPOSED DIE PAD SHALL BE WITHIN 0.30mm OF THE NOMINAL DIE PAD SIZE.
16. COUNTRY OF ORIGIN MUST BE MARKED ON THE PACKAGE.

SYMBOL	COMMON DIMENSIONS			
	ALL DIMENSIONS ARE IN MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	1.20	
A_1	0.05	—	0.15	13
A_2	0.95	1.00	1.05	
D	16.00 BSC.			4
D_1	14.00 BSC.			7,8
E	16.00 BSC.			4
E_1	14.00 BSC.			7,8
L	0.45	0.60	0.75	
N	100			
e	0.50 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	—	—	0.08	
ddd	—	—	0.08	

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG. CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C100E-8R	7.70	8.00	8.30	7.70	8.00	8.30

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 100L TQFP, 14x14x1.00mm WITH EXPOSED PAD OPTION, INVERTED DIE PAD
APPROVAL | DOCUMENT CONTROL NO. 21-0148 | REV A | 2/2

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