19-0383; Rev 0; 7/05

MAXIM

四通道、低功耗、1200Mbps ATE驱动器

概述

MAX9977为四通道、低功耗、高速、引脚电子驱动器，每个通道含有一个三电平引脚驱动器。驱动器具有宽工作电压范围和高速工作特性，提供高阻和有源端接(第3级驱动)模式，且在低电源电压下仍可保持高线性度。

MAX9977提供高速、差分控制输入，内部50Ω (100Ω LVDS)端接电阻能够兼容于1.8V和3.5V端接的0.4V_{P-P} CML逻辑，减少了电路板所需的分立元件。MAX9977AD无内部端接。

通过3线、兼容于低压CMOS逻辑电平的串口编程设置MAX9977的低泄漏、三态/端接工作模式。

MAX9977的工作电压范围为-1.5V至+6.5V (请联系工厂，了解其它工作范围)，每通道的最大功耗仅为0.8W。该器件采用100引脚、14mm x 14mm x 0.1mm、引脚间距0.5mm的TQFP封装。封装顶部带有8mm x 8mm裸焊盘，提高了散热效率。该器件工作在+60°C至+100°C的器件管芯温度，并具有管芯温度监视输出。

应用

中等性能的片上系统ATE和存储器应用

特性

- ♦ 低功耗：0.8W/通道
- ♦ 高速：3V_{P-P}时，1200Mbps；1V_{P-P}时，1800Mbps
- ♦ 低定时偏差
- ♦ -1.5V至+6.5V宽工作电压范围
- ♦ 便于与大多数逻辑电平接口
- ♦ 有源端接(第3级驱动)
- ♦ 控制输入端有50Ω内部端接电阻
- ♦ 低增益误差和失调误差
- ♦ 与MAX9963和MAX9965四通道驱动器引脚兼容

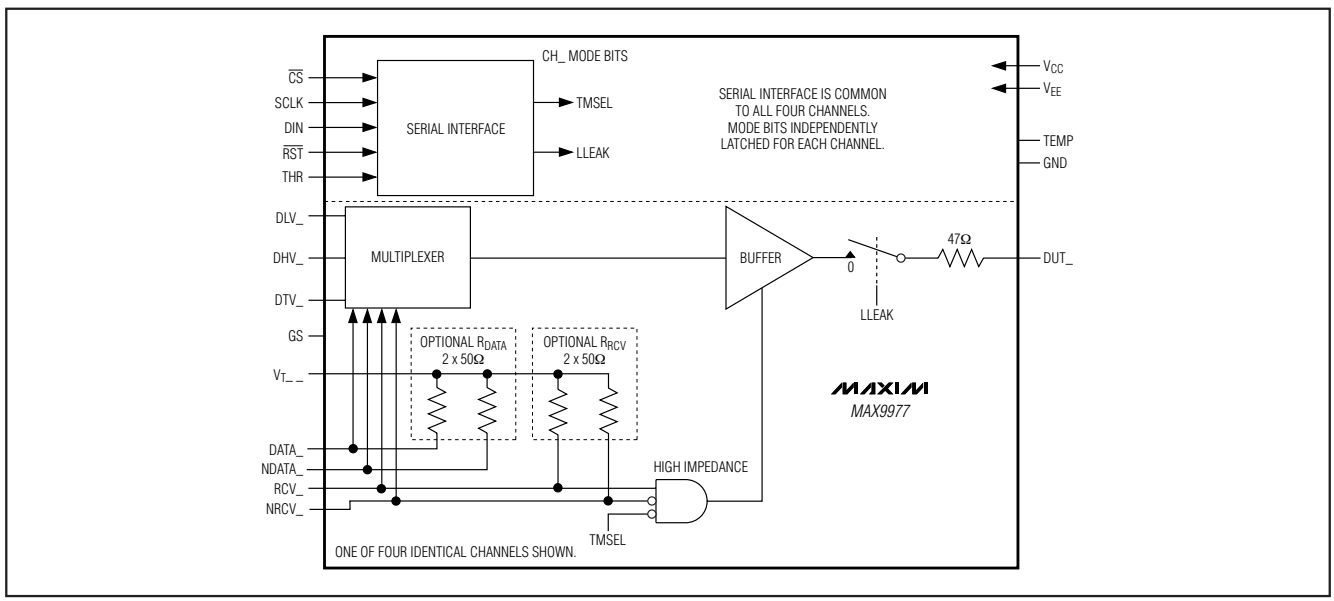
定购信息

PART	TEMP RANGE	PIN-PACKAGE	EXPOSED PAD VARIATION CODE
MAX9977AKCCQ	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977AKCCQ+	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977ADCCQ*	0°C to +70°C	100 TQFP-IDP**	C100E-8R
MAX9977ADCCQ+*	0°C to +70°C	100 TQFP-IDP**	C100E-8R

*未来产品—供货信息请与厂商联系。
**IDP = 倒置管芯焊盘。
+表示无铅封装。

引脚配置和选型指南在数据资料的最后给出。

功能框图



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11V
V_{EE} to GND.....-5.75V to +0.3V
V_{CC} - V_{EE}.....-0.3V to +16.75V
DUT_ to GND.....-2.75V to +7.5V
DATA_, NDATA_, RCV_, NRCV_ to GND .....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_ .....±1.5V
V_T12, V_T34 to GND.....-2.5V to +5V
DATA_, NDATA_, RCV_, NRCV_ to V_T12 or V_T34 .....±2V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$ to GND .....-1V to +5V
DHV_, DLV_, DTV_ to GND .....-2.5V to +7.5V
DHV_ to DLV_ .....±10V
DHV_ to DTV_ .....±10V
DLV_ to DTV_.....±10V
GS to GND .....±1V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
TEMP Current.....-0.5mA to +20mA
DUT_ Short Circuit to -1.5V to +6.5V.....Continuous
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP (derate 167mW/°C above +70°C) 13.3W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply	V_{CC}		9.5	9.75	10.5	V
Negative Supply	V_{EE}		-5.25	-4.75	-4.50	V
Positive Supply Current (Note 2)	I_{CC}	Drivers active		192	215	mA
		Drivers in high impedance		175	196	
Negative Supply Current (Note 2)	I_{EE}	Drivers active		-224	-251	mA
		Drivers in high impedance		-207	-232	
Power Dissipation (Note 2)	P_D	Drivers active		3.0	3.3	W
		Drivers in high impedance		2.7	3.1	
DUT_ CHARACTERISTICS						
Operating Voltage Range	V_{DUT}	(Note 3)	-1.5		+6.5	V
Leakage Current in High-Impedance Mode	I_{DUT}	LLEAK = 0; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V			±3	µA
Leakage Current in Low-Leakage Mode		LLEAK = 1; $V_{DUT\_}$ = -1.5V, 0, +3V, +6.5V		±5	±50	nA
Combined Capacitance	C_{DUT}	Driver in term mode (DUT_ = DTV_)		2	5	pF
		Driver in high-impedance mode		4	6	
Low-Leakage Enable Time		(Notes 4, 5)		20		µs
Low-Leakage Disable Time		(Notes 5, 6)		0.1		µs
Low-Leakage Recovery		Time to return to the specified maximum leakage after a 3V, 4V/ns step at DUT_ (Notes 5, 6)		5		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL AND LEVELS INPUTS						
LEVEL PROGRAMMING INPUTS (DHV_, DLV_, DTV_)						
Input Bias Current	I_{BIAS}				±25	µA
Settling Time		To 0.1% of full-scale change		1		µs
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)						
Input High Voltage	V_{IHD}		0		3.5	V
Input Low Voltage	V_{ILD}		-0.2		+3.2	V
Differential Input Voltage	V_{DIFF}	Between differential inputs	±0.15		±1.00	V
		Between a differential input and its termination voltage			±1.9	
Input Termination Voltage	$V_{T\_\_}$		0		+3.5	V
Input Termination Resistor		Between signal and corresponding termination voltage input	47.5	50	52.5	Ω
SINGLE-ENDED CONTROL INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$)						
Internal Threshold Reference	V_{THRINT}		1.05	1.25	1.45	V
Internal Reference Output Resistance	R_O			20		kΩ
External Threshold Reference	V_{THR}		0.43		1.73	V
Input High Voltage	V_{IH}		V_{THR} + 0.2		3.5	V
Input Low Voltage	V_{IL}		-0.1		V_{THR} - 0.2	V
Input Bias Current	I_B				±25	µA
SERIAL INTERFACE TIMING (Figure 4)						
SCLK Frequency	f_{SCLK}				50	MHz
SCLK Pulse-Width High	t_{CH}		8			ns
SCLK Pulse-Width Low	t_{CL}		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		3.5			ns
DIN to SCLK High Setup	t_{DS}		3.5			ns
DIN to SCLK High Hold	t_{DH}		3.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		20			ns
TEMPERATURE MONITOR (TEMP)						
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ		3.33		V
Temperature Coefficient				+10		mV/°C
Output Resistance				20		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVERS (Note 7)						
DC OUTPUT CHARACTERISTICS (R_L ≥ 10MΩ)						
DHV_, DLV_, DTV_ Output Offset Voltage	V_{OS}	At DUT_ with $V_{DHV\_}$, $V_{DTV\_}$, $V_{DLV\_}$ independently tested at +1.5V			±15	mV
Output Offset Voltage Due to Ground Sense	V_{GSOS}	V_{GS} = +100mV, $V_{DHV\_}$ = 6.5V + 100mV		±2		mV
		V_{GS} = -100mV, $V_{DLV\_}$ = -1.5V - 100mV		±2		
DHV_, DLV_, DTV_ Output Offset Temperature Coefficient				+200		µV/°C
DHV_, DLV_, DTV_ Gain	A_V	Measured with $V_{DHV\_}$, $V_{DLV\_}$, and $V_{DTV\_}$ at 0 and 4.5V	0.997	1.00	1.003	V/V
DHV_, DLV_, DTV_ Gain Temperature Coefficient				-50		ppm/°C
Linearity Error		$V_{DUT\_}$ = 1.5V, 3V (Note 8)			±5	mV
		Full range (Notes 8, 9)			±15	
DHV_ to DLV_ Crosstalk		$V_{DLV\_}$ = 0; $V_{DHV\_}$ = 200mV, 6.5V			±2	mV
DLV_ to DHV_ Crosstalk		$V_{DHV\_}$ = 5V; $V_{DLV\_}$ = -1.5V, +4.8V			±2	mV
DTV_ to DLV_ and DHV_ Crosstalk		$V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0; $V_{DTV\_}$ = -1.5V, +6.5V			±2	mV
DHV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DLV\_}$ = 0; $V_{DHV\_}$ = 1.6V, 3V			±2	mV
DLV_ to DTV_ Crosstalk		$V_{DTV\_}$ = 1.5V; $V_{DHV\_}$ = 3V; $V_{DLV\_}$ = 0, 1.4V			±2	mV
DHV_, DTV_, DLV_ DC Power-Supply Rejection Ratio	PSRR	(Note 10)			±18	mV/V
Maximum DC Drive Current	$I_{DUT\_}$		±40		±80	mA
DC Output Resistance	$R_{DUT\_}$	$I_{DUT\_}$ = ±30mA (Note 11)	46	47	48	Ω
DC Output Resistance Variation	$\Delta R_{DUT\_}$	$I_{DUT\_}$ = ±1mA, ±8mA		0.5	1	Ω
		$I_{DUT\_}$ = ±1mA, ±8mA, ±15mA, ±40mA		0.75	1.5	
DYNAMIC OUTPUT CHARACTERISTICS (Z_L = 50Ω)						
AC Drive Current			±80			mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		15	22	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		110	130	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		210	370	
Drive-Mode Undershoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		4	11	mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		20	65	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V		30	185	
Term-Mode Spike		$V_{DHV\_}$ = $V_{DTV\_}$ = 1V, $V_{DLV\_}$ = 0		180	250	mV
		$V_{DLV\_}$ = $V_{DTV\_}$ = 0, $V_{DHV\_}$ = 1V		180	250	
High-Impedance-Mode Spike		$V_{DLV\_}$ = -1.0V, $V_{DHV\_}$ = 0		100		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V		100		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Settling Time to within 25mV		3V step (Note 12)		4		ns
Settling Time to within 5mV		3V step (Note 12)		40		ns
TIMING CHARACTERISTICS (Z_L = 50Ω) (Note 13)						
Prop Delay, Data to Output	t_{PDD}		1.2	1.5	1.9	ns
Prop Delay Match, t_{LH} vs. t_{HL}		$3V_{P-P}$		±40	±100	ps
Prop Delay Match, Drivers within Package		(Note 14)		40		ps
Prop-Delay Temperature Coefficient				+1.6		ps/°C
Prop Delay Change vs. Pulse Width		$0.2V_{P-P}$, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width		±25	±50	ps
		$1V_{P-P}$, 40MHz, 0.6ns to 24.4ns pulse width, relative to 12.5ns pulse width		±25	±50	
		$2V_{P-P}$, 40MHz, 0.75ns to 24.25ns pulse width, relative to 12.5ns pulse width		±30	±55	
		$3V_{P-P}$, 40MHz, 0.9ns to 24.1ns pulse width, relative to 12.5ns pulse width		±35	±60	
		$5V_{P-P}$, Z_L = 500Ω, 40MHz, 1.4ns to 23.6ns pulse width, relative to 12.5ns pulse width		±100		
Prop Delay Change vs. Common-Mode Voltage		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V		50	75	ps
Prop Delay, Drive to High Impedance	t_{PDDZ}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	1.6	2.1	2.6	ns
Prop Delay, High Impedance to Drive	t_{PDZD}	$V_{DHV\_}$ = 1.0V, $V_{DLV\_}$ = -1.0V, $V_{DTV\_}$ = 0	2.6	3.2	3.9	ns
Prop Delay Match, t_{PDDZ} vs. t_{PDZD}			-1.5	-1.1	-0.7	ns
Prop Delay Match, t_{PDDZ} vs. t_{LH}			0.2	0.6	1.0	ns
Prop Delay, Drive to Term	t_{PDDT}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.3	1.8	2.3	ns
Prop Delay, Term to Drive	t_{PDTD}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V	1.6	2.1	2.7	ns
Prop Delay Match, t_{PDDT} vs. t_{PDTD}			-0.7	-0.3	-0.1	ns
Prop Delay Match, t_{PDDT} vs. t_{LH}			-0.1	+0.3	+0.7	ns
DYNAMIC PERFORMANCE (Z_L = 50Ω)						
Rise and Fall Time	t_R, t_F	$0.2V_{P-P}$, 10% to 90%	260	310	360	ps
		$1V_{P-P}$, 10% to 90%	330	390	450	
		$2V_{P-P}$, 10% to 90%	430	500	570	
		$3V_{P-P}$, 10% to 90%	500	650	750	
		$5V_{P-P}$, Z_L = 500Ω, 10% to 90%	800	1000	1200	
Rise and Fall Time Match	t_R vs. t_F	$3V_{P-P}$, 10% to 90%		±50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, V_T12 = V_T34 = 1.8V, T_J = +85°C, unless otherwise noted. All temperature coefficients are measured at T_J = +60°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Pulse Width (Note 15)		$0.2V_{P-P}$		550		ps
		$1V_{P-P}$		550	630	
		$2V_{P-P}$		650	750	
		$3V_{P-P}$		850	1000	
		$5V_{P-P}$, Z_L = 500Ω		1300		
Data Rate (Note 16)		$0.2V_{P-P}$		1800		Mbps
		$1V_{P-P}$		1800		
		$2V_{P-P}$		1500		
		$3V_{P-P}$		1200		
		$5V_{P-P}$, Z_L = 500Ω		800		
Dynamic Crosstalk		(Note 17)		15		mV_{P-P}
Rise and Fall Time, Drive to Term	t_{DTR}, t_{DTF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1a (Note 18)	0.6	1.0	1.3	ns
Rise and Fall Time, Term to Drive	t_{TDR}, t_{TDF}	$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, 10% to 90%, Figure 1b (Note 18)	0.6	1.0	1.3	ns
GROUND SENSE						
GS Voltage Range	V_{GS}		±250			mV
GS Input Bias Current		V_{GS} = 0			±25	µA

Note 1: Unless otherwise specified, all minimum and maximum DC and AC driver 3V rise and fall time test limits are 100% tested at production. All other test limits are guaranteed by design. All tests are performed at nominal supply voltages, unless otherwise noted.

Note 2: Total is for a quad device and is specified at the worst-case setting. The supply currents are measured with typical supply voltages.

Note 3: Externally forced voltages may exceed this range provided that the Absolute Maximum Ratings are not exceeded.

Note 4: Transition time from LLEAK being asserted to leakage current dropping below specified limits.

Note 5: Based on simulation results only.

Note 6: Transition time from LLEAK being deasserted to output returning to normal operating mode.

Note 7: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 8: Specifications measured at the end points of the full range. Full range is -1.3V ≤ $V_{DHV\_}$ ≤ +6.5V, -1.5V ≤ $V_{DLV\_}$ ≤ +6.3V, -1.5V ≤ $V_{DTV\_}$ ≤ +6.5V.

Note 9: Relative to straight line between 0 and 4.5V.

Note 10: Change in offset voltage with power supplies independently set to their minimum and maximum values.

Note 11: Nominal target value is 47Ω. Contact factory for alternate trim selections within the 45Ω to 51Ω range.

Note 12: Measured from the crossing point of DATA_ inputs to the settling of the driver output.

Note 13: Prop delays are measured from the crossing point of the differential input signals to the 50% point of the expected output swing. Rise time of the differential inputs DATA_ and RCV_ are 250ps (10% to 90%).

Note 14: Rising edge to rising edge or falling edge to falling edge.

Note 15: Specified amplitude is programmed. At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 16: Specified amplitude is programmed. Maximum data rate is specified in transitions per second. A square wave that reaches at least 90% of its programmed amplitude may be generated at one-half of this frequency.

Note 17: Crosstalk from one driver to any other. Aggressor channel is driving $3V_{P-P}$ into a 50Ω load. Victim channel is in term mode with $V_{DTV\_}$ = +1.5V.

Note 18: Indicative of switching speed from DHV_ or DLV_ to DTV_ and DTV_ to DHV_ or DLV_ when $V_{DLV\_}$ < $V_{DTV\_}$ < $V_{DHV\_}$. If $V_{DTV\_}$ < $V_{DLV\_}$ or $V_{DTV\_}$ > $V_{DHV\_}$, switching speed is degraded by a factor of approximately 3.

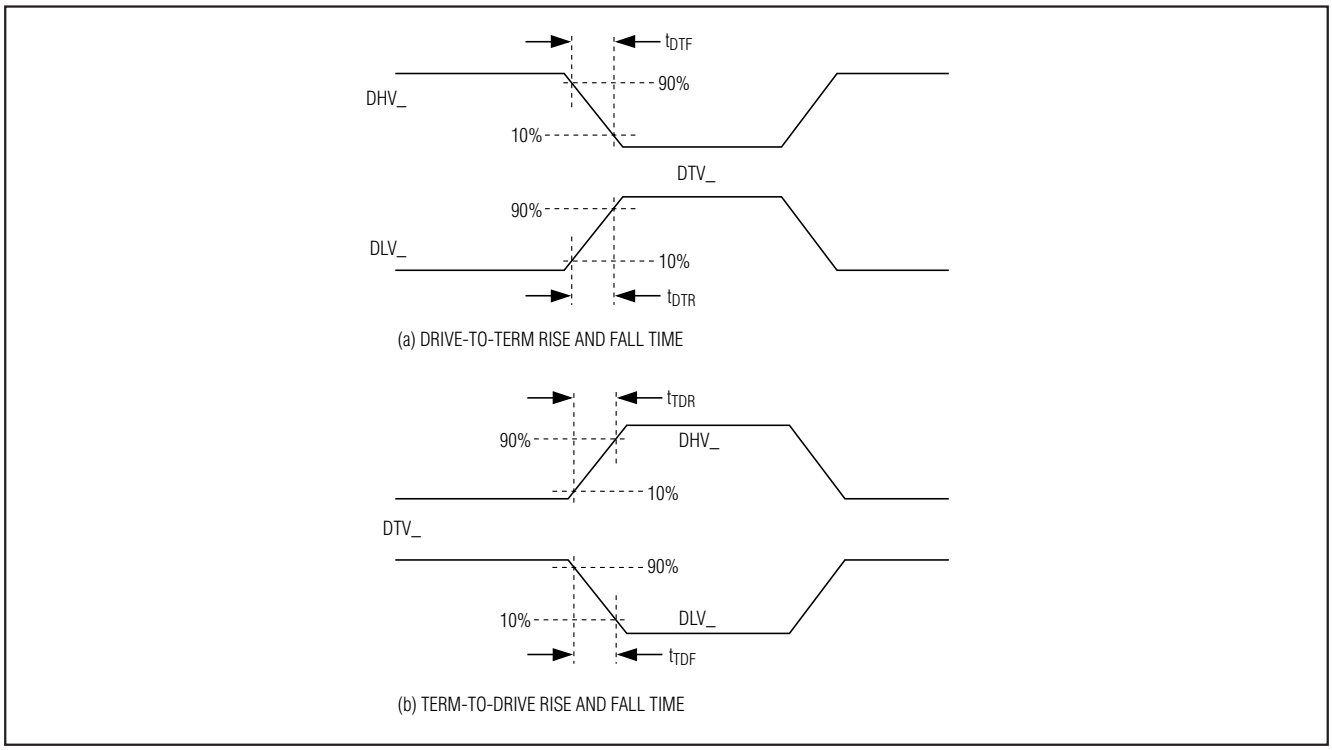
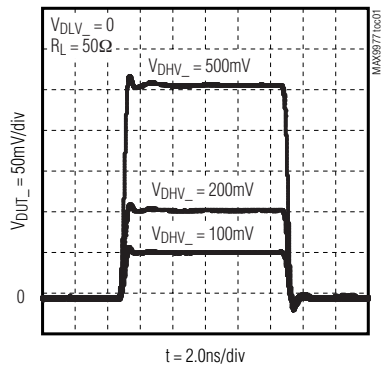


图1. 驱动至终端、终端至驱动的上升和下降时间

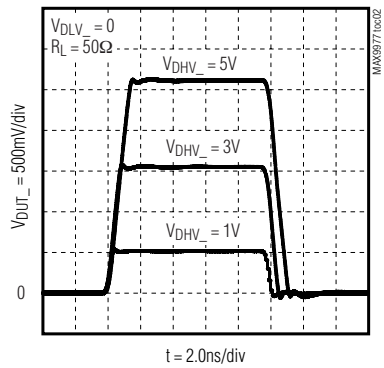
典型工作特性

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

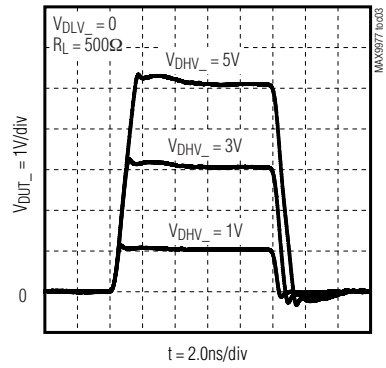
DRIVER SMALL-SIGNAL RESPONSE



DRIVER LARGE-SIGNAL RESPONSE



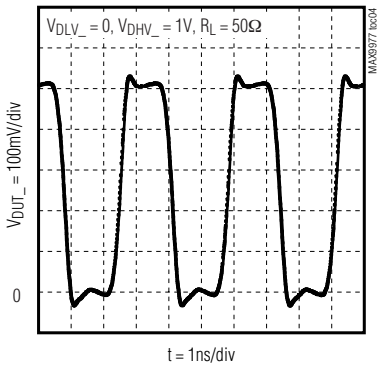
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



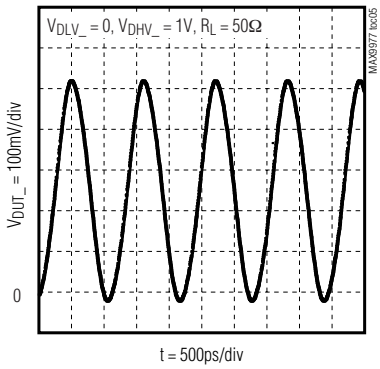
典型工作特性(续)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

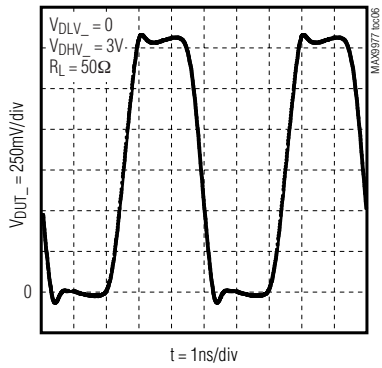
DRIVER 1V, 600Mbps SIGNAL RESPONSE



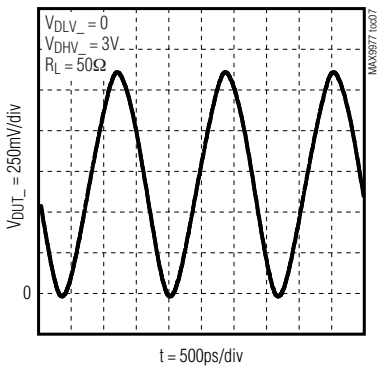
DRIVER 1V, 1800Mbps SIGNAL RESPONSE



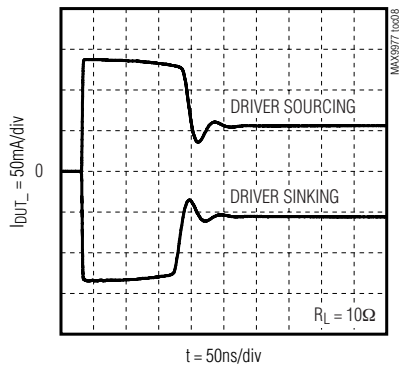
DRIVER 3V, 400Mbps SIGNAL RESPONSE



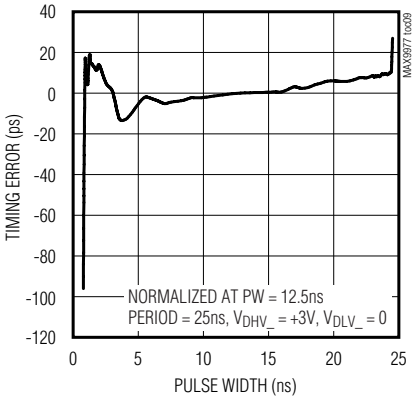
DRIVER 3V, 1200Mbps SIGNAL RESPONSE



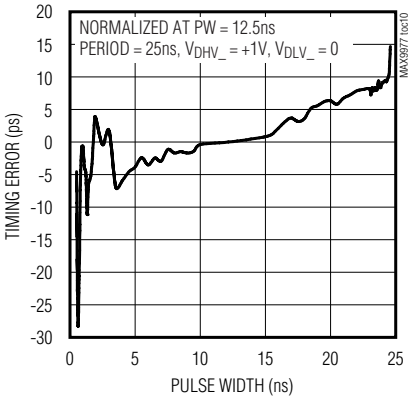
DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



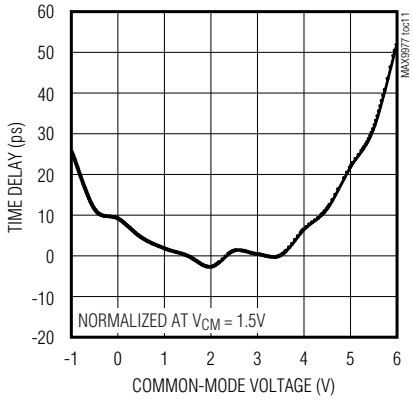
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



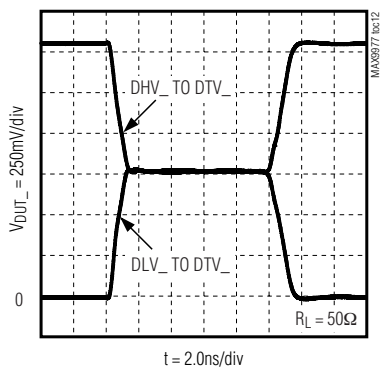
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



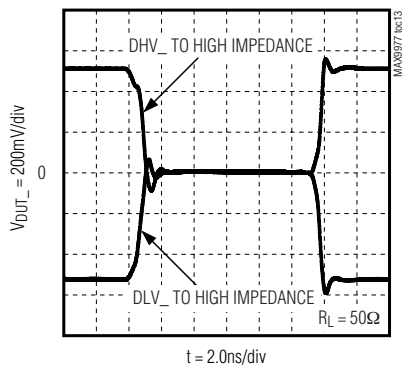
DRIVE TO TERM TRANSITION



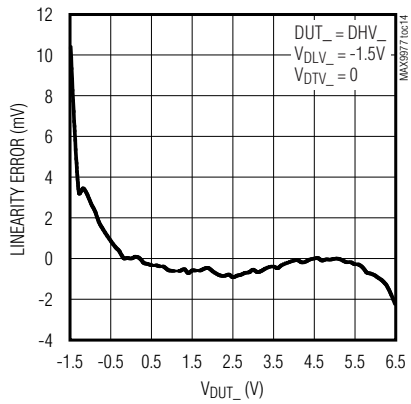
典型工作特性(续)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

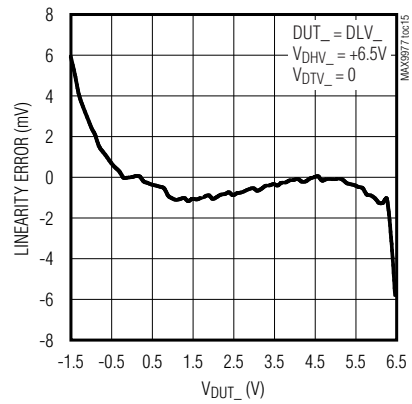
DRIVE TO HIGH-IMPEDANCE TRANSITION



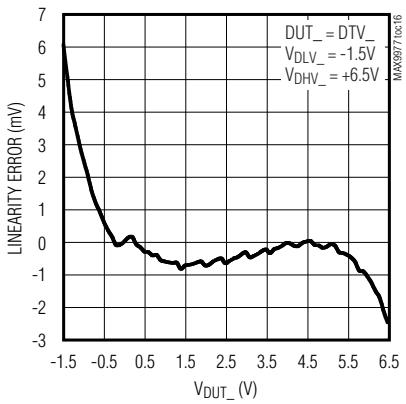
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



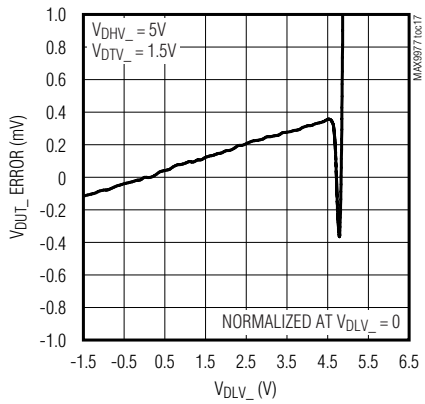
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



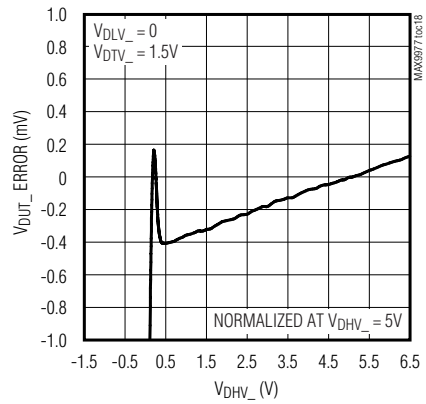
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



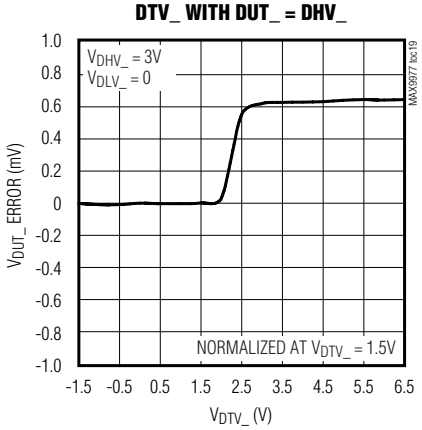
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DHV_



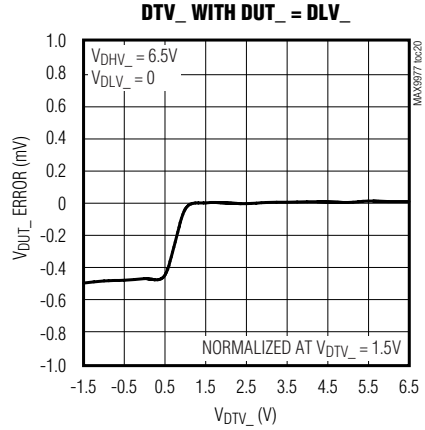
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DLV_



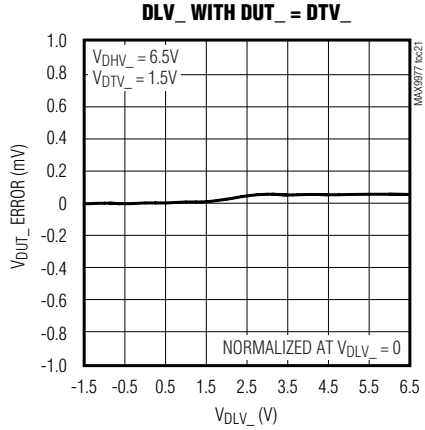
CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DHV_



CROSSTALK TO DUT_ FROM DTV_ WITH DUT_ = DLV_



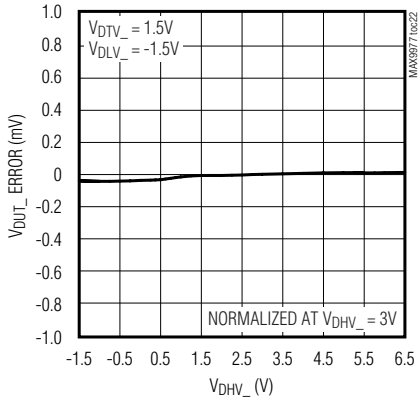
CROSSTALK TO DUT_ FROM DLV_ WITH DUT_ = DTV_



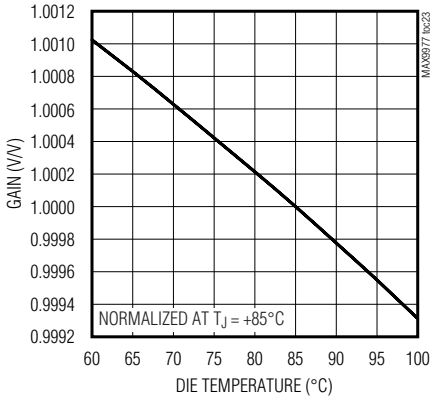
典型工作特性(续)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

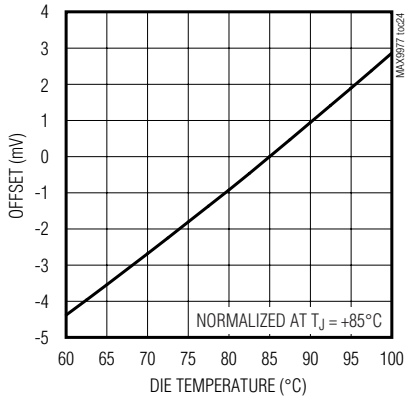
CROSSTALK TO DUT_ FROM DHV_ WITH DUT_ = DTV_



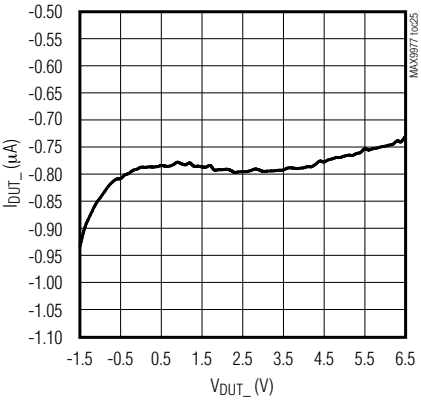
DRIVER GAIN vs. TEMPERATURE



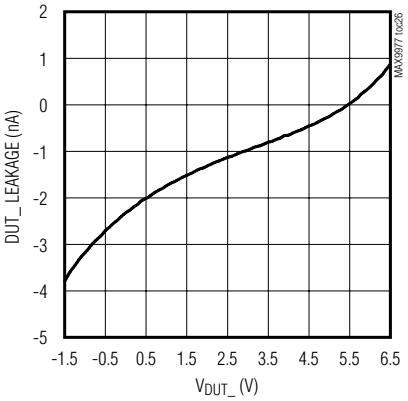
DRIVER OFFSET vs. TEMPERATURE



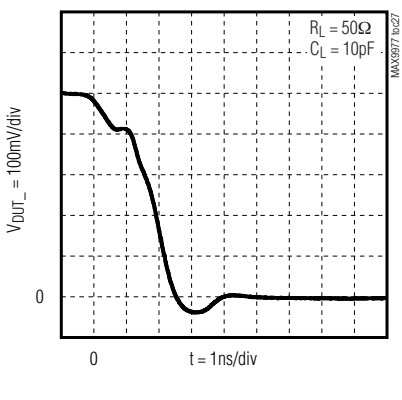
HIGH-IMPEDANCE CURRENT vs. DUT_ VOLTAGE



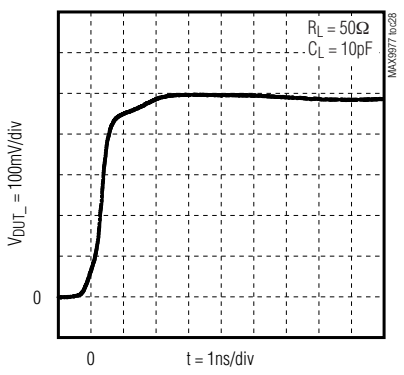
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



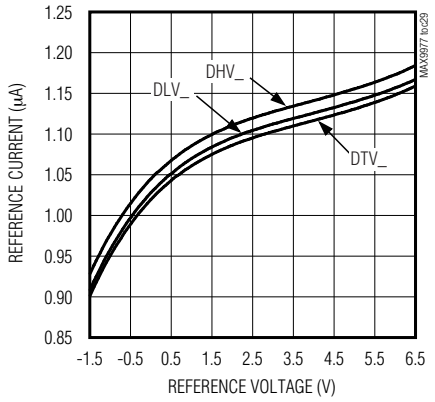
DRIVE 1V TO LOW-LEAKAGE TRANSITION



LOW-LEAKAGE TO DRIVE 1V TRANSITION



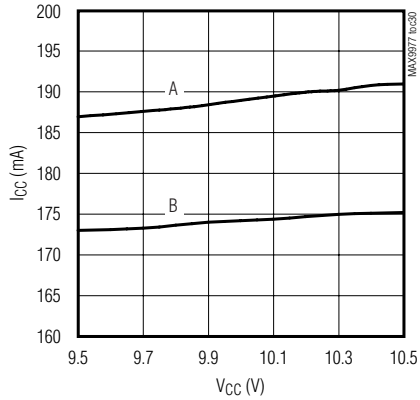
DRIVER REFERENCE CURRENT vs. DRIVER REFERENCE VOLTAGE



典型工作特性(续)

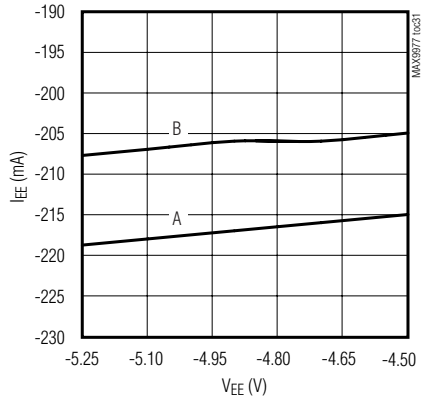
(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{GS} = 0, T_J = +85°C, unless otherwise noted.)

SUPPLY CURRENT I_{CC} vs. VOLTAGE CURRENT V_{CC}



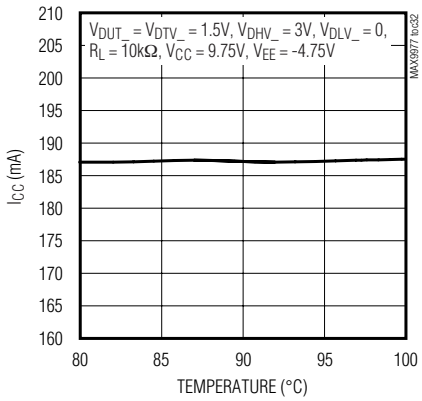
A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$, $R_L = 10k\Omega$, $V_{EE} = -4.75V$
B: SAME AS A EXCEPT DRIVER IN HIGH-IMPEDANCE MODE

SUPPLY CURRENT I_{EE} vs. VOLTAGE CURRENT V_{EE}

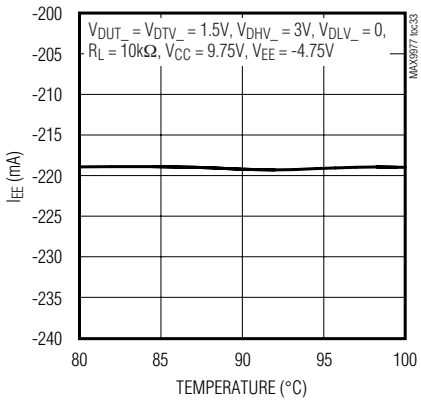


A: $V_{DUT\_} = V_{DTV\_} = 1.5V$, $V_{DHV\_} = 3V$, $V_{DLV\_} = 0$, $R_L = 10k\Omega$, $V_{CC} = 9.75V$
B: SAME AS A EXCEPT DRIVER IN HIGH-IMPEDANCE MODE

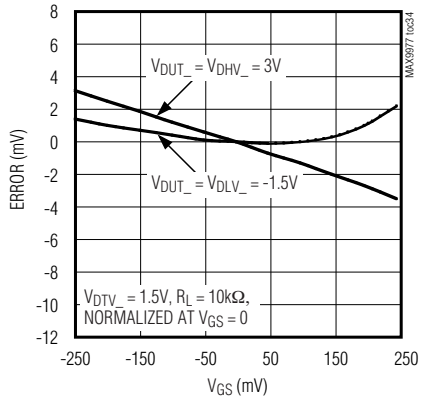
SUPPLY CURRENT I_{CC} vs. TEMPERATURE



SUPPLY CURRENT I_{EE} vs. TEMPERATURE



DRIVER OUTPUT-VOLTAGE ERROR vs. GROUND-SENSE VOLTAGE



四通道、低功耗、1200Mbps ATE驱动器

引脚说明

引脚	名称	功能
1	$V_{T}34$	通道3/4端接电压差分输入端，DATA3、NDATA3、RCV3、NRCV3、DATA4、NDATA4、RCV4和NRCV4，请参考*功能框图*。
2	DATA4	通道4多路复用器控制输入。通过差分控制输入DATA4和NDATA4，选择DHV4或DLV4作为驱动器4的输入。DATA4高于NDATA4时，选择DHV4；NDATA4高于DATA4时，选择DLV4。参见表1。
3	NDATA4	
4	RCV4	通道4多路复用器控制输入。差分控制输入RCV4和NRCV4，可将通道4设置为接收模式。RCV4高于NRCV4时，通道4进入接收模式；NRCV4高于RCV4时，通道4进入驱动模式。参见表1。
5	NRCV4	
6	DATA3	通道3多路复用器控制输入。通过差分控制输入DATA3和NDATA3，选择DHV3或DLV3作为驱动器3的输入。DATA3高于NDATA3时，选择DHV3；NDATA3高于DATA3时，选择DLV3。参见表1。
7	NDATA3	
8	RCV3	通道3多路复用器控制输入。差分控制输入RCV3和NRCV3，可将通道3设置为接收模式。RCV3高于NRCV3时，通道3进入接收模式；NRCV3高于RCV3时，通道3进入驱动模式。参见表1。
9	NRCV3	
10, 27, 54, 55, 60, 61, 65, 66, 71, 72, 99	V_{EE}	电源负端输入。
11, 28, 51, 56, 62, 64, 70, 75, 98	GND	接地端。
12	$\overline{RST}$	复位输入，串行寄存器异步复位输入，$\overline{RST}$低电平有效，参见图3。
13	$\overline{CS}$	片选输入，串口使能输入，$\overline{CS}$低电平有效。
14	SCLK	串行时钟输入，串口时钟。
15	DIN	数据输入，串口数据输入。
16, 26, 52, 58, 68, 74, 100	V_{CC}	电源正端输入。
17	NRCV2	通道2多路复用器控制输入。差分控制输入RCV2和NRCV2，可将通道2设置为接收模式。RCV2高于NRCV2时，通道2进入接收模式；NRCV2高于RCV2时，通道2进入驱动模式。参见表1。
18	RCV2	
19	NDATA2	通道2多路复用器控制输入。通过差分控制输入DATA2和NDATA2，选择DHV2或DLV2作为驱动器2的输入。DATA2高于NDATA2时，选择DHV2；NDATA2高于DATA2时，选择DLV2。参见表1。
20	DATA2	
21	NRCV1	通道1多路复用器控制输入，差分控制输入RCV1和NRCV1，可将通道1设置为接收模式。RCV1高于NRCV1时，通道1进入接收模式；NRCV1高于RCV1时，通道1进入驱动模式。参见表1。
22	RCV1	
23	NDATA1	通道1多路复用器控制输入。通过差分控制输入DATA1和NDATA1，选择DHV1或DLV1作为驱动器1的输入。DATA1高于NDATA1时，选择DHV1；NDATA1高于DATA1时，选择DLV1。参见表1。
24	DATA1	
25	$V_{T}12$	通道1/2端接电压差分输入端，DATA1、NDATA1、RCV1、NRCV1、DATA2、NDATA2、RCV2和NRCV2。参见*功能框图*。
29–38, 43, 44, 45, 49, 50, 57, 69, 76, 77, 81, 82, 83, 88–97	N.C.	没有连接，不要连接该引脚。

引脚说明(续)

引脚	名称	功能
39	DHV2	通道2驱动器高压输入。
40	DLV2	通道2驱动器低压输入。
41	DTV2	通道2驱动器端接电压输入。
42	GS	所有通道的地检测输入端。
46	DHV1	通道1驱动器高压输入。
47	DLV1	通道1驱动器低压输入。
48	DTV1	通道1驱动器端接电压输入。
53	DUT1	通道1待测器件输入/输出。
59	DUT2	通道2待测器件输入/输出。
63	TEMP	温度监视输出，每个器件一个输出。
67	DUT3	通道3待测器件输入/输出。
73	DUT4	通道4待测器件输入/输出。
78	DTV4	通道4驱动器端接电压输入。
79	DLV4	通道4驱动器低压输入。
80	DHV4	通道4驱动器高压输入。
84	THR	所有通道的单端逻辑门限基准。
85	DTV3	通道3驱动器端接电压输入。
86	DLV3	通道3驱动器低压输入。
87	DHV3	通道3驱动器高压输入。

详细说明

MAX9977低功耗、高速、引脚电子IC包括四个三电平引脚驱动器。该驱动器可工作在-1.5V至+6.5V范围，具有高速工作特性，它包括高阻和有源端接(第3级驱动)模式，在低电源电压下仍可保持高线性度。

高速输入端口具有可选则的内部电阻，使器件能够兼容于CML接口，并减少了电路板所需的分立元件。将端接电压输入V_T12和V_T34连接到一个适当电压，用于驱动电路端接多路复用器的控制输入(参见*功能框图*)。

通过3线、兼容于低压CMOS逻辑的串口编程设置MAX9977的低泄漏、三态/端接工作模式。

与MAX9963和MAX9965的兼容性

从MAX9963或MAX9965升级到MAX9977，需采取以下步骤：

1) MAX9977的GS对应MAX9963/MAX9965的CHV2。将CHV2设置为0V。
2) MAX9977的THR对应MAX9963/MAX9965的CHV3。如果CHV3由一个以地检测端为参考的DAC控制，则重新配置该输入，使其不受地检测端变化的影响。
3) MAX9977AK的DRV_和RCV_输入带有两个内部端接电阻的中心抽头V_T12和V_T34，对应MAX9963/MAX9965的比较器输出电阻端接点V_{CCO12}和V_{CCO34}。适当偏置这些端接点。

输出驱动器

驱动器输入是一个高速多路复用器，可以选择DHV_、DLV_或DTV_三个电压之一作为输入。选择开关由高速输入DATA_、RCV_以及模式控制位TMSEL (表1)控制。

DUT_可在缓冲器输出和高阻模式之间高速切换，也可配置为低泄漏模式(见图2和表1)。高速输入RCV_和模式控制位TMSEL、LLEAK控制这一切换。高阻模式下，DUT_的偏置电流在-1.5V至+6.5V电压范围内小于3µA，而节点仍然能够跟踪高速信号。低泄漏模式下，DUT_的偏置电流进一步降至50nA以下，信号跟踪能力变慢。详细内容，请参考*低泄漏模式，LLEAK*部分。

驱动器输出阻抗标称值为47Ω。若需45Ω至51Ω范围内的不同电阻，请与厂商联系。

四通道、低功耗、1200Mbps ATE驱动器

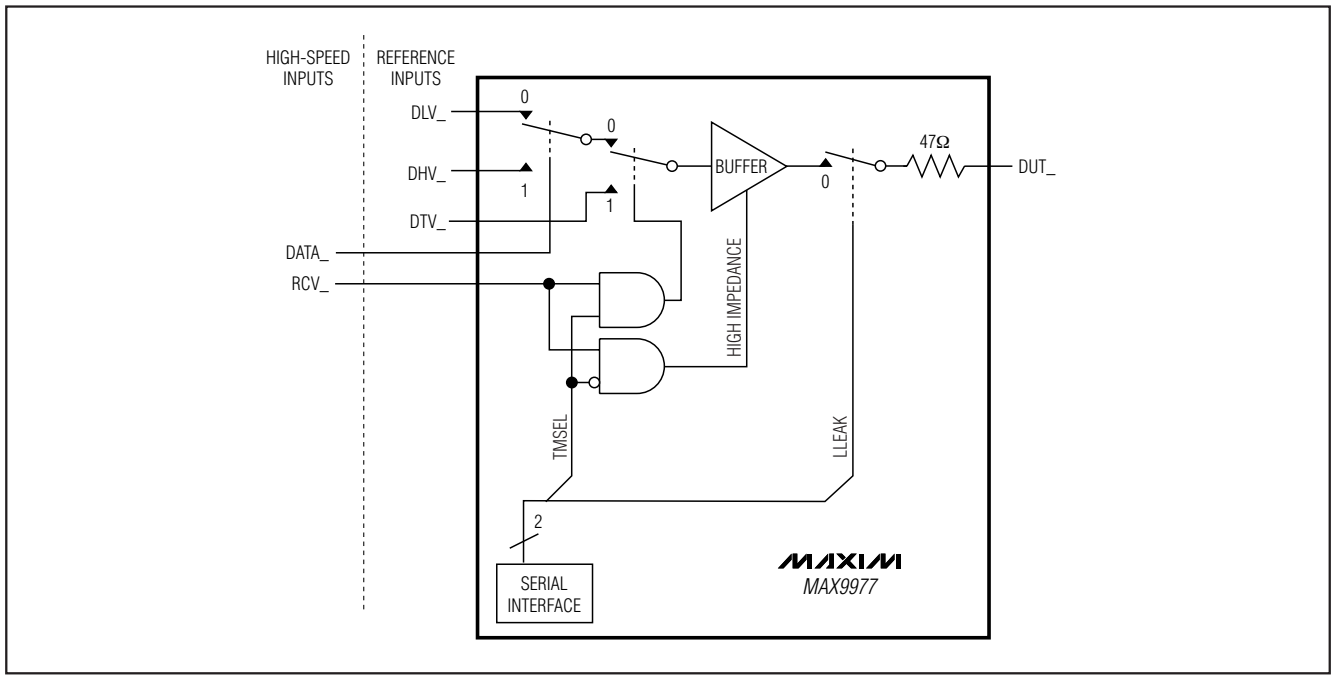


图2. 简化的驱动器通道

表1. 驱动器逻辑

EXTERNAL CONNECTIONS		INTERNAL CONTROL REGISTER		DRIVER OUTPUT
DATA	RCV	TMSEL	LLEAK	
1	0	X	0	Drive to DHV_
0	0	X	0	Drive to DLV_
X	1	1	0	Drive to DTV_ (term mode)
X	1	0	0	High-impedance mode (high-Z)
X	X	X	1	Low-leakage mode

串口和器件控制

CMOS兼容串行接口控制MAX9977的工作模式(图3和表2)。如图4所示，控制数据进入一个8位移位寄存器(MSB在前)，并在$\overline{CS}$变为高电平时锁存该数据。锁存器为MAX9977的每个通道提供两个控制位。来自移位寄存器的数据装入其中一个锁存器或所有四个锁存器，具体由D4和D7位决定。控制位同外部输入DATA_和RCV_一起管理每个通道的功能。$\overline{RST}$将四个通道均设置为LLEAK = 1，强制它们进入低泄漏模式。其它位均不受影响。上电时，在V_{CC}和V_{EE}稳定之前，使$\overline{RST}$保持低电平。

模拟控制输入THR用于设置输入逻辑电平的门限，允许与低至0.9V的CMOS逻辑电平接口。THR浮空时，会产生来自内部基准的1.25V门限电压，并与2.5V至3.3V逻辑电平兼容。

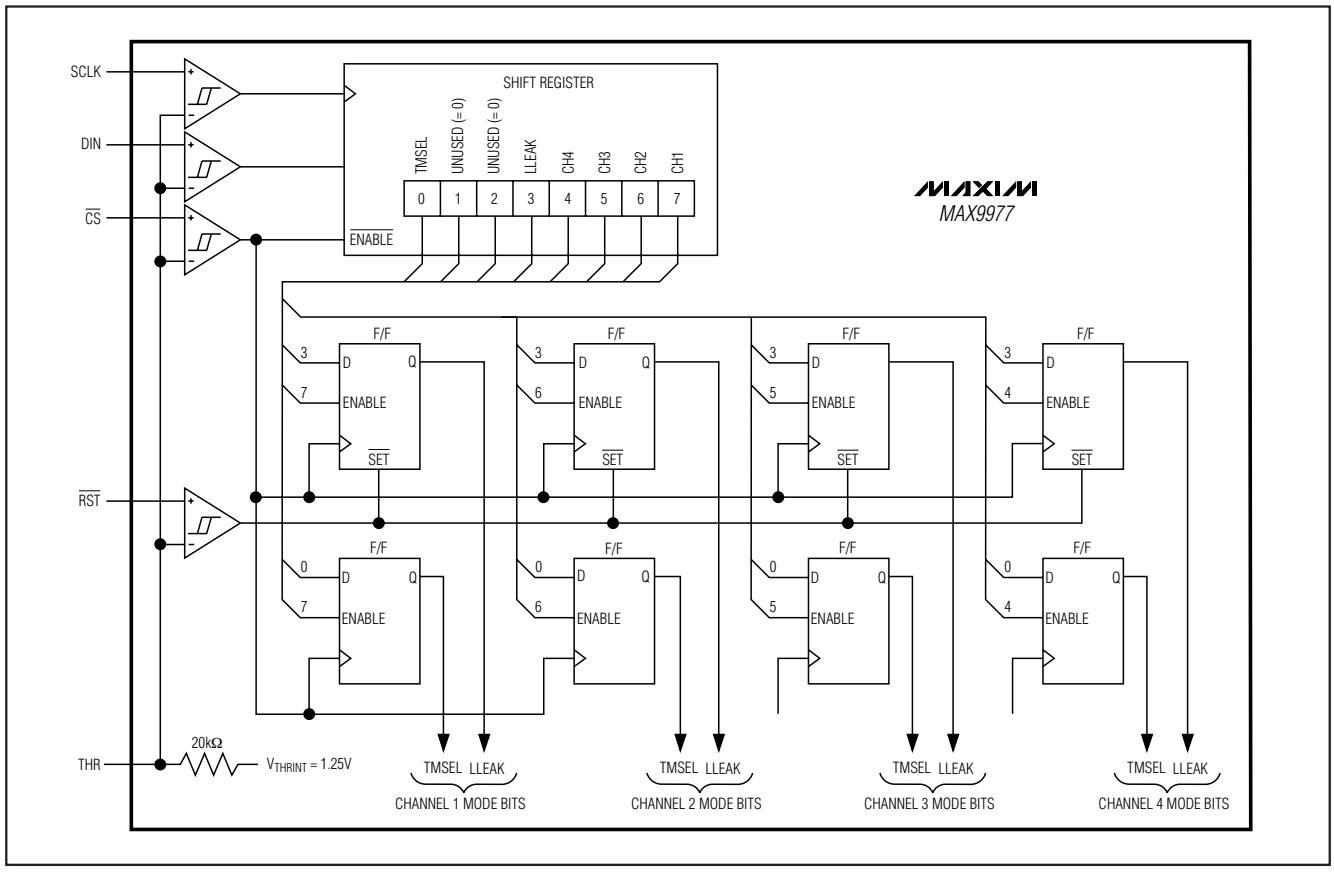


图3. 串行接口

表2. 串行接口位说明

BIT	NAME	DESCRIPTION	BIT STATE AFTER RESET AND AT POWER-UP
D7	CH1	Channel 1 Write Enable. Set to 1 to update the control byte for channel 1. Set to 0 to make no changes to channel 1.	0
D6	CH2	Channel 2 Write Enable. Set to 1 to update the control byte for channel 2. Set to 0 to make no changes to channel 2.	0
D5	CH3	Channel 3 Write Enable. Set to 1 to update the control byte for channel 3. Set to 0 to make no changes to channel 3.	0
D4	CH4	Channel 4 Write Enable. Set to 1 to update the control byte for channel 4. Set to 0 to make no changes to channel 4.	0
D3	LLEAK	Low-Leakage Select. Set to 1 to put driver in low-leakage mode. Set to 0 for normal operation.	1
D2	UNUSED	These bits are not used. Their logic state has no effect.	X
D1	UNUSED		X
D0	TMSEL	Termination Select. Driver termination select bit.	0

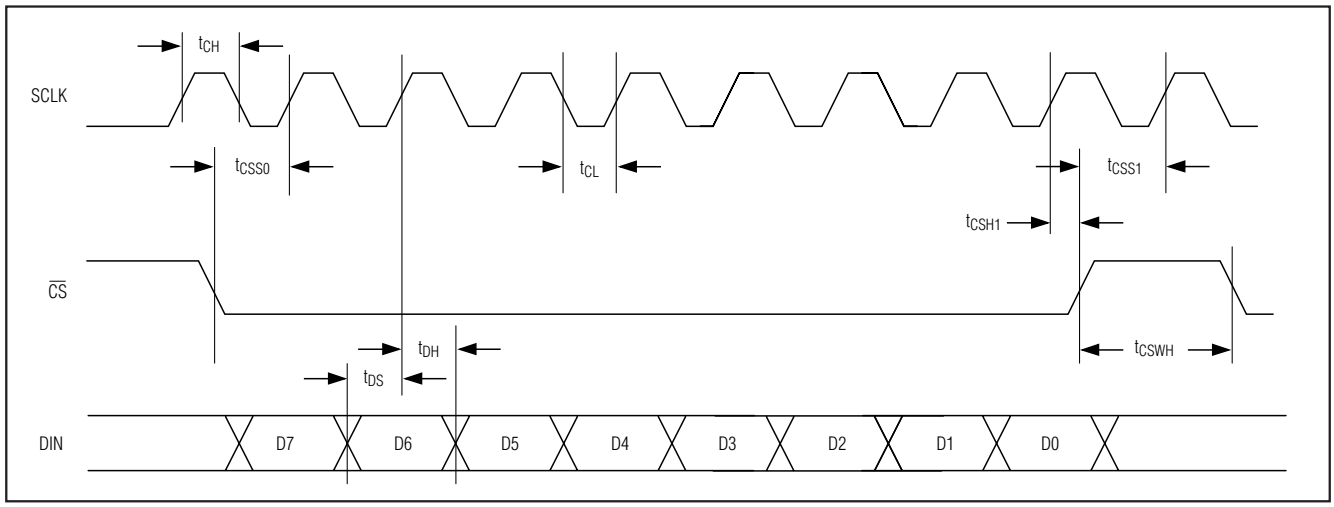


图4. 串口时序

低泄漏模式，LLEAK

通过串口将LLEAK置位，或利用$\overline{RST}$使MAX9977进入低泄漏状态(参考*Electrical Characteristics*)。该模式不需要输出断开与继电器的连接，即可方便进行IDDQ和PMU测量。对于每个通道，LLEAK可独立编程设置。

当DUT_以高速信号驱动，而LLEAK置位时，泄漏电流瞬间增大并超过正常工作时的限制。*Electrical Characteristics*表中的低泄漏恢复指标给出了器件在这种条件下的运行状态。

GS输入

地检测输入端GS为多路复用器的输入提供一个地电位参考。将GS与驱动DHV_、DTV_和DLV_的DAC电路的接地端连接。

GS偏离DHV_、DLV_和DTV_范围，以保证当GS变化时提供适当的余量。在GS变化的情况下，必须保持足够的电压余量。确保：

$$V_{CC} \geq 9.5V + Max\ (V_{GS})$$

$$V_{EE} \leq -4.5V + Min\ (V_{GS})$$

温度监视

MAX9977提供温度输出信号TEMP，当管芯温度等于+70°C (343K)时，输出标称值为3.33V的电压。此输出电压与温度成正比，比例系数为10mV/°C。

散热

在常规环境下，MAX9977需要外部散热器通过裸焊盘进行散热。裸焊盘与V_{EE}等电势，必需连接至V_{EE}或进行隔离。

裸焊盘封装的θ_{JC}大约为1°C/W至2°C/W，因此管芯温度很大程度上取决于应用中的散热方案。在以下条件下总功耗最大：

- V_{CC} = +10.5V
- V_{EE} = -5.25V
- $V_{DHV\_}$ = 6.5V，DATA = 高电平
- 短路电流 = 60mA

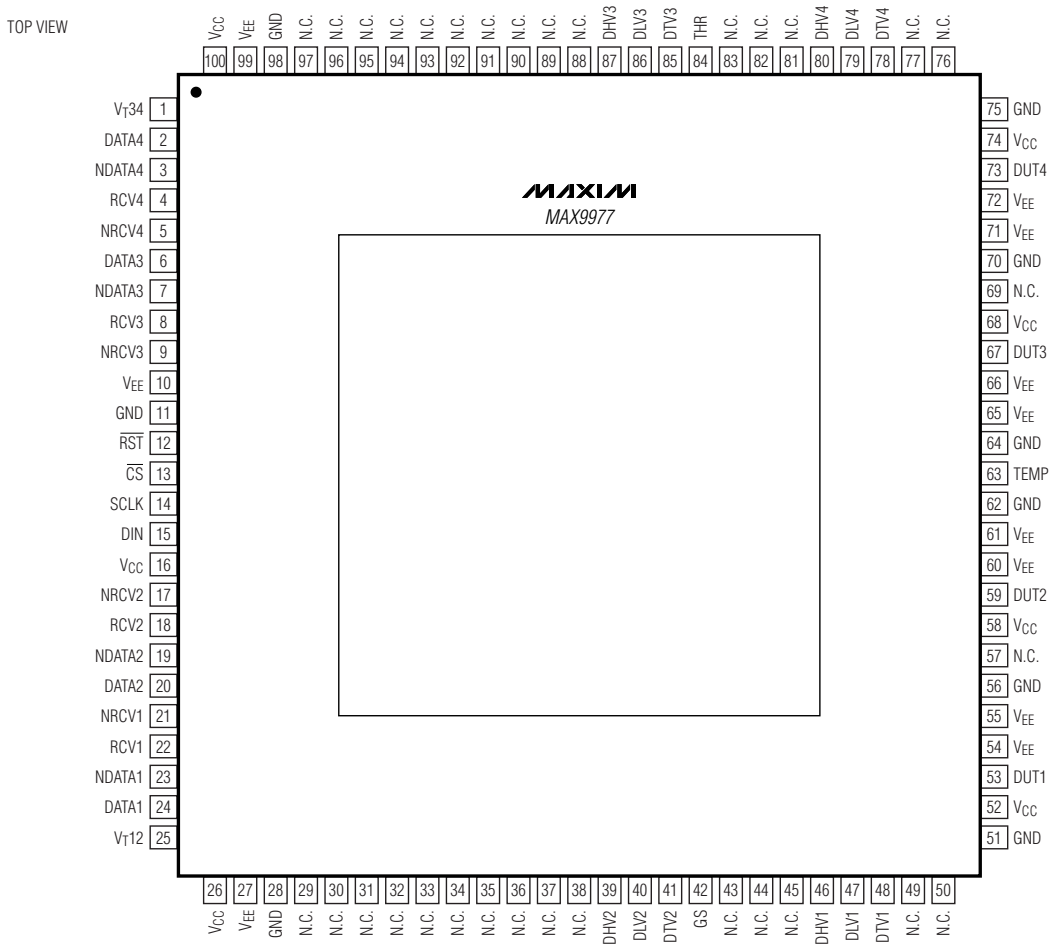
在这些极限条件下，总功耗大约为5.8W。如果在这些条件下，管芯温度不能维持在可以接受的水平，可通过软箝位将负载输出电流限制在较低值和/或降低电源电压。

电源考虑

所有V_{CC}和V_{EE}电源输入引脚通过0.01µF电容旁路，并使用至少10µF的大电容旁路每个电源。

四通道、低功耗、1200Mbps ATE驱动器

引脚配置



TQFP-IDP

选型指南

PART	INTERNAL DATA_ AND RCV_ TERMINATIONS	HEAT EXTRACTION
MAX9977AKCCQ	100Ω with center tap	Top
MAX9977ADCCQ*	None	Top

**未来产品—供货信息请与厂商联系。*

封装信息

(如需最近的封装外型信息，请查询 **www.maxim-ic.com.cn/packages**。)