MSP430F42X0混合信号微控制器

特性

- 低电源电压范围：1.8V-3.6V
- 超低功耗:活动模式:250μA@1MHz，2.2V
  待机模式:1.1μA
  关闭模式(RAM保持):0.1μA
- 五种省电模式
- 6μs内从待机模式唤醒
- 16位RISC体系，125ns指令周期
- 16位带内部参考的Σ-△模数转换器
- 12位数模转换器
- 带3个捕获/比较寄存器的16位定时器Timer_A
- 节电（Brownout）检测器
- 引导加载程序（BSL）
- 串行在线编程，无需外部编程电压
- 安全熔丝可编程代码保护
- 集成56段带对比度控制LCD驱动器
- MSP430x42x0系列器件包括：- MSP430F4250：16KB ROM，256B RAM 256B Flash Memory
  - MSP430F4260：24KB ROM，256B RAM 256B Flash Memory
  - MSP430F4270：32KB ROM，256B RAM 256B Flash Memory
- 完整的模块说明，参见MSP430x4xx系列用户指南，文献号SLAU056

说明

德州仪器MSP430系列超低功耗控制器由针对多种不同应用具有不同外围模块的芯片组成。其结构与五种低功耗模式相结合，适合在便携测量应用中实现延长电池寿命的目的。芯片具有强大的16位精简指令集，16位寄存器和常数发生器，可以实现最大代码执行效率。数字控制振荡器（DCO）使得从低功耗模式到活动模式的唤醒时间小于6μs。

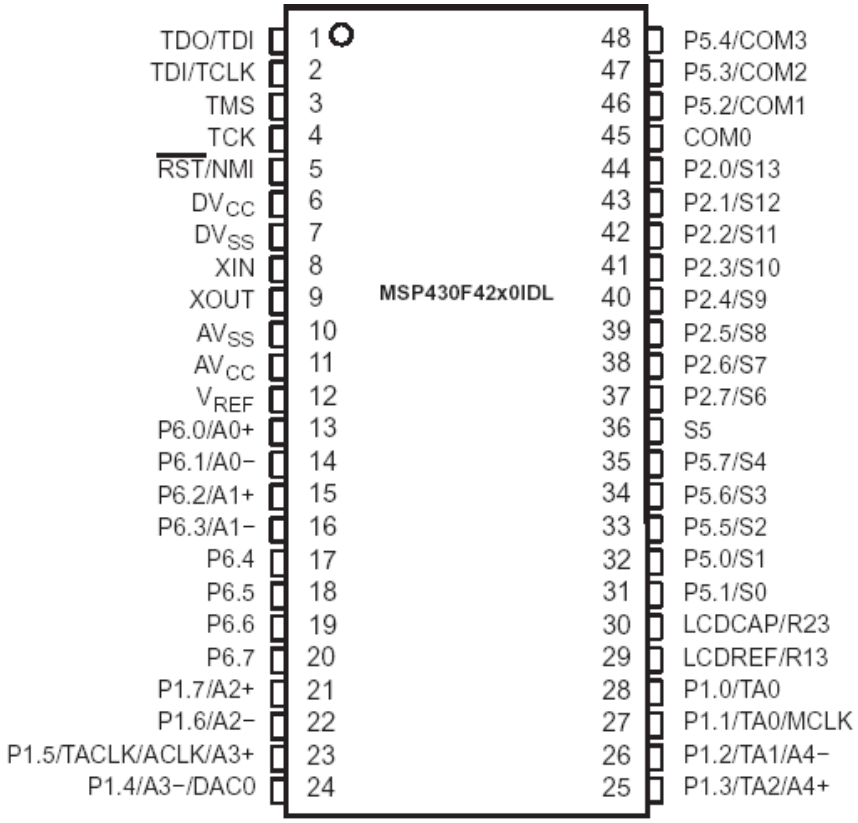
MSP430x42x0系列是一款配置有16位定时器，16位高性能Σ-△模数转换器，12位数模转换器，32个I/O口和液晶显示驱动的微控制器。

典型应用包括模拟和数字传感系统，数字马达控制，远程控制，自动调温器，数字定时器，手持式仪表等。

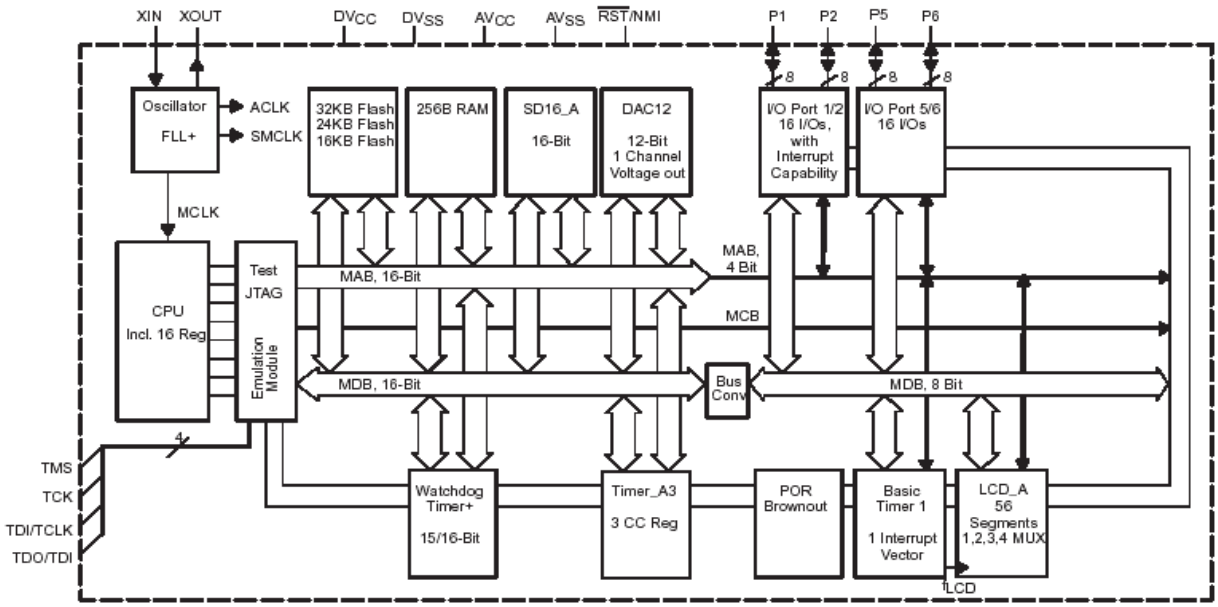
可用选项

TA	封装器件
	塑料 48-PIN SSOP(DL)
-40ºC to 85ºC	MSP430F4250IDL
	MSP430F4260IDL
	MSP430F4270IDL

MSP430F42x0引脚说明



MSP430F42x0功能框图



MSP430F42x0引脚功能

引脚			说明
名称	序号	I/O	
TDO/TDI	1	I/O	测试数据输出口．TDO/TDI数据输出或编程数据入口端
TDI/TCLK	2	I	测试数据输入或测试时钟输入.器件保护熔丝与TDI/TCLK相连
TMS	3	I	测试模式选择.TMS被用做器件编程和测试输入口
TCK	4	I	测试时钟.TCK是器件编程和测试的时钟入口
RST/NMI	5	I	通用数字I/O口/复位输入或非屏蔽中断输入端口
DVcc	6		数字电源电压,正端
DVss	7		数字电源电压,负端
XIN	8	I	晶体振荡器XT1的输入端
XOUT	9	O	晶体振荡器XT1的输出端
AVss	10		模拟电源电压，负端
AVcc	11		模拟电源电压，正端.
VREF	12	I/O	模拟参考电压
P6.0/A0+	13	I/O	通用数字I/O /模拟输入A0+
P6.1/A0-	14	I/O	通用数字I/O /模拟输入A0-
P6.2/A1+	15	I/O	通用数字I/O /模拟输入A1+
P6.3/A1-	16	I/O	通用数字I/O /模拟输入A1-
P6.4	17	I/O	通用数字I/O
P6.5	18	I/O	通用数字I/O
P6.6	19	I/O	通用数字I/O
P6.7	20	I/O	通用数字I/O
P1.7/A2+	21	I/O	通用数字I/O/ 模拟输入A2+
P1.6/A2-	22	I/O	通用数字I/O/ 模拟输入A2-
P1.5/TACLK/ACLK/A3+	23	I/O	通用数字I/O/ Timer_A，TACLK时钟信号输入 ACLK输出(1,2,4或8分频)/模拟输入A3+
P1.4/A3-/DAC0	24	I/O	通用数字I/O/ 模拟输入A3-/DAC12输出
P1.3/TA2/A4+	25	I/O	通用数字I/O/Timer_A,捕获:CCI2A，比较：Out2输出/模拟输入A4+
P1.2/TA1/A4-	26	I/O	通用数字I/O/Timer_A，捕获:CCI1A,比较：Out1输出/模拟输入A4-
P1.1/TA0/MCLK	27	I/O	通用数字I/O/Timer_A，捕获:CCI0B/MCLK输出
P1.0/TA0	28	I/O	通用数字I/O/ Timer_A，捕获:CCI0A 输入/比较：Out0输出/BSL信号发送
LCDREF/R13	29		外部LCD参考电压输入/LCD模拟电压3输入口（V3或者V4）
LCDCAP/R23	30		LCD电荷泵的电容接口/ LCD模拟电压2输入口（V2）
P5.1/S0	31	I/O	通用数字I/O/LCD段输出0
P5.0/S1	32	I/O	通用数字I/O/LCD段输出1
P5.5/S2	33	I/O	通用数字I/O/LCD段输出2
P5.6/S3	34	I/O	通用数字I/O/LCD段输出3

P5.7/S4	35	I/O	通用数字I/O/LCD段输出4
S5	36	I/O	LCD段输出5
P2.7/S6	37	I/O	通用数字I/O/LCD段输出6
P2.6/S7	38	I/O	通用数字I/O/LCD段输出7
P2.5/S8	39	I/O	通用数字I/O/LCD段输出8
P2.4/S9	40	I/O	通用数字I/O/LCD段输出9
P2.3/S10	41	I/O	通用数字I/O/LCD段输出10
P2.2/S11	42	I/O	通用数字I/O/LCD段输出11
P2.1/S12	43	I/O	通用数字I/O/LCD段输出12
P2.0/S13	44	I/O	通用数字I/O/LCD段输出13
COM0	45	O	LCD公共输出0,COM0-3用于LCD
P5.2/COM1	46	I/O	通用数字I/O/LCD公共输出1,COM0-3用于LCD
P5.3/COM2	47	I/O	通用数字I/O/LCD公共输出2,COM0-3用于LCD
P5.4/COM3	48	I/O	通用数字I/O/LCD公共输出3,COM0-3用于LCD

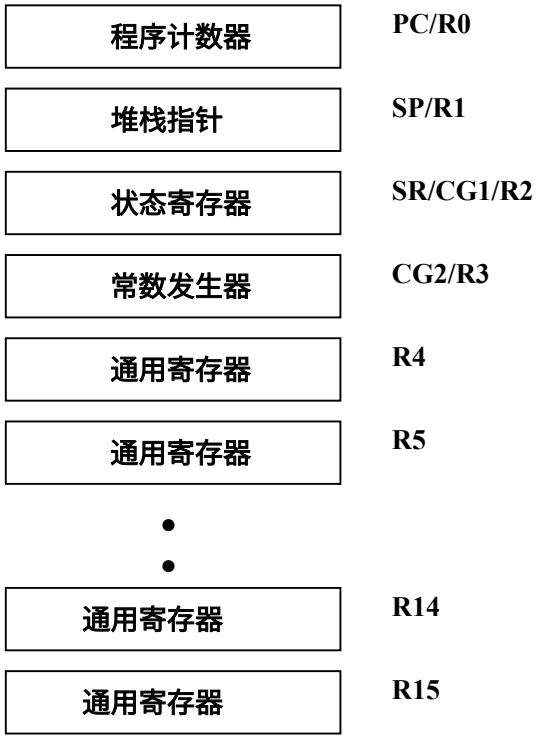
简要说明

CPU

MSP430 CPU具有16位精简指令结构，对应用来说是高度透明的。所有操作，除了程序流指令以外，都是作为寄存器操作，结合7种源操作数寻址方式和4种目的操作数寻址方式来执行的。

CPU 内部集成 16 个寄存器，减小了指令执行时间。寄存器到寄存器操作执行时间减少到处理器频率的一个周期。4 个寄存器 R0 到 R3 被保留，专门用作程序计数器，堆栈计数器，状态寄存器，和常数发生器，其余的寄存器可用作通用寄存器。

外设利用一个数据、地址和控制总线连接到CPU，并能容易的利用所有处理指令操作。



指令集

这个指令集由三种格式和七种寻址方式的 51 条指令组成。每条指令都能用字或字节方式。表 1 给出了三类指令格式的例子，寻址方式在表 2 中列出。

表 1 指令字格式

双操作数，源-目的	例如 ADD R4，R5	R4+R5→R5
单操作数，仅目的	例如 CALL R8	PC→（TOS），R8→PC
相对跳转，无／有条件	例如 JNE	不相等，跳转

表 2 寻址方式说明

寻址方式	s	d	语法	例子	操作
寄存器	√	√	MOV Rs， Rd	MOV R10， R11	R10→R11
索引	√	√	MOV X(Rn)， Y(Rm)	MOV 2(R5)， 6(R6)	M(2 + R5) → M(6 + R6)
符号(PC 相对)	√	√	MOV EDE， TONI		M(EDE) → M(TONI)
绝对	√	√	MOV &MEM，TCDAT		M(MEM) → M(TCDAT)
间接	√		MOV @Rn， Y(Rm)	MOV @R10，Tab(R6)	M(R10) → M(Tab + R6)
间接自动增量	√		MOV @Rn+， RM	MOV @R10+， R11	M(R10)→R11, R10 + 2→R10
立即	√		MOV #X， TONI	MOV #45， TONI	#45→ M(TONI)

注意： s =源 d =目的

工作模式

MSP430 具有一种活动模式和五种软件可选择的低功耗运行模式。中断事件可以将芯片从五种低功耗模式的任何一种唤醒，服务中断请求并返回中断程序之前的低功耗模式。

可以通过软件配置下列 6 种工作模式：

- 活动模式 AM：
  - 所有时钟是活动的。
- 低功率方式 0(LPM0)：
  - CPU被禁止。
  - ACLK和SMCLK保持活动。MCLK能用于模块。
  - FLL+环路控制保持活动。
- 低功率方式 1(LPM1)：
  - CPU 被禁止。
  - FLL+环路控制被禁止。
  - ACLK 和 SMCLK 保持活动。
  - MCLK 能用于模块。
- 低功率方式 2(LPM2)：
  - CPU 被禁止。
  - MCLK 和 FLL+环路控制以及 DCOCLK 被禁止。
  - DCO 的直流发生器保持活动。
  - ACLK 保持活动。
- 低功率方式3(LPM3)：
  - CPU被禁止。
  - MCLK， FLL+环路控制和DCOCLK被禁止。
  - DCO's 直流发生器禁止。
  - ACLK保持活动。

- 低功率方式 4(LPM4)：
  - CPU 禁止
  - ACLK 禁止
  - MCLK、FLL+环路控制和 DCOCLK 被禁止。
  - DCO 的直流发生器被禁止。
  - 晶体振荡器停止。

中断向量地址

中断向量和上电启动地址位于地址范围0FFFFH-0FFE0H。向量包含相应的中断处理指令序列的16位地址。

表3 **MSP430F42x0**的中断源，中断标志，和中断向量

中断源	中断标志	系统中断	字地址	优先级
上电 外部复位 看门狗 闪速存储器 程序计数器范围溢出 (见注4)	WDTIFG KEYV (见注1)	复位	0FFFEh	15, 最高
NMI(非屏蔽中断) 振荡器故障 闪速存储器非法访问	NMIIFG (见注1和3) OFIFG (见注1和3) ACCVIFG (见注1和3)	(非)屏蔽 (非)屏蔽 (非)屏蔽	0FFFCh	14
			0FFFAh	13
Σ -△ SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (见注1和2)	可屏蔽	0FFF8h	12
			0FFF6h	11
看门狗定时器	WDTIFG	可屏蔽	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer_A3	TACCR0 CCIFG0 (注2)	可屏蔽	0FFECh	6
Timer_A3	TACCR1 CCIFG1, TACCR2 CCIFG2, TAIFG (见注1和2)	可屏蔽	0FFEAh	5
I/O端口P1(8个标志)	P1IFG.0到 P1IFG.7 (见注1和2)	可屏蔽	0FFE8h	4
DAC12	DAC12_0IFG(见注2)	可屏蔽	0FFE6h	3
			0FFE4h	2
I/O端口P2(8个标志)	P2IFG.0到 P2IFG.7 (见注1和2)	可屏蔽	0FFE2h	1
基本定时器1	BTIFG	可屏蔽	0FFE0h	0, 最低

注释:

1．多源中断

2．中断标志位于模块中

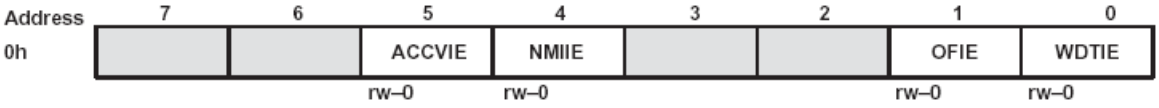
3．(非)屏蔽：独立中断允许位可以禁止中断事件，但是全局中断允许位不能禁止.

4．如果CPU试图从模块寄存器存储器地址范围(0h-1FFh)取指，将发生复位。

特殊功能寄存器

MSP430特殊功能寄存器(SFR)位于最低地址空间，并按字节模式寄存器组织。特殊功能寄存器应用字节指令访问。

中断使能寄存器1和2



WDTIE: 看门狗定时器中断使能。当选择看门狗方式时不活动。当定时器配置为一个通用定时器时该位激活。

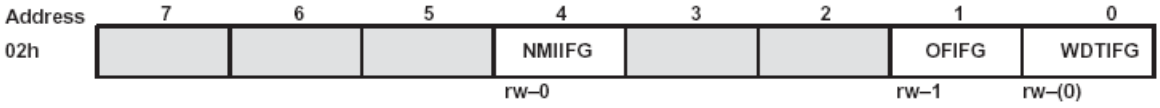
OFIE: 振荡器故障中断使能。

NMIIE: 非屏蔽中断使能。

ACCVIE: 闪速存储器非法访问中断使能。

BTIE: 基本定时器中断使能。

中断标志寄存器1和2



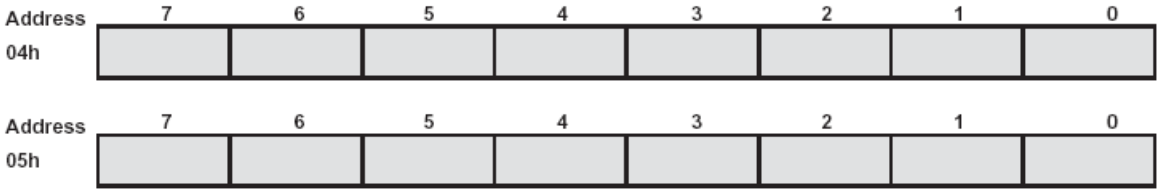
WDTIFG: 当看门狗定时器溢出(看门狗方式)或口令出错时置位。当VCC上电或RST/NMI引脚在复位方式下有复位条件时复位。

OFIFG: 当振荡器有故障时置位。

NMIIFG: 通过RST/NMI引脚置位。

BTIFG: 基本定时器中断标志。

模块使能寄存器1和2



图例: rw: 位可读写。

rw-0,1: 位可读写，由 PUC 复位或置位。

rw-(0,1): 位可读写，由 POR 复位或置位。

不存在于器件中的SFR位。

存储器组织

		MSP430F4250	MSP430F4260	MSP430F4270
存储器 主:中断矢量 主:代码存储器	大小 闪存 闪存	16kB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	24kB 0FFFFh – 0FFE0h 0FFFFh – 0A000h	32kB 0FFFFh – 0FFE0h 0FFFFh – 08000h
信息存储器	大小 闪存	256位 010FFh – 01000h	256位 010FFh – 01000h	256位 010FFh – 01000h
引导存储器	大小 ROM	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h	1kB 0FFFh – 0C00h
RAM	大小	256位 02FFh – 0200h	256位 02FFh – 0200h	256位 02FFh – 0200h
外围设备	16位 8位 8位SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

引导装载程序(BSL)

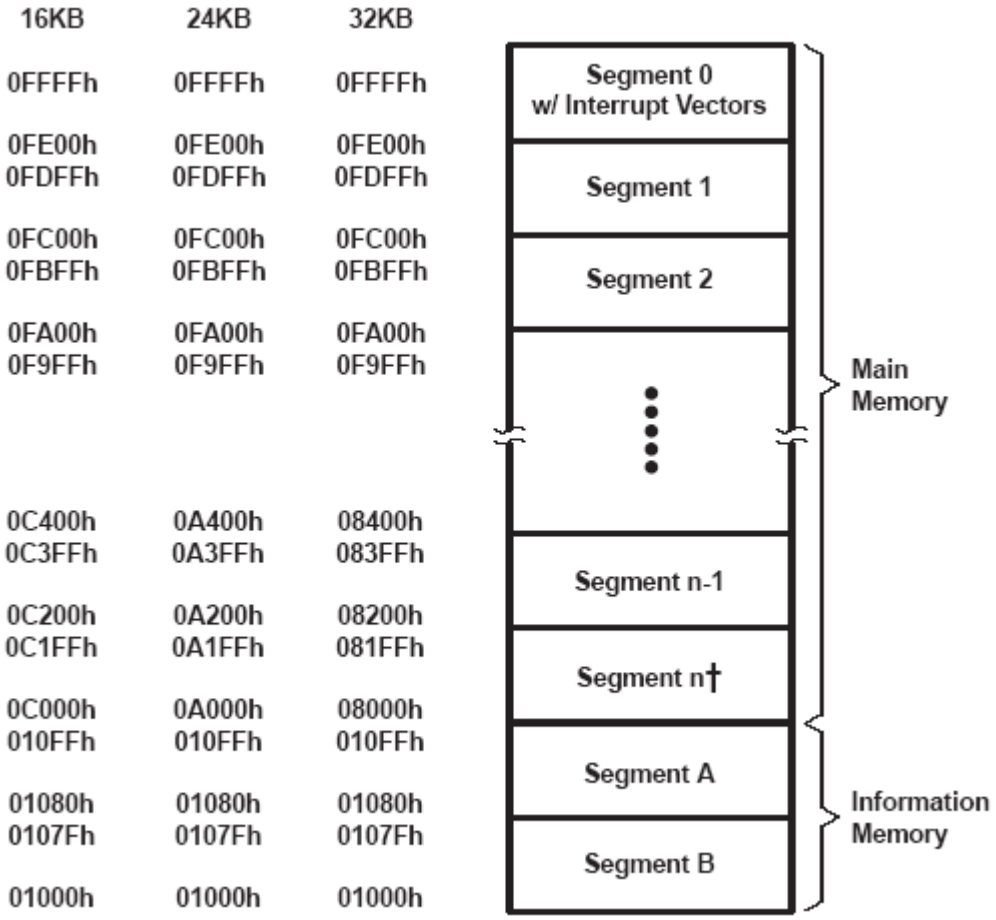
MSP430引导装载程序(BSL)使用户能够通过一个UART串行接口对FLASH存储器或者RAM进行编程。通过BSL对MSP430存储器的操作是由用户定义的密码保护的。要获得BSL特性的完整描述和它的执行过程，参见用户报告《MSP430引导加载程序》，文献号 SLAA089。

BSL功能	DL封装管脚
数据发送	28 – P1.0
数据接受	27 – P1.1

闪速存储器

闪速存储器可以通过 JTAG 接口、引导装载程序或者 CPU 在系统编程。CPU 可以对闪速存储器进行单字节或者单字的写操作。闪速存储器的特性包括：

- 闪速存储器有n段主存储器和每段128字节的两段信息存储器(A和B)。主存储器中每个段长为512字节。
- 段 0 到 n 可以一步擦除，也可以每段分别擦除。
- 段 A 和 B 可以分别擦除，或与段 0 到 n 作为一组擦除。
- 未编程的新器件在信息存储器中可能有一些已经编程的字节(用于生产期间的测试)。在首次使用之前用户应该执行一次对信息存储器的擦除。



片内外设

外设通过数据,地址,和控制总线连接到 CPU，并能用所有操作指令处理。若要完整的模块描述，请参考 MSP430x4xx 系列用户手册，文献号 SLAU056。

振荡器和系统时钟

MSP430FE42x0 系列芯片内部具有 FLL+模块，包括支持 32768Hz 钟表晶体振荡器，一个内部数控振荡器（DCO）和一个高频晶体振荡器。FLL＋时钟模块设计为能同时满足降低系统成本和系统功耗。FLL＋具有数字频率锁相环硬件特性，与数字调制器相连将 DCO 频率稳定在钟表晶振频率的一个可编程的倍数上。内部 DCO 提供一个快速启动的时钟源并在 6us 内稳定。FLL+模块提供下列时钟信号：

- 辅助时钟 ACLK，来源于 32768Hz 钟表晶振或者一个高频晶振
- 主系统时钟 MCLK，由系统和 CPU 使用。
- 子系统时钟 SMCLK，由外围模块使用。
- 辅助时钟 ACLK/n，ACLK、ACLK/2、ACLK/4 或者 ACLK/8 的缓冲输出。

Brownout

brownout掉电电路在上电和断电时用来为芯片提供正确的内部复位信号。供电电源监测器电路检测CPU在掉电电路释放芯片复位信号后开始代码执行。不过，这时VCC可能还没有达到VCC(min)。用户必须确保缺省的FLL+设置没有改变直到VCC到达VCC（min）。

数字I/O

具有4个8位I/O端口P1，P2，P5和P6

- 所有 I/O 位可单独编程。
- 任何输入、输出、和中断条件的结合都是可能的。
- P1 和 P2 端口的所有 8 位具有中断沿可选的中断输入能力。

所有指令支持对端口控制寄存器的读写操作。

基本定时器1

基本定时器的两个独立的 8 位定时器，也可级联组成一个 16 位的定时器/计数器。两个定时器可以软件读写。基本定时器 1 能用来产生周期性中断。

带可调整电荷泵的 LCD 驱动器

LCD_A 驱动器产生驱动液晶显示器的段信号和公共信号。LCD_A 控制器具有专用数据存储器保持段驱动信息。公共信号和段信号按照定义的模式产生。支持静态，2MUX、3MUX 和 4MUX 驱动模式。模块可通过内置的电荷泵提供独立于供电电源的 LCD 电压，因此还可以通过程序控制 LCD 电压的高低和对比度。

WDT看门狗定时器

看门狗定时器模块的基本功能是在发生软件问题时复位系统。如果设定的时间间隔溢出了，就会产生一个系统复位。如果看门狗功能在应用中并不需要，这个模块可以配置为一个内部定时器，在设定的时间间隔产生中断。

Timer_A3

Timer_A3 是一个 16 位的带有三个捕获/比较寄存器的定时器/计数器。Timer_A3 能够支持多重捕获/比较，PWM 输出和内部定时。定时器 A3 也具有可扩展的中断能力。中断可由计数器溢出和任一捕获/比较寄存器产生。

Timer_A3 Signal Connections					
Input Pin Number DL	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number DL
23 - P1.5	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
23 - P1.5	$\overline{\text{TACLK}}$	INCLK			
28 - P1.0	TA0	CCI0A	CCR0	TA0	28 - P1.0
27 - P1.1	TA0	CCI0B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
26 - P1.2	TA1	CCI1A	CCR1	TA1	26 - P1.2
26 - P1.2	TA1	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
25 - P1.3	TA2	CCI2A	CCR2	TA2	25 - P1.3
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

SD16_A

SD16_A 模块提供 16 位模数转换。集成了 16 位Σ-△模数转换内核和参考电压发生器，除了外部模拟输入外，还可以测量内部电压 VCC 和温度传感器。

DAC12

DAC12 模块是一个 12 位的，带电阻阶梯网络的电压输出的 DAC。它能以 8 位或 12 位模式工作。

MSP430FE427的外围存储器布局

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DAC12	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
SD16_A (see also: Peripherals with Byte Access)	General Control	SD16CTL	0100h
	Channel 0 Control	SD16CCTL0	0102h
	Interrupt vector word register	SD16IV	0110h
	Channel 0 conversion memory	SD16MEM0	0112h
PERIPHERALS WITH BYTE ACCESS			
SD16_A (see also: Peripherals with Word Access)	Channel 0 Input Control	SD16INCTL0	0B0h
	Analog Enable	SD16AE	0B7h
LCD_A	LCD Voltage Control 1	LCDAVCTL1	0AFh
	LCD Voltage Control 0	LCDAVCTL0	0AEh
	LCD Voltage Port Control 1	LCDAPCTL1	0ADh
	LCD Voltage Port Control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
FLL+Clock	FLL+ Control 1	FLL_CTL1	054h
	FLL+ Control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

开放室温范围运行条件下（除非另有说明）的最大额定值

施加在VCC上的相对于VSS的电压……-0.3V到4.1V

施加在任何引脚上的电压（参见注意）……-0.3V到VCC+0.3V

任何芯片终端上的二极管电流……±2mA

存储温度（未编程芯片）……-55℃到150℃

存储温度（已编程芯片）……-40℃到85℃

超过所列的“最大绝对允许值”的运行条件可能引起芯片的永久性损坏。这些只是额定的极限，并不代表芯片在超出“推荐运行条件”之外的条件下芯片能够正常运行。在一段时期内暴露在最大绝对额定值将影响芯片的可靠性。

注意：所有电压相对于 VSS.。JTAG 熔断电压，V_{FB} ，可超过最大绝对允许值。当熔断 JATG 熔丝时此电压施加于 TDI/TCLK。

推荐运行条件

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})			2.5		3.6	V
Supply voltage, V_{SS} (AV_{SS} = DV_{SS} = V_{SS})			0		0	V
Operating free-air temperature range, T_A			−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 1)	LF selected, XTS_FLL=0	Watch crystal		32.768		kHz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

注意：在LF模式下，LFXT1振荡器需要一个钟表晶振。在XT1模式下，LFXT1振荡器可接陶瓷协振器或晶振。

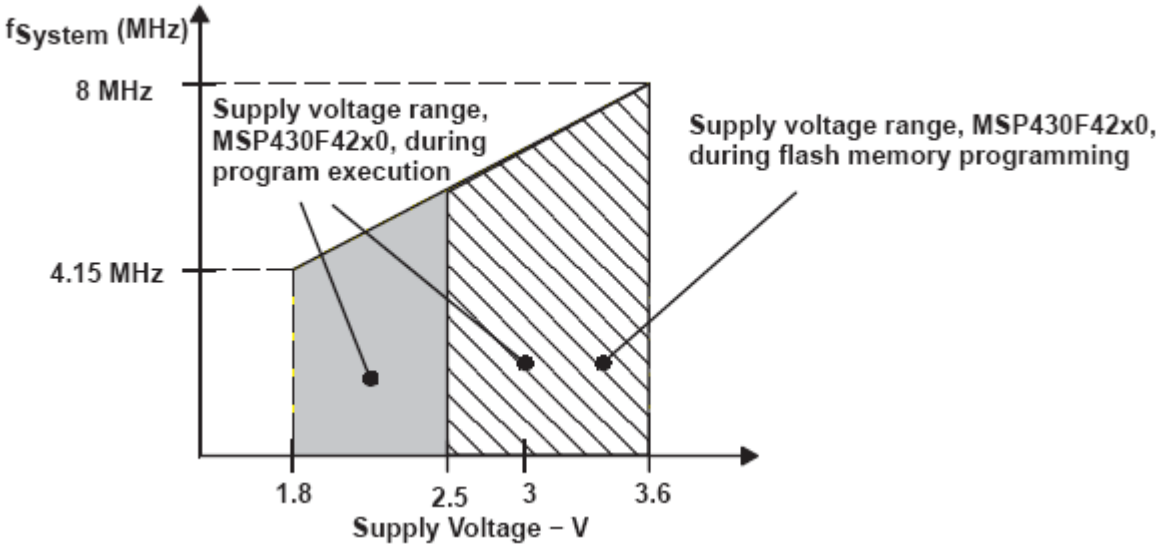


图 1 频率和供电电压，典型特征

在推荐运行室温条件下（除非另有说明）的电气特性：流入Avcc＋DVcc的供电电流，不包括外部电流

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)} = 1$ MHz, $f_{(ACLK)} = 32{,}768$ Hz XTS=0, SELM=(0,1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		250	370	µA
			V_{CC} = 3 V		400	520	
$I_{(LPM0)}$	Low-power mode, (LPM0) (see Note 1)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		55	70	µA
			V_{CC} = 3 V		95	110	
$I_{(LPM2)}$	Low-power mode, (LPM2), f(MCLK) = f (SMCLK) = 0 MHz, f(ACLK) = 32,768 Hz, SCG0 = 0 (see Note 2)	T_A = −40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32{,}768$ Hz, SCG0 = 1 Basic Timer1 enabled , ACLK selected LCD_A enabled, CPEN = 0: (static mode ; $f_{LCD} = f_{(ACLK)}/32$) (see Note 2 and Note 3)	T_A = −40°C	V_{CC} = 2.2 V		1.0	2.0	µA
		T_A = 25°C			1.1	2.0	
		T_A = 60°C			2.0	3.0	
		T_A = 85°C			3.5	6.0	
		T_A = −40°C	V_{CC} = 3 V		1.8	2.8	
		T_A = 25°C			1.6	2.7	
		T_A = 60°C			2.5	3.5	
		T_A = 85°C			4.2	7.5	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)} = 0$ MHz, $f_{(ACLK)} = 32{,}768$ Hz, SCG0 = 1 Basic Timer1 enabled , ACLK selected LCD_A enabled, CPEN = 0: (4-mux mode; $f_{LCD} = f_{(ACLK)}/32$) (see Note 2 and Note 3)	T_A = −40°C	V_{CC} = 2.2 V		2.5	3.5	µA
		T_A = 25°C			2.5	3.5	
		T_A = 85°C			3.8	6.0	
		T_A = −40°C	V_{CC} = 3 V		2.9	4.0	
		T_A = 25°C			2.9	4.0	
		T_A = 85°C			4.4	7.5	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1 (see Note 2)	T_A = −40°C	V_{CC} = 2.2 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 60°C			0.7	1.1	
		T_A = 85°C			1.7	3.0	
		T_A = −40°C	V_{CC} = 3 V		0.1	0.8	
		T_A = 25°C			0.1	0.8	
		T_A = 60°C			0.8	1.2	
		T_A = 85°C			1.9	3.5	

活动模式下电流消耗与系统频率的关系，F-版

$$I_{(AM)} = I_{(AM)\,[1\ MHz]} \times f_{(System)\ [MHz]}$$

活动模式下电流消耗与供电电压的关系，F-版

$$I_{(AM)} = I_{(AM)\,[3\ V]} + 175\ \mu A/V \times (V_{CC} - 3\ V)$$

施密特触发输入一端口P1，P2,P5和P6；RST/NMI;JTAG:TCK,TMS,TDI/TCLK,TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.55	V
		V_{CC} = 3 V	1.5		1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

输入端口Px.x,TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A capture timing	TA0, TA1, TA2	2.2 V	62			ns
			3 V	50			
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
			3 V			10	
$f_{(TAint)}$	Timer_A, clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
			3 V			10	

漏电流－端口 P1，P2，P5 和 P6（见 note1）

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

输出－端口P1，P2，P5和P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{CC}−0.6		V_{CC}	
		$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}−0.25		V_{CC}	
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 2	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

输出频率

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	(x = 1, 2, 5, 6; 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ±1.5 mA	V_{CC} = 2.2 V / 3 V	DC		f_{System}	MHz
$f_{(MCLK)}$	P1.1/TA0/MCLK	C_L = 20 pF				f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%− 15 ns	50%	50%+ 15 ns	

输出－端口P1，P2，P5和P6（继续）

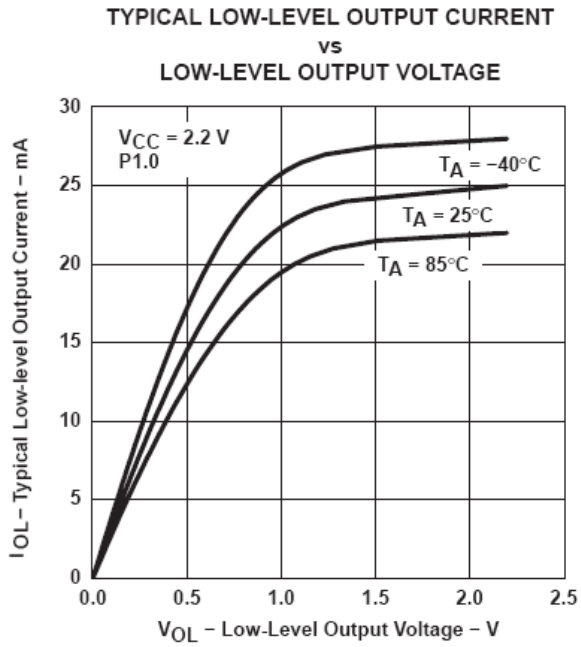


图 2

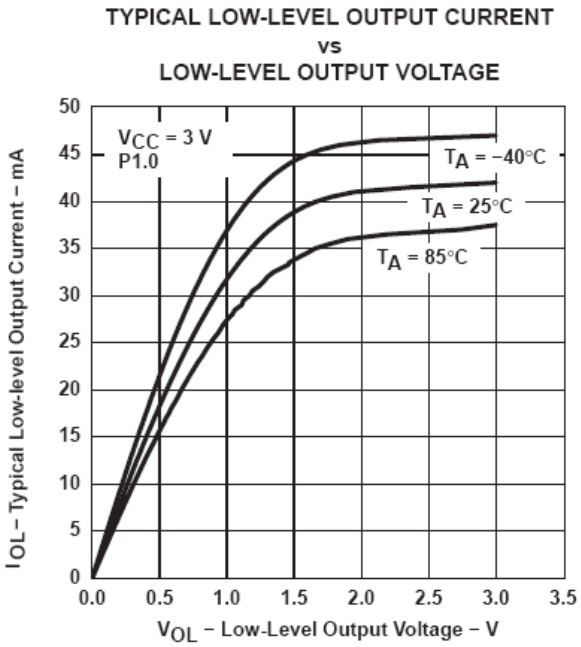


图 3

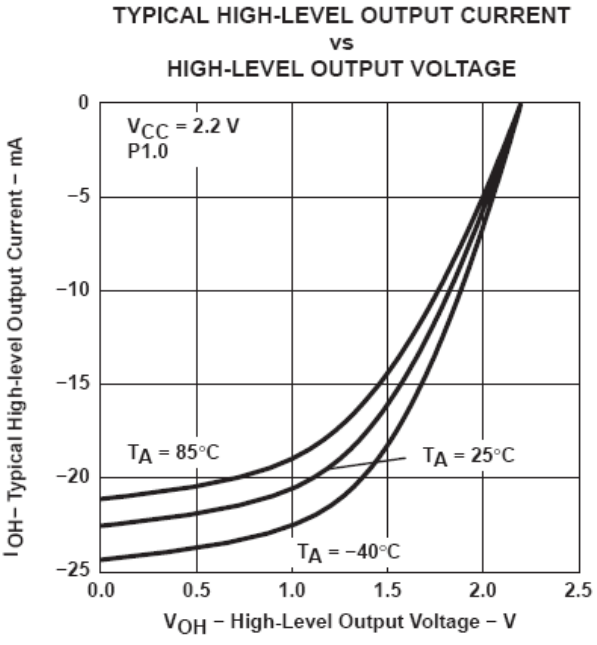


图 4

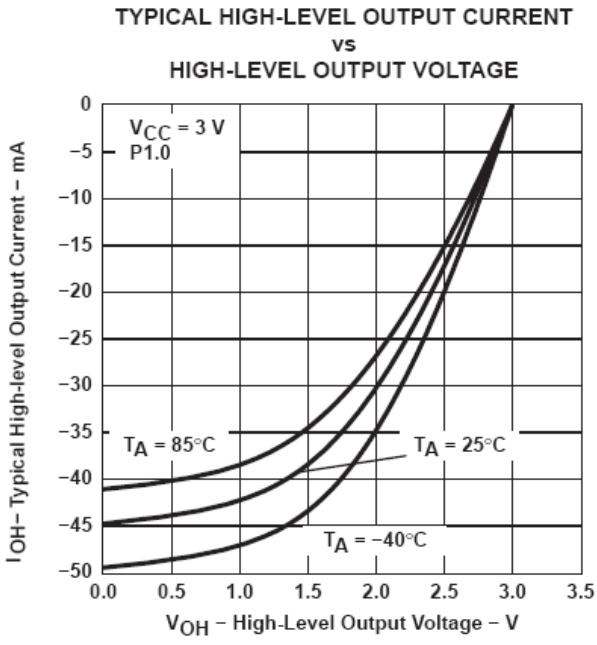


图 5

从LPM3唤醒

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 2.2 V/3 V			6	µs
		f = 2 MHz				6	
		f = 3 MHz				6	

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply Voltage Range	Charge pump enabled (CPEN = 1; VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (CPEN = 1; VLCDx > 0000)		4.7			µF
$I_{CC(LCD)}$	Supply Current	$V_{LCD(typ)}$=3V; CPEN = 1; VLCDx= 1000, all segments on f_{LCD}= f_{ACLK}/32 no LCD connected (see Note 2) T_A = 25°C	2.2 V		3.8		µA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			VCC		V
V_{LCD}	LCD voltage	VLCDx = 0001			2.60		V
V_{LCD}	LCD voltage	VLCDx = 0010			2.66		V
V_{LCD}	LCD voltage	VLCDx = 0011			2.72		V
V_{LCD}	LCD voltage	VLCDx = 0100			2.78		V
V_{LCD}	LCD voltage	VLCDx = 0101			2.84		V
V_{LCD}	LCD voltage	VLCDx = 0110			2.90		V
V_{LCD}	LCD voltage	VLCDx = 0111			2.96		V
V_{LCD}	LCD voltage	VLCDx = 1000			3.02		V
V_{LCD}	LCD voltage	VLCDx = 1001			3.08		V
V_{LCD}	LCD voltage	VLCDx = 1010			3.14		V
V_{LCD}	LCD voltage	VLCDx = 1011			3.20		V
V_{LCD}	LCD voltage	VLCDx = 1100			3.26		V
V_{LCD}	LCD voltage	VLCDx = 1101			3.32		V
V_{LCD}	LCD voltage	VLCDx = 1110			3.38		V
V_{LCD}	LCD voltage	VLCDx = 1111		TBD	3.44	TBD	V
R_{LCD}	LCD Driver Output impedance	V_{LCD} = 3V; CPEN = 1; VLCDx = 1000, I_{LOAD} = ±10µA	2.2 V			10	kOhm

POR/掉电复位（BOR）（见note1）

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6)		0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6 through Figure 8)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 6)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTES:
1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$ is ≤ 1.8V.
2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after V_{CC} = $V_{(B\_IT-)}$ + $V_{hys(B\_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x4xx Family User's Guide* (SLAU056) for more information on the brownout.

典型特性

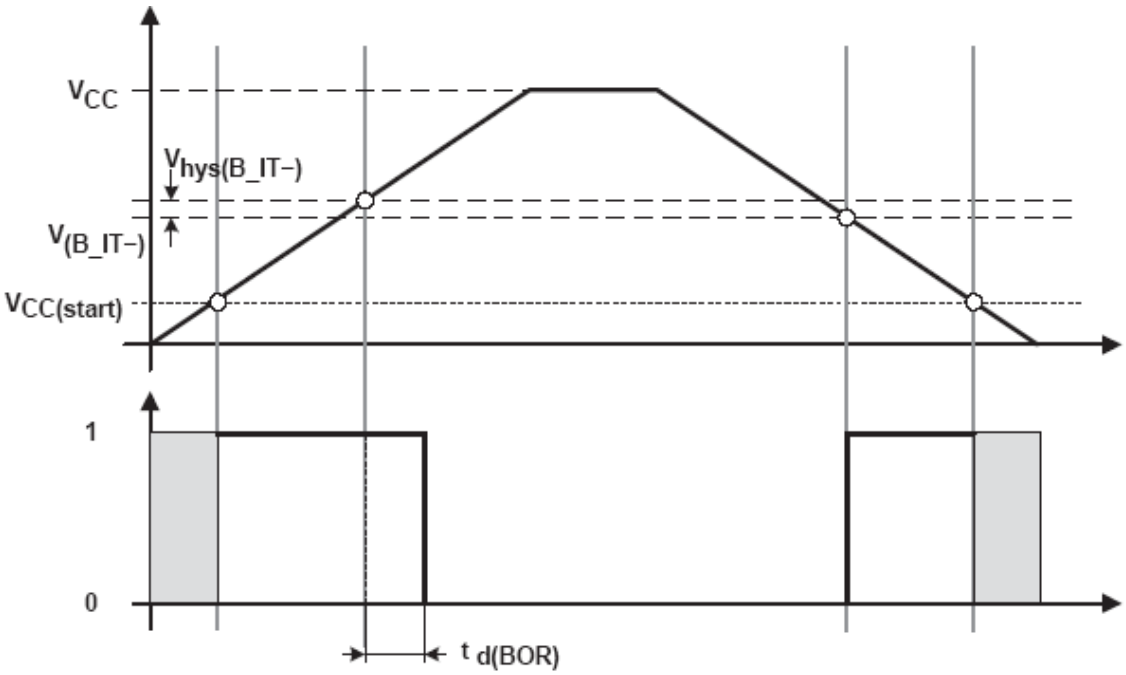


图6 POR/掉电复位（BOR）和电源电压

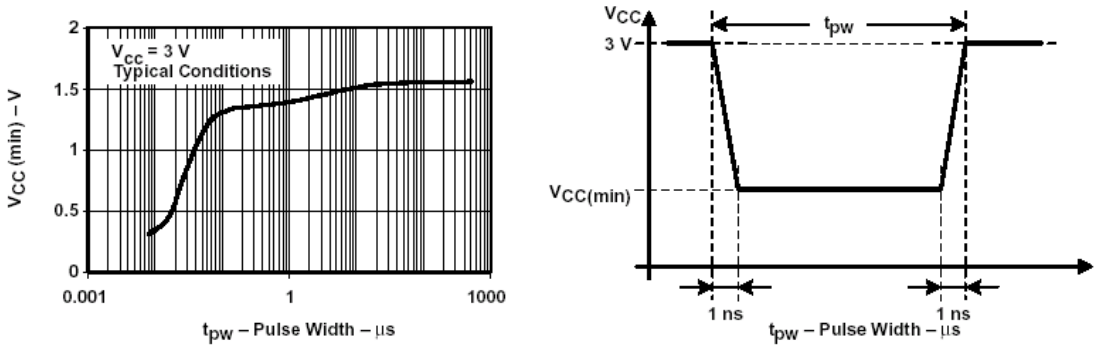


图7 V(CC)min电平上的方波电压降产生一次POR/掉电复位（BOR）信号

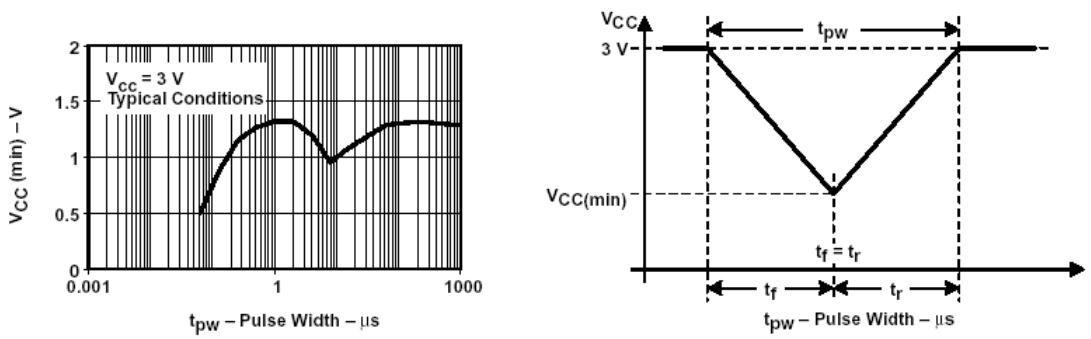


图8 V(CC)min电平上的三角形电压降产生一次POR/掉电复位（BOR）信号

DCO

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2; DCOPLUS= 0	2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0 ; DCOPLUS = 1	2.2 V	0.3	0.65	1.25	MHz
		3 V	0.3	0.7	1.3	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0; DCOPLUS = 1, (see Note 1)	2.2 V	2.5	5.6	10.5	MHz
		3 V	2.7	6.1	11.3	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1	2.2 V	0.7	1.3	2.3	MHz
		3 V	0.8	1.5	2.5	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCOPLUS = 1, (see Note 1)	2.2 V	5.7	10.8	18	MHz
		3 V	6.5	12.1	20	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1	2.2 V	1.2	2	3	MHz
		3 V	1.3	2.2	3.5	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	9	15.5	25	MHz
		3 V	10.3	17.9	28.5	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCOPLUS = 1	2.2 V	1.8	2.8	4.2	MHz
		3 V	2.1	3.4	5.2	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	13.5	21.5	33	MHz
		3 V	16	26.6	41	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCOPLUS = 1	2.2 V	2.8	4.2	6.2	MHz
		3 V	4.2	6.3	9.2	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x; DCOPLUS = 1, (see Note 1)	2.2 V	21	32	46	MHz
		3 V	30	46	70	
S_n	Step size between adjacent DCO taps: $S_n = f_{DCO(Tap\ n+1)} / f_{DCO(Tap\ n)}$, (see Figure 10 for taps 21 to 27)	1 < TAP ≤ 20	1.06		1.11	
		TAP = 27	1.07		1.17	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0, (see Note 2)	2.2 V	–0.2	–0.3	–0.4	%/°C
		3 V	–0.2	–0.3	–0.4	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2; DCOPLUS = 0 (see Note 2)		0	5	15	%/V

NOTES: 1. Do not exceed the maximum system frequency.
2. This parameter is not production tested.

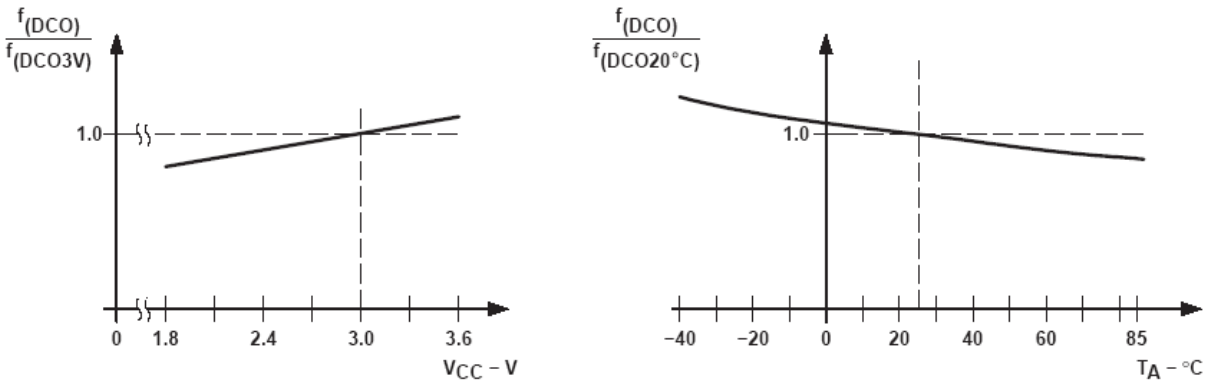


图9 DCO频率与供电电源Vcc和外部环境温度的关系

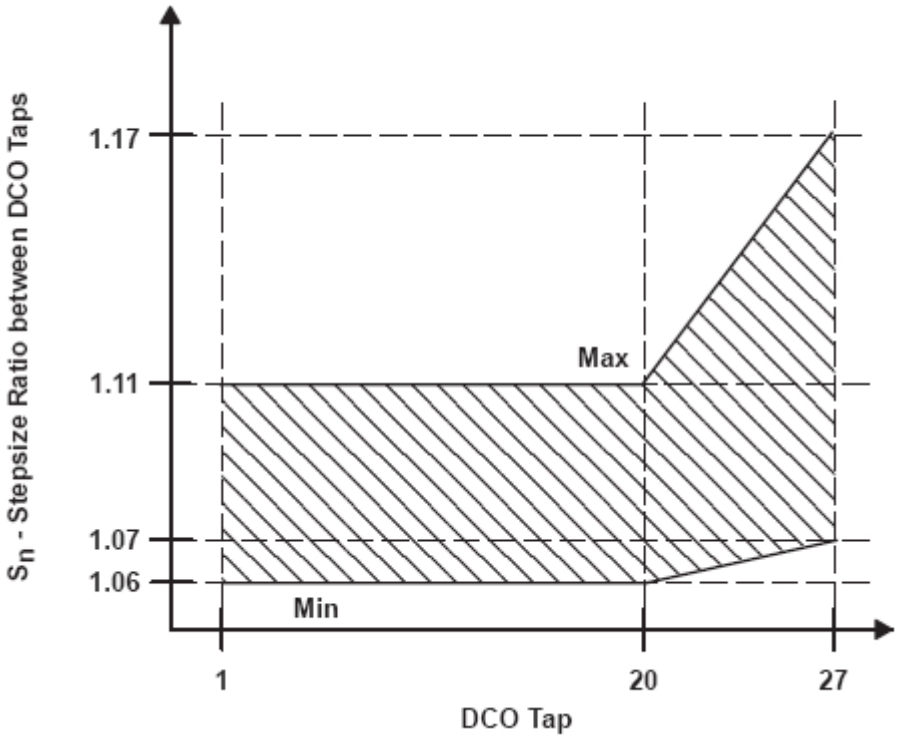


图10 DCO频率间隔大小

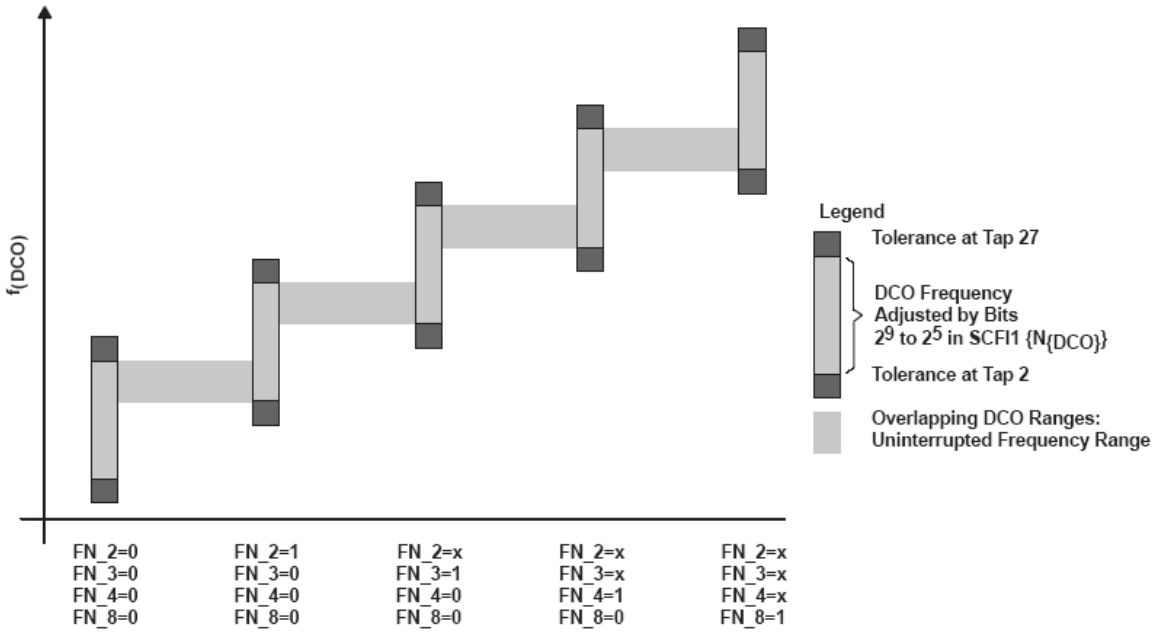


图11 五种由FN_x位控制的DCO交迭范围

晶体振荡器，LFXT1振荡器（见note1和note2）

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}			$0.8 \times V_{CC}$		V_{CC}	

NOTES:
1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}). This is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   - Keep as short of a trace as possible between the 'F42x0 and the crystal.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

SD16_A 供电电源和推荐操作条件

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00; GAIN: 1,2	3 V		650	TBD	µA
			SD16BUFx = 00; GAIN: 4,8,16	3 V		730	TBD	
			SD16BUFx = 00; GAIN: 32	3 V		1050	TBD	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00; GAIN: 1	3 V		620	TBD	
			SD16BUFx = 00; GAIN: 32	3 V		700	TBD	
		SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 01; GAIN: 1	3 V		TBD		
			SD16BUFx = 10; GAIN: 1	3 V		TBD		
			SD16BUFx = 11; GAIN: 1	3 V		TBD		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)		3 V	0.03	0.5		

SD16_A 输入范围

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full scale input voltage range	Bipolar Mode, SD16UNI = 0			$-V_{REF}/2GAIN$		$+V_{REF}/2GAIN$	mV
		Unipolar Mode, SD16UNI = 1			0		$+V_{REF}/2GAIN$	mV
V_{ID}	Differential input voltage range for specified performance (see Note 1)	SD16REFON=1	SD16GAINx = 1			±500		mV
			SD16GAINx = 2			±250		
			SD16GAINx = 4			±125		
			SD16GAINx = 8			±62		
			SD16GAINx = 16			±31		
			SD16GAINx = 32			±15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V		200		kΩ
			SD16GAINx = 32	3 V		75		
		f_{SD16} = 1MHz, SD16BUFx = 01	SD16GAINx = 1	3 V		>10		MΩ
Z_{ID}	Differential Input impedance (IN+ to IN−)	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V	300	400		kΩ
			SD16GAINx = 32	3 V	100	150		
		f_{SD16} = 1MHz, SD16BUFx > 00	SD16GAINx = 1	3 V		>10		MΩ
V_I	Absolute input voltage range	SD16BUFx = 00			AV_{SS} -0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} −1.2V	
V_{IC}	Common-mode input voltage range	SD16BUFx = 00			AV_{SS} -0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} −1.2V	

SD16_A 性能（f_{SD16}=30kHz，SD16REFON=1，SD16BUFx=01）

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-Noise + Distortion Ratio	SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 256	f_{IN} = 2.8Hz	3 V		84		dB
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 512		3 V		84		
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 1024		3 V		84		
	Nominal Gain	SD16GAINx = 1; SD16OSRx = 1024		3 V	0.97	1.00	1.02	
dG/dT	Gain Temperature Drift	SD16GAINx = 1; SD16OSRx = 1024 (see Note 1)		3 V		15		ppm/°C
dG/dV_{CC}	Gain Supply Voltage Drift	SD16GAINx = 1; SD16OSRx = 1024; V_{CC} = 2.5V - 3.6V (see Note 2)				0.35		%/V

SD16_A 性能（f_{SD16}=1MHz，SD16OSRx=256，SD16REFON=1，SD16BUFx=00）

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-Noise + Distortion Ratio	SD16GAINx = 1,Signal Amplitude = 500mV	f_{IN} = 50Hz, 100Hz	3 V	83.5	85		dB
		SD16GAINx = 2,Signal Amplitude = 250mV		3 V	81.5	84		
		SD16GAINx = 4,Signal Amplitude = 125mV		3 V	76	79.5		
		SD16GAINx = 8,Signal Amplitude = 62mV		3 V	73	76.5		
		SD16GAINx = 16,Signal Amplitude = 31mV		3 V	69	73		
		SD16GAINx = 32,Signal Amplitude = 15mV		3 V	62	69		
G	Nominal Gain (see Note 1)	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2		3 V	1.90	1.96	2.02	
		SD16GAINx = 4		3 V	3.76	3.86	3.96	
		SD16GAINx = 8		3 V	7.36	7.62	7.84	
		SD16GAINx = 16		3 V	14.56	15.04	15.52	
		SD16GAINx = 32		3 V	27.20	28.35	29.76	
E_{OS}	Offset Error (see Note 1)	SD16GAINx = 1		3 V			±0.2	%FSR
		SD16GAINx = 32		3 V			±1.5	
dE_{OS}/dT	Offset Error Temperature Coefficient (see Note 1)	SD16GAINx = 1		3 V		±4	±20	ppm FSR/°C
		SD16GAINx = 32		3 V		±20	±100	
CMRR	Common-Mode Rejection Ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>75		
PSRR	Power Supply Rejection Ratio	SD16GAINx = 1		3 V		>80		dB

SD16_A 温度传感器

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient	See Note 1		1.18	1.32	1.46	mV/K
$V_{Offset,sensor}$	Sensor offset voltage	See Note 1		−100		100	mV
V_{Sensor}	Sensor output voltage (see Note 3)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C	3 V	355	395	435	
		Temperature sensor voltage at T_A = 0°C (see Note 1)	3 V	320	360	400	

NOTES: 1. Not production tested, limits characterized.
2. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor} (273 + T [°C]) + V_{Offset,sensor} [mV]$
3. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.

SD16_A内部电压参考

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0	3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1; SD16VMIDON = 0	3 V			±200	nA
t_{ON}	Turn on time	SD16REFON = 0->1; SD16VMIDON = 0; C_{REF} = 100nF	3 V		5		ms
PSRR	Line regulation	SD16REFON = 1; SD16VMIDON = 0	3 V		10		uV/V

NOTES: 1. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A， 参考源输出缓冲

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference Supply + Reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	µA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			±1	mA
	Maximum voltage variation vs. load current	$\|I_{LOAD}\|$ = 0 to 1mA	3 V	−15		+15	mV
t_{ON}	Turn on time	SD16REFON = 0->1; SD16VMIDON = 1; C_{REF} = 470nF	3 V		100		µs

SD16_A， 外部参考输入

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

12位DAC 供电规范

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.20		3.60	V
I_{DD}	Supply Current (see Notes 1 and 2)	DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		50	110	µA
		DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h, $V_{REF,DAC12} = AV_{CC}$	2.2V/3V		50	110	
		DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, $V_{REF,DAC12} = AV_{CC}$	2.2V/3V		200	440	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, $V_{REF,DAC12} = AV_{CC}$	2.2V/3V		700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, $V_{REF,DAC12}$ = 1.2V ΔAV_{CC} = 100mV	2.7V		70		dB

NOTES:
1. No load at the output pin assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = $20*\log\{\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}\}$.
4. V_{REF} is applied externally. The internal reference is not used.

12位DAC 线性规格（见图12）

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2V DAC12AMPx = 7, DAC12IR = 1	2.7V		±2.0	±8.0	LSB
DNL	Differential nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2V DAC12AMPx = 7, DAC12IR = 1	2.7V		±0.4	±1.0	LSB
E_O	Offset voltage w/o calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2V DAC12AMPx = 7, DAC12IR = 1	2.7V			±20	mV
	Offset voltage with calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2V DAC12AMPx = 7, DAC12IR = 1	2.7V			±2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.7V		±30		µV/C
E_G	Gain error (see Note 1)	$V_{REF,DAC12}$ = 1.2V	2.7V			±3.50	% FSR
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.7V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx=2	2.7V			100	ms
		DAC12AMPx=3,5	2.7V			32	
		DAC12AMPx=4,6,7	2.7V			6	

NOTES:
1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first order equation: $y = a + b*x$. $V_{DAC12\_xOUT} = E_O + (1 + E_G) * (V_{REF,DAC12}/4095) * DAC12\_xDAT$, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx ={0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

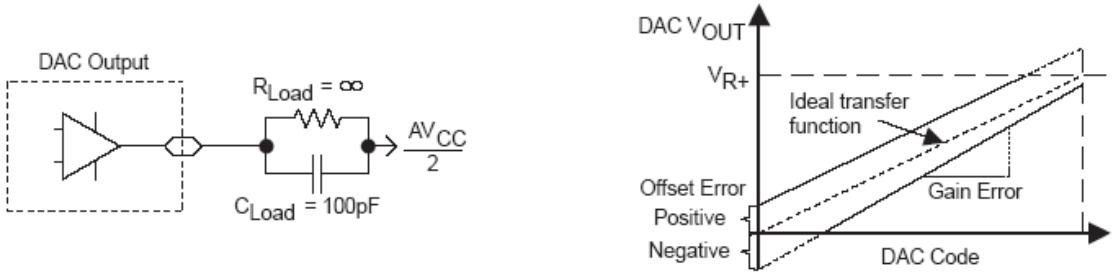


图12 线性测试负载条件和增益/偏移定义

12位DAC 线性规格（继续）

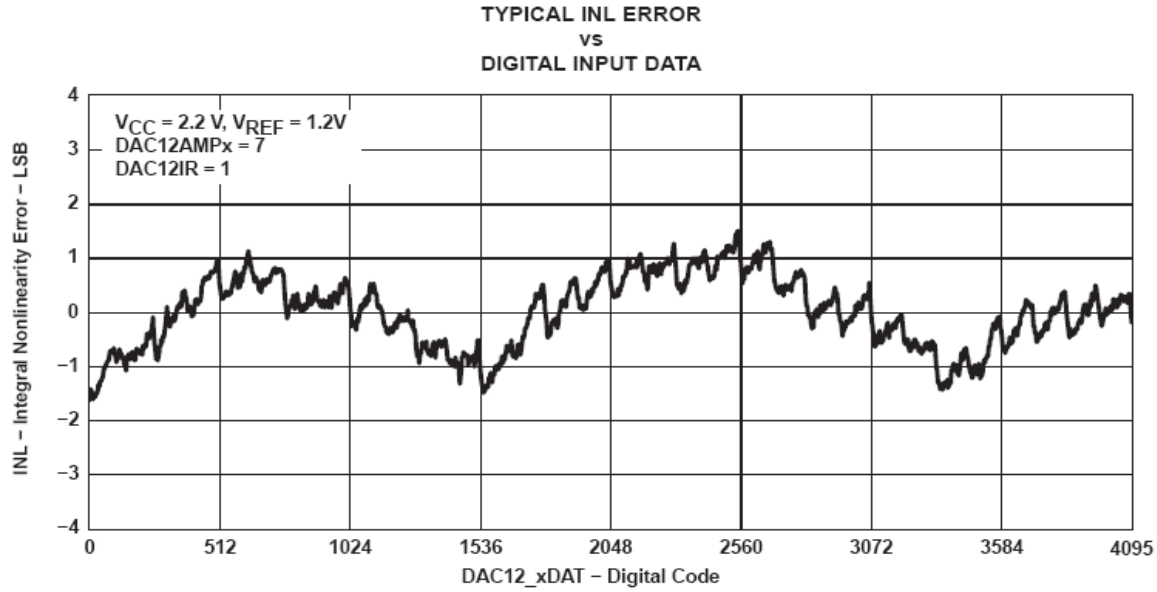


图 13

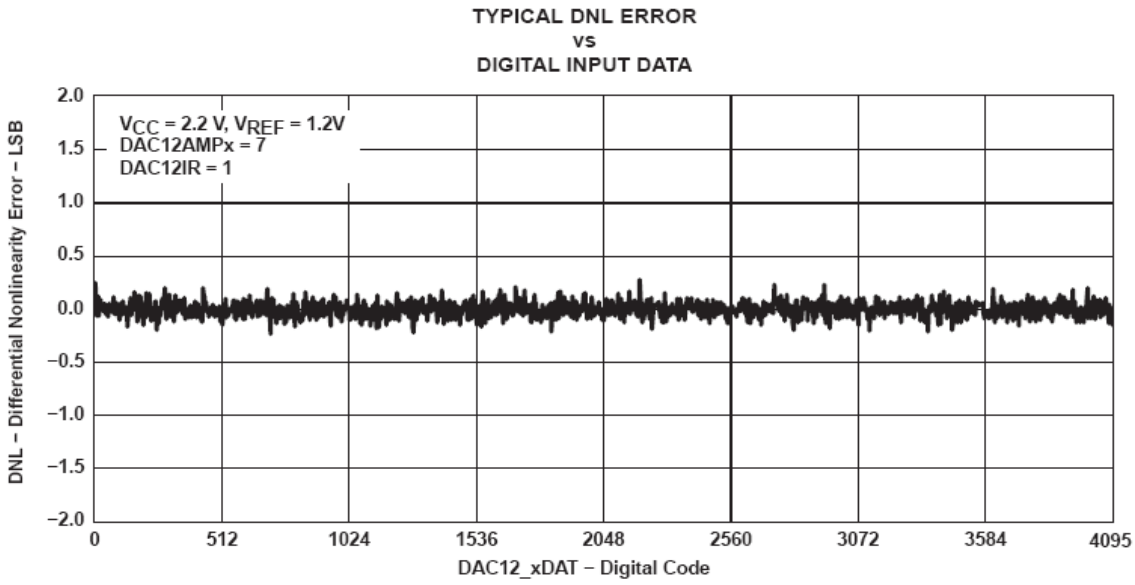


图 14

12位 DAC 输出规格

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 15)	No Load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.005	V
		No Load, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.05		AV_{CC}	
		R_{Load}= 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.1	
		R_{Load}= 3 kΩ, $V_{REF,DAC12} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.13		AV_{CC}	
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2V/3V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	−0.5		+0.5	mA
			3V	−1.0		+1.0	
$R_{O/P(DAC12)}$	Output Resistance (see Figure 15)	R_{Load}= 3 kΩ, $V_{O/P(DAC12)}$ < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2V/3V		150	250	Ω
		R_{Load}= 3 kΩ, $V_{O/P(DAC12)} > AV_{CC}$−0.3 V DAC12_xDAT = 0FFFh	2.2V/3V		150	250	
		R_{Load}= 3 kΩ, 0.3V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} − 0.3V	2.2V/3V		1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

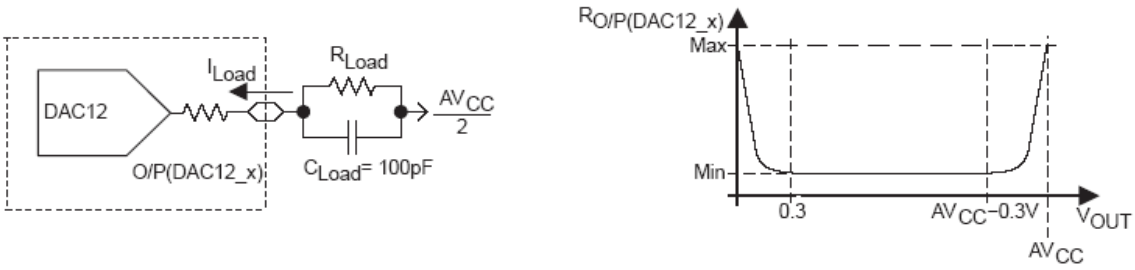


图15 DAC12_x 输出阻抗测试

12位 DAC 参考源输入规格

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Reference input voltage range	DAC12IR=0, (see Notes 1 and 2)	2.2V/3V		AV_{CC}/3	AV_{CC}+0.2	V
		DAC12IR=1, (see Notes 3 and 4)	2.2V/3V		AVcc	AVcc+0.2	
$R_{i(VREF)}$	Reference input resistance	DAC12IR=0 , (see Note 5)	2.2V/3V	20			MΩ
		DAC12IR=1	2.2V/3V	40	48	56	kΩ

NOTES:
1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{E(O)}] / [3*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $V_{REF} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
5. Characterized, not production tested

12位DAC，动态规格；$V_{REF,\ DAC12}$＝AVcc，DAC12IR＝1（见图16和图17）

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, Error$_{V(O)}$ < ±0.5 LSB (see Note 1,Figure 16)	DAC12AMPx=0 → {2, 3, 4}	2.2V/3V		60	120	µs
			DAC12AMPx=0 → {5, 6}	2.2V/3V		15	30	
			DAC12AMPx=0 → 7	2.2V/3V		6	12	
$t_{S(FS)}$	Settling time,full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		100	200	µs
			DAC12AMPx=3,5	2.2V/3V		40	80	
			DAC12AMPx=4,6,7	2.2V/3V		15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx=2	2.2V/3V		5		µs
			DAC12AMPx=3,5	2.2V/3V		2		
			DAC12AMPx=4,6,7	2.2V/3V		1		
SR	Slew Rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V	0.05	0.12		V/µs
			DAC12AMPx=3,5	2.2V/3V	0.35	0.7		
			DAC12AMPx=4,6,7	2.2V/3V	1.5	2.7		
Glitch energy: full-scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		10		nV-s
			DAC12AMPx=3,5	2.2V/3V		10		
			DAC12AMPx=4,6,7	2.2V/3V		15		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 16.
2. Slew rate applies to output voltage steps >= 200mV.

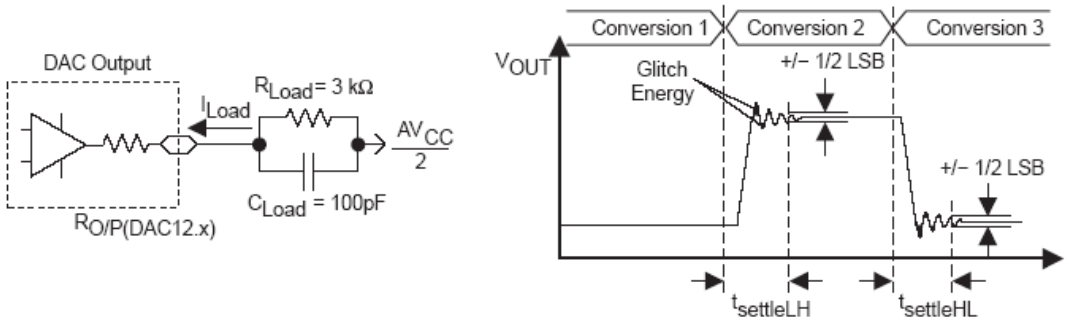


图16 建立时间和短时脉冲波形干扰测试

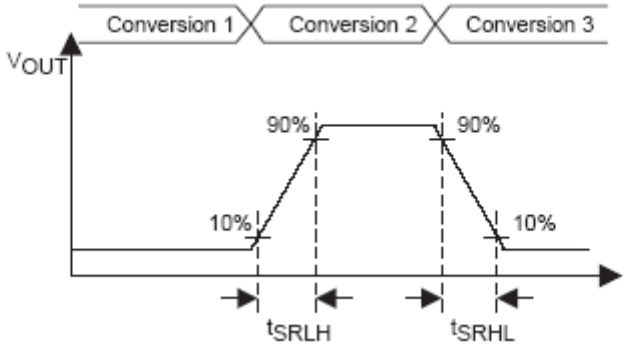


图17 回转（slew）速率测试

12位DAC，动态规格（T_A＝25℃ 除非由别的说明）

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC}=1.5V, V_{AC}=0.1V_{PP} (see Figure 18)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	550			

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

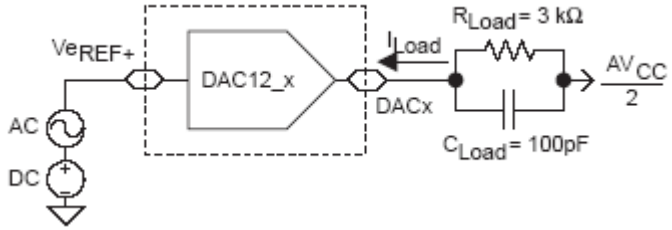


图18 3-dB带宽规格的测试条件

闪存

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.5		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.5V/3.6V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.5V/3.6V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.5V/3.6V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.5V/3.6V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64−byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine (t_{FTG} = 1/f_{FTG}).

JATG接口

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

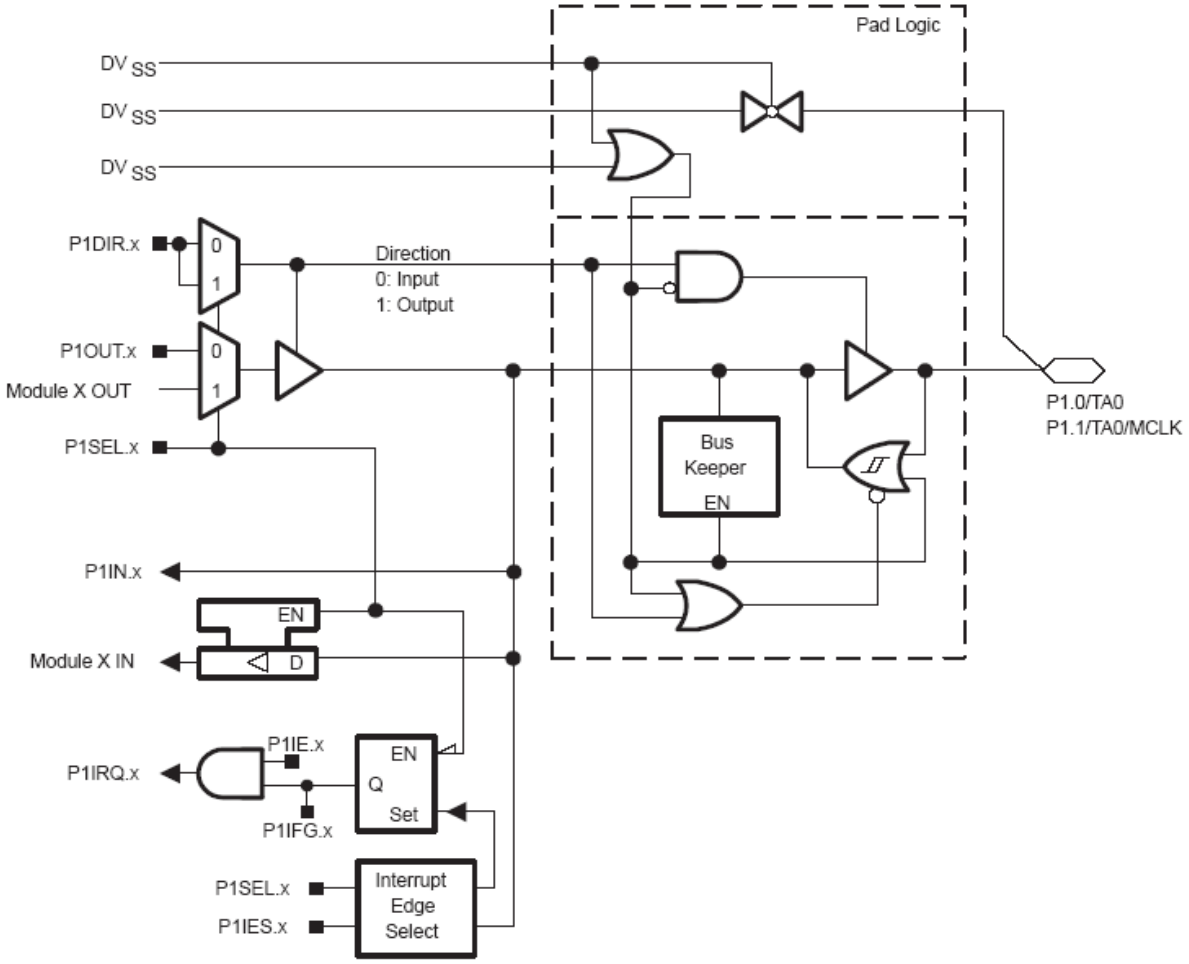
JATG熔丝（见注解1）

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

输入/输出电路原理图

端口P1,P1.0到P1.1,带施密特触发的输入/输出



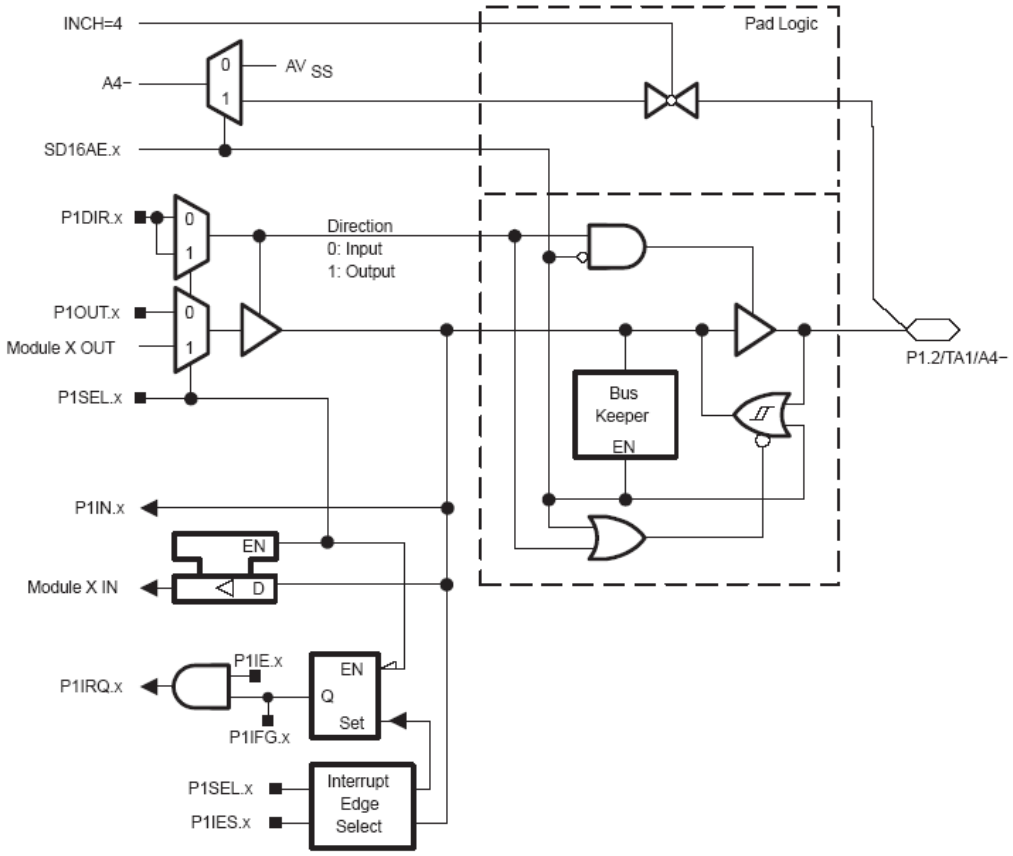
P1（P1.0,P1.1）引脚功能

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0	0	P1.0† Input/Output	0/1	0
		Timer_A3.CCI0A	0	1
		Timer_A3.TA0	1	1
P1.1/TA0/MCLK	1	P1.1† Input/Output	0/1	0
		Timer_A3.CCI0B	0	1
		MCLK	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

P1端口原理图：P1.2,带施密特触发的输入/输出和模拟功能



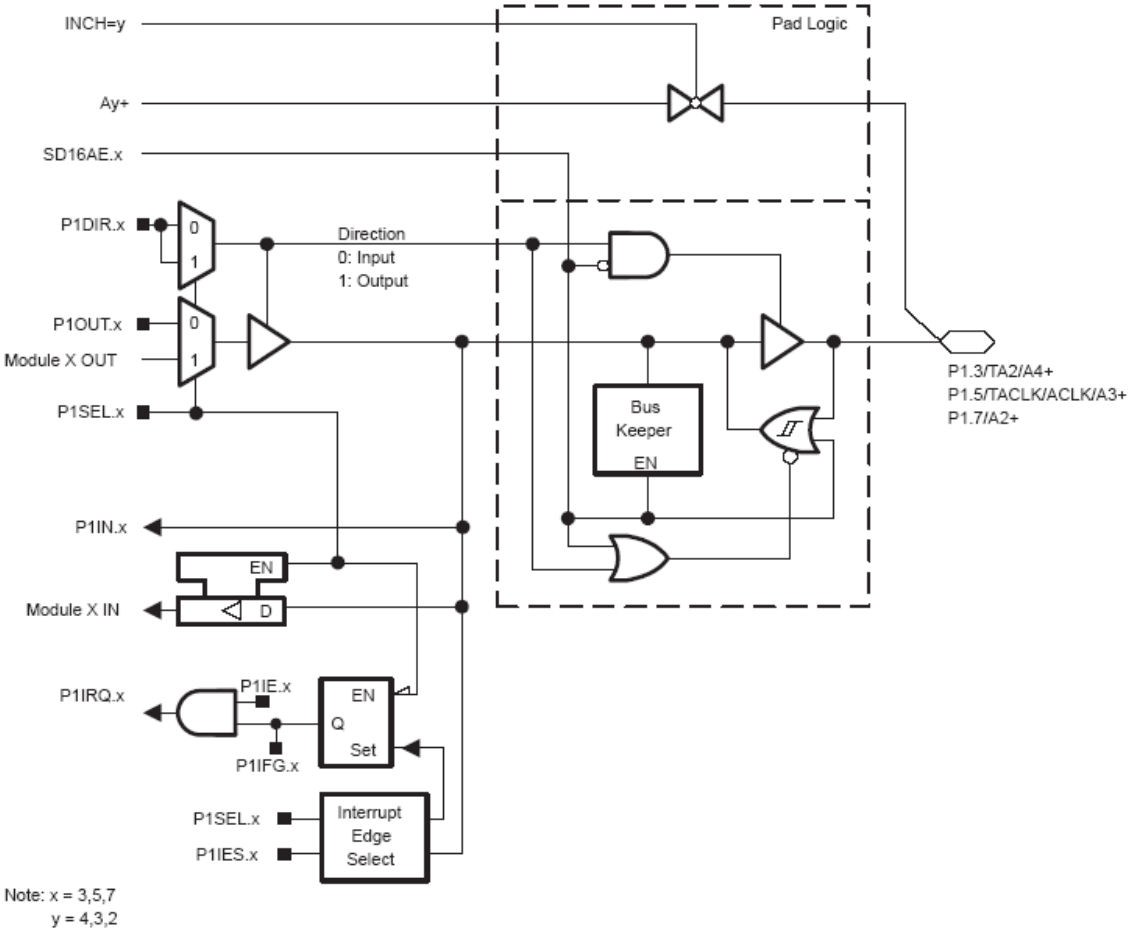
P1端口（P1.2）引脚功能

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	SD16AE.x
P1.2/TA1/A4−	2	P1.2† Input/Output	0/1	0	0
		Timer_A3.CCI1A	0	1	0
		Timer_A3.TA1	1	1	0
		A4− (see Notes 3, 4)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A4−) connected to V_{SS} if corresponding SD16AE.x bit is cleared.

P1端口原理图：P1.3，P1.5,P1.7,带施密特触发的输入/输出和模拟功能



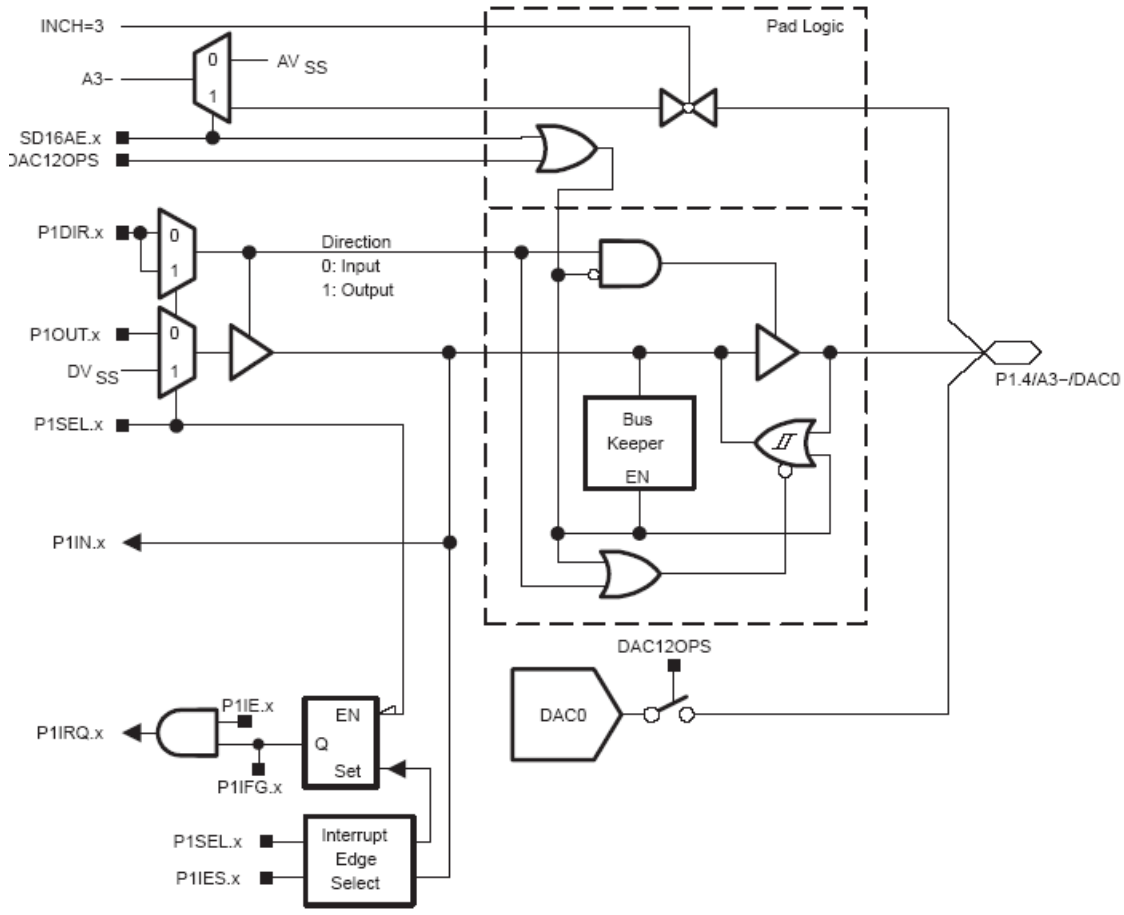
P1端口（P1.3,P1.5,P1.7）引脚功能

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	SD16AE.x
P1.3/TA2/A4+	3	P1.3† Input/Output	0/1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		A4+ (see Note 3)	X	X	1
P1.5/TACLK/ACLK/A3+	5	P1.5† Input/Output	0/1	0	0
		Timer_A3.TACLK/$\overline{\text{INCLK}}$	0	1	0
		ACLK	1	1	0
		A3+ (see Note 3)	X	X	1
P1.7/A2+	7	P1.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		A2+ (see Note 3)	X	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

P1端口原理图：P1.4,带施密特触发的输入/输出和模拟功能



Note: x = 4

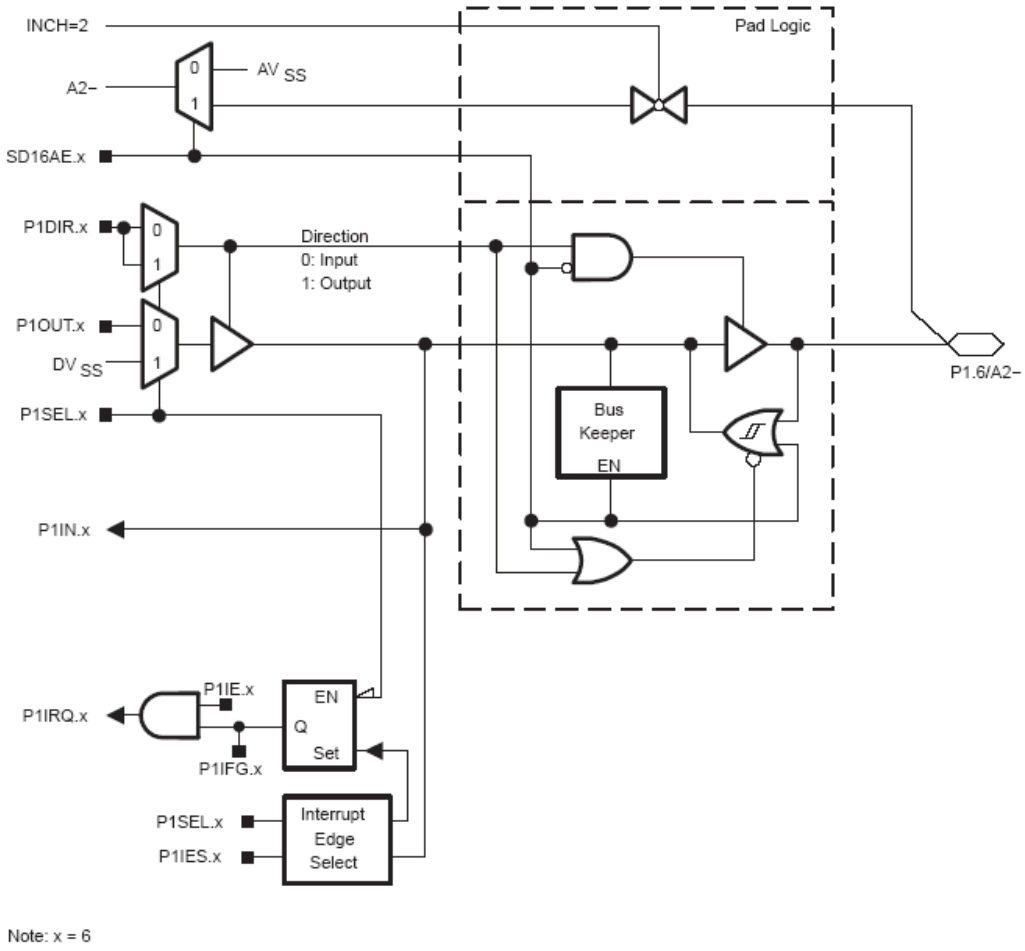
P1端口（P1.4 ）引脚功能

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	SD16AE.x	DAC12OPS
P1.4/A3−/DAC0	4	P1.4† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		DVSS	1	1	0	0
		A3− (see Notes 3, 4)	X	X	1	0
		DAC0 (see Note 5)	X	X	X	1

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A3−) connected to AV_{SS} if corresponding SD16AE.x bit is cleared.
5. Setting the DAC12OPS bit also disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

端口P1,P1.6,带施密特触发的输入/输出和模拟功能



Note: x = 6

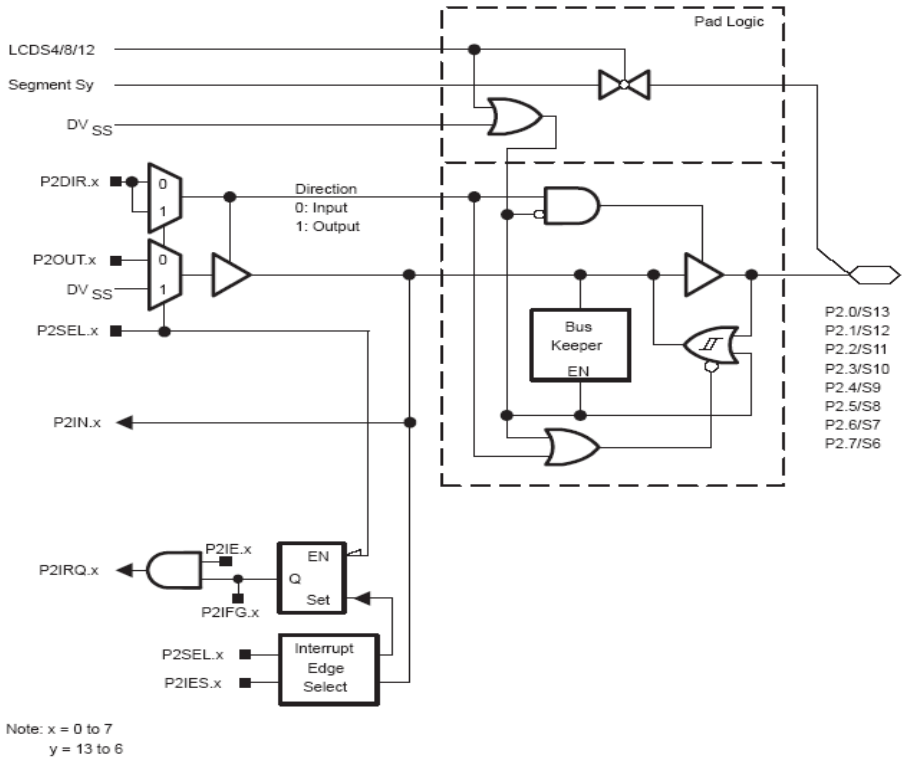
P1 端口（P1.6 ）引脚功能

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	SD16AE.x	DAC12OPS
P1.4/A3−/DAC0	4	P1.4† Input/Output	0/1	0	0	0
		N/A	0	1	0	0
		DVSS	1	1	0	0
		A3− (see Notes 3, 4)	X	X	1	0
		DAC0 (see Note 5)	X	X	X	1

† Default after reset (PUC/POR)

NOTES:
1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
4. Negative input to SD16_A (A3−) connected to AV_{SS} if corresponding SD16AE.x bit is cleared.
5. Setting the DAC12OPS bit also disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

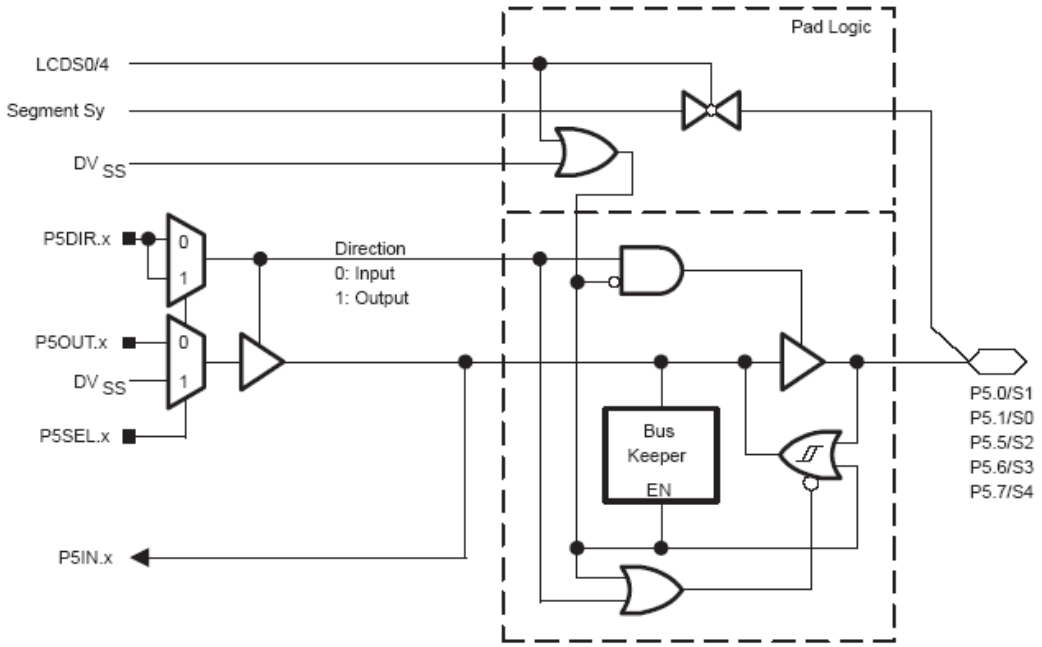
端口P2,P2.0到P2.7,带施密特触发的输入/输出,模拟功能和LCD



P2 端口（P2.0 到 P2.7 ）引脚功能

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS12
P2.0/S13	0	P2.0† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S13	X	X	1
P2.1/S12	1	P2.1† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S12	X	X	1
P2.2/S11	2	P2.2† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S11	X	X	1
P2.3/S10	3	P2.3† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S10	X	X	1
P2.4/S9	4	P2.4† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1
P2.5/S8	5	P2.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1
P2.6/S7	6	P2.6† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P2.7/S6	7	P2.7† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1

端口P5,P5.0,P5.1 P5.5到P5.7,带施密特触发的输入/输出和LCD功能



Note: x = 0,1,5,6,7
y = 1,0,2,3,4

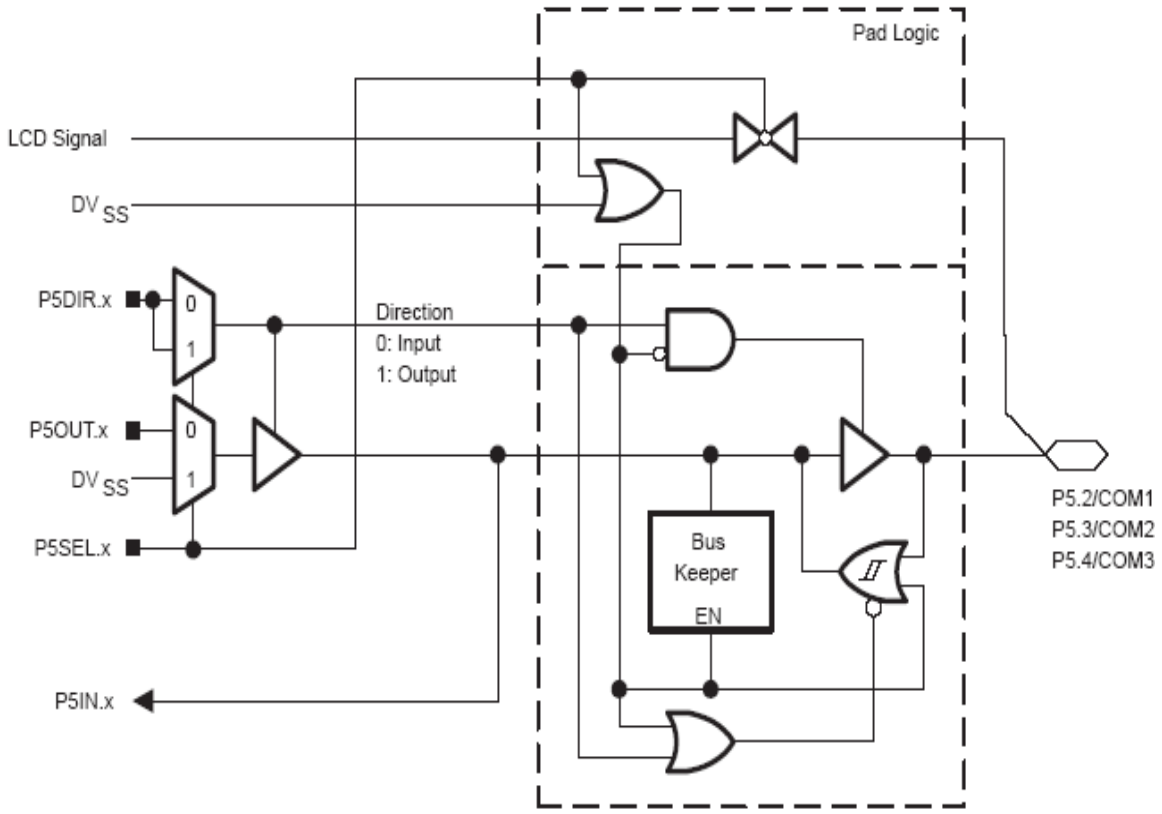
端口P5（P5.0,P5.1 P5.5，P5.6）引脚功能

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS0
P5.0/S1	0	P5.0† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S1	X	X	1
P5.1/S0	1	P5.1† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1
P5.5/S2	5	P5.5† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S2	X	X	1
P5.6/S3	6	P5.6† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S3	X	X	1

端口P5 （P5.7）引脚功能

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS4
P5.7/S4	7	P5.7† Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S4	X	X	1

端口P5, P5.2到P5.4,带施密特触发的输入/输出和LCD功能



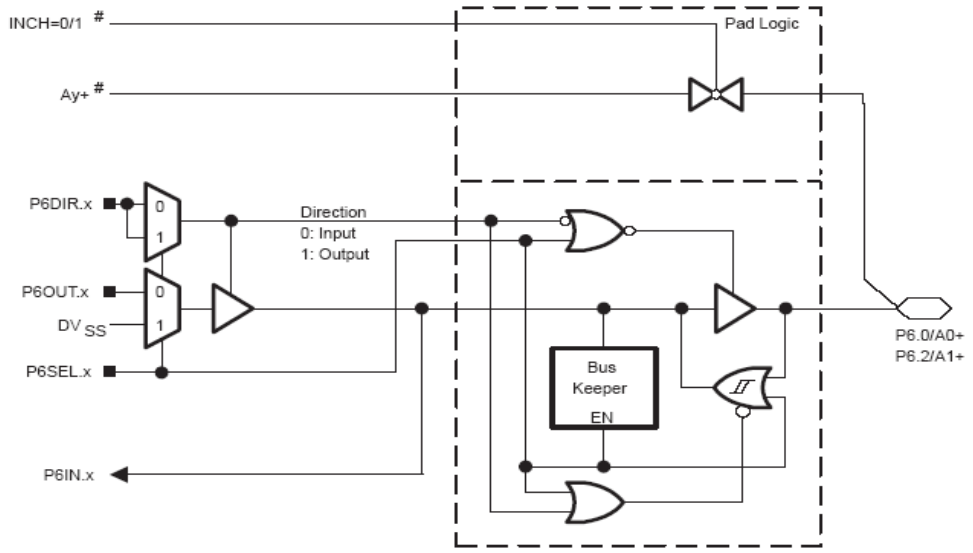
Note: x = 2 to 4

端口P5（P5.2到P5.4）引脚功能

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.2† Input/Output	0/1	0
		COM1	X	1
P5.3/COM2	3	P5.3† Input/Output	0/1	0
		COM2	X	1
P5.4/COM3	4	P5.4† Input/Output	0/1	0
		COM3	X	1

† Default after reset (PUC/POR)
NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

端口P6,P6.0,P6.2带施密特触发的输入/输出和模拟功能

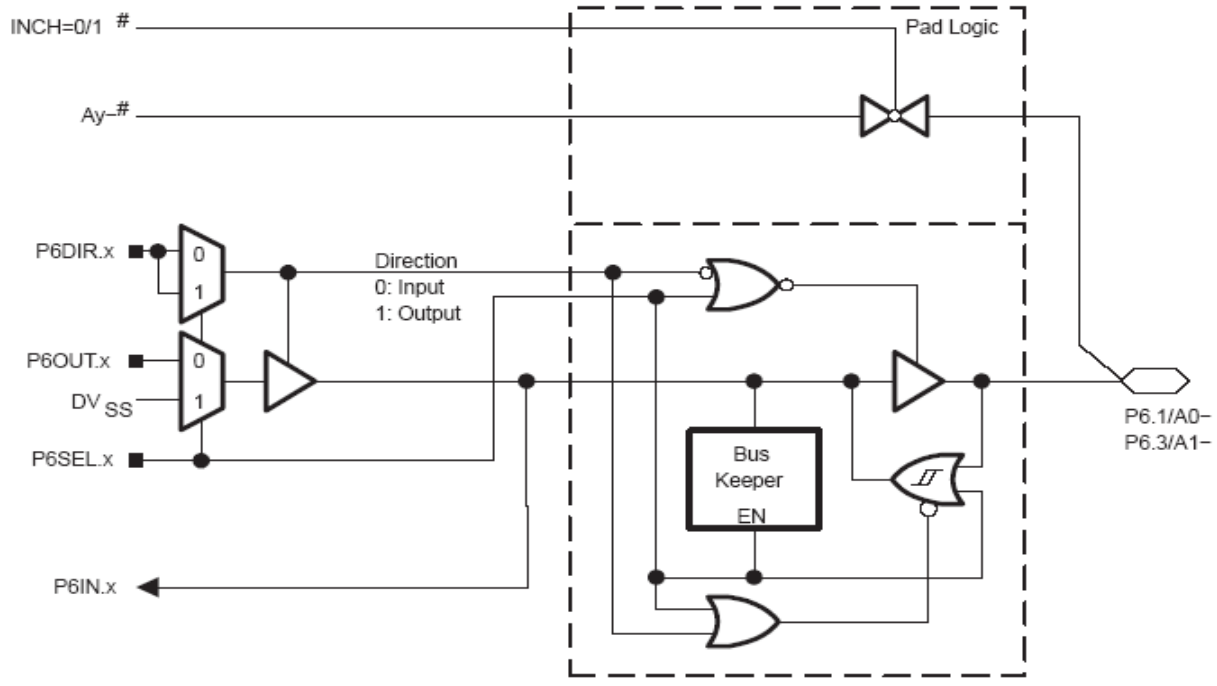


Note: x = 0,2
y = 0,1
#Signal from or to SD16

端口P6（P6.0,P6.2）引脚功能

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.0/A0+	0	P6.0† Input/Output	0/1	0
		A0+ (see Note 3)	X	1
P6.2/A1+	2	P6.2† Input/Output	0/1	0
		A1+ (see Note 3)	X	1

端口P6,P6.1,P6.3带施密特触发的输入/输出和模拟功能



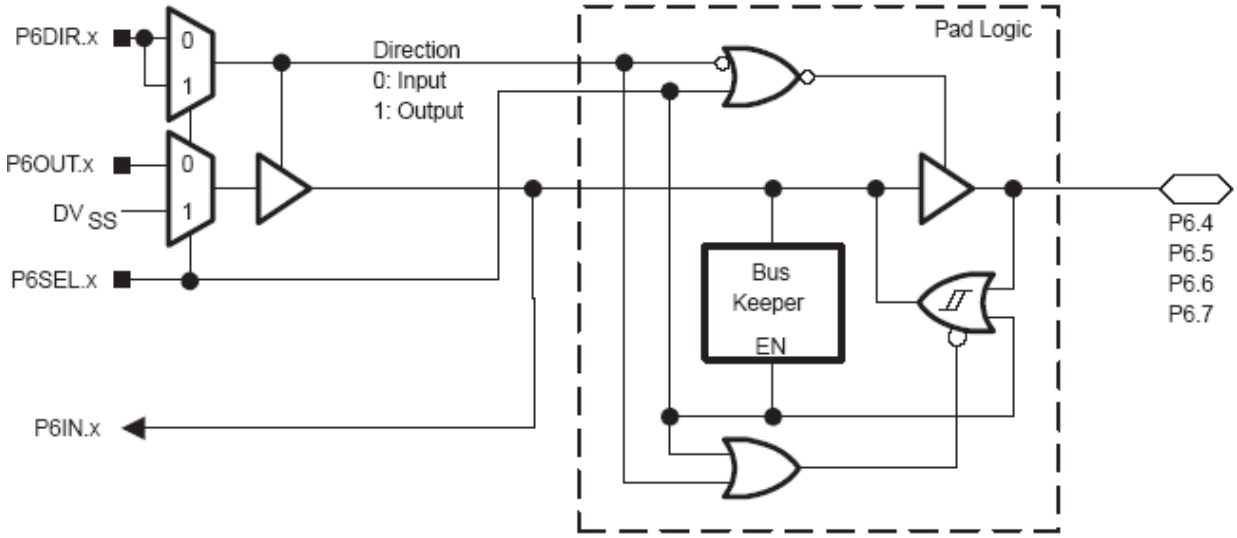
端口P6（P6.1,P6.3）引脚功能

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.1/A0−	1	P6.1† Input/Output	0/1	0
		A0− (see Note 3)	X	1
P6.3/A1−	3	P6.3† Input/Output	0/1	0
		A1− (see Note 3)	X	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

端口P6,P6.4到P6.7带施密特触发的输入/输出和模拟功能



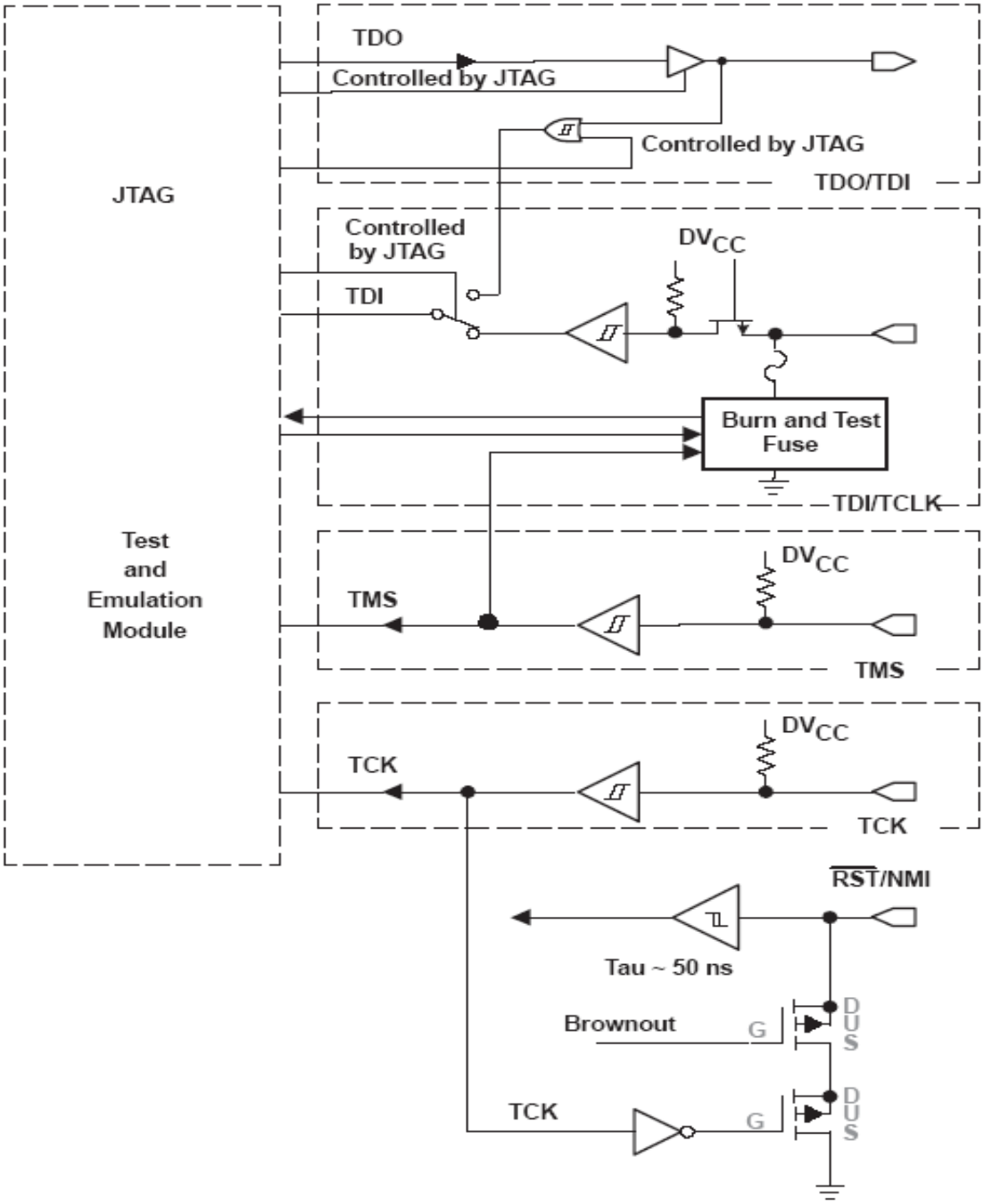
端口P6（P6.4到P6.7）引脚功能

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.4	4	P6.4† Input/Output	0/1	0
		N/A	0	1
		DVSS	1	1
P6.5	5	P6.5† Input/Output	0/1	0
		N/A	0	1
		DVSS	1	1
P6.6	6	P6.6† Input/Output	0/1	0
		N/A	0	1
		DVSS	1	1
P6.7	7	P6.7† Input/Output	0/1	0
		N/A	0	1
		DVSS	1	1

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

JTAG口 TMS，TCK，TDI/TCLK,TDO/TDI，带施密特触发的输入/输出或输出



JTAG 熔丝检查模式

在TDI引脚上具有熔丝的MSP430芯片具有熔丝检查模式，在上电复位（POR）初次操作JTAG接口时检测熔丝的通断。当被激活时，如果熔丝没有烧断一个3V1.8mA的熔丝检查电流I_{FT}将从TDI引脚流向地。必须注意避免意外激活熔丝检查模式而增加整个系统的电源损耗。

熔丝检查模式的激活发生在TMS引脚的第一个下降沿或者上电过程中TMS保持为低。TMS引脚上的第二个上升沿关闭熔丝检查模式。关闭后，熔丝检查模式保持休眠状态直到下一次POR发生。每一次POR后熔丝检查模式都有可能被激活。

熔丝检查电流仅在熔丝检查模式激活且TMS引脚为低（见图19）时才流过。JTAG引脚由内部端接，所以无需外部端接。

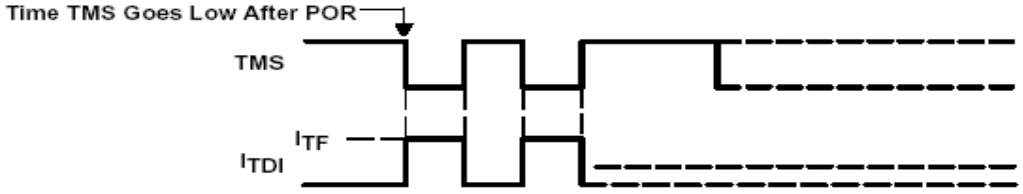
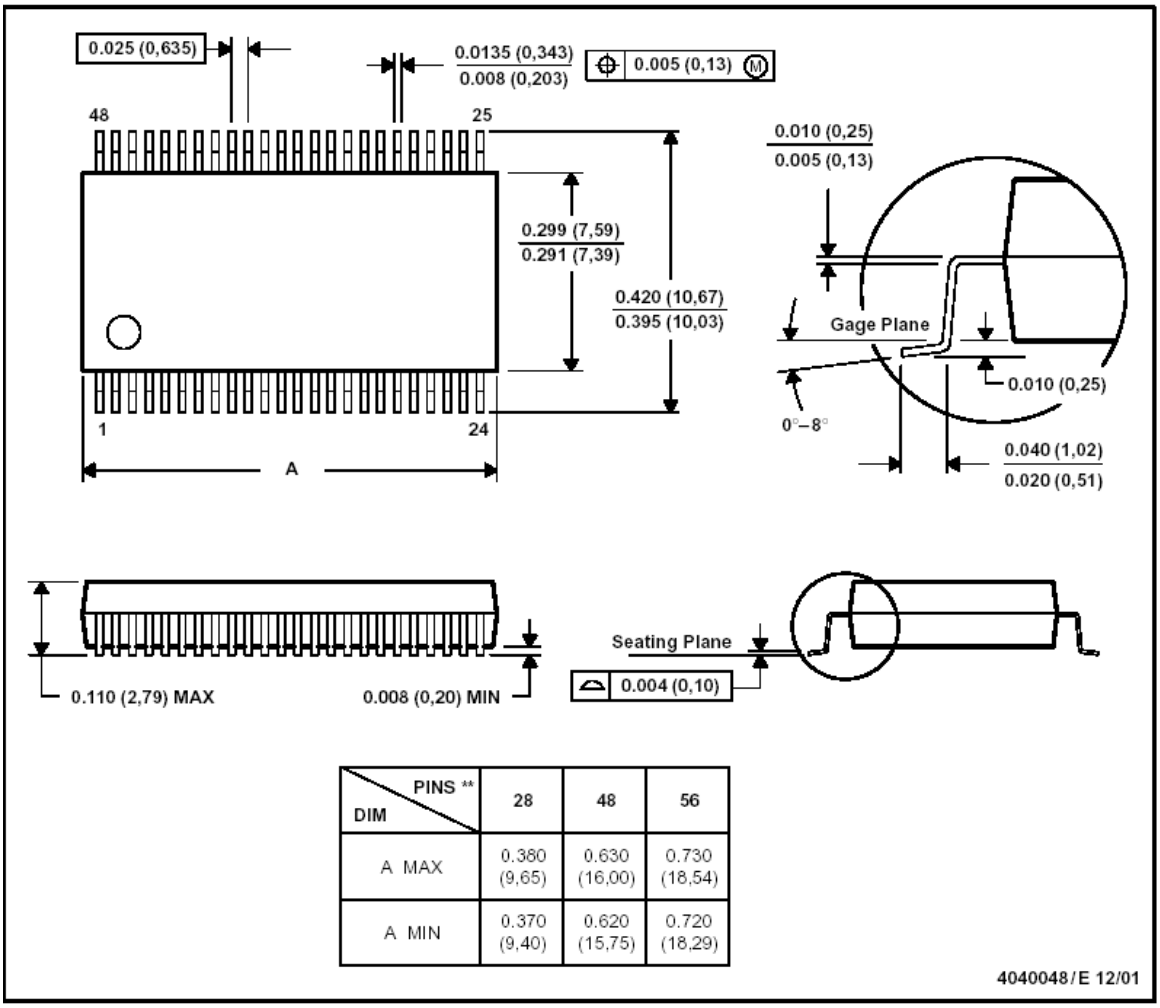


图 19 熔丝检查模式电流，MSP430F42x0

封装尺寸图

DL (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

说明：该中文资料在翻译过程中难免存在不足和错误，请依照英文资料为准。