用单片机控制TEA5768HL设计
数字调谐FM收音机

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笔者用单片机AT89S8252控制Philips公司的一款单片数字调谐FM立体声收音机芯片TEA5768/67设计了一台数字调谐FM收音机，现将设计方法介绍给读者。

TEA5768HL简介

TEA5768HL是一款适用于低电压环境（2.5～5V，典型值为3V）的单片立体声FM数字调谐收音机芯片，它集成了RF放大、变频、IF放大和鉴频等电路。用它制作的收音机，只需要很少的外围元件并且完全免调试，体积可以做得很小(若外围元件全用贴片封装，收音模块的尺寸可做到大概1.3cm×1.3cm)，由于该芯片的高集成度，节约了整机成本和设计时间。它的零售价位大概在20元左右。

该芯片灵敏度较高，其RF输入电压的典型值只有2μV，可覆盖的调频频率的范围是76～108MHz，即通过软件设置，收音机能被调谐到中国及其他一些国家的FM频段。由于内部集成了FM解调器，所以不再需要外部的鉴频器。内部的立体声解码器也是完全免调试的，为制作者带来了很大的方便。该单片收音机可以在单声道和立体声之间随意切换，并具有软静噪、立体声补偿、待机等多种功能。通过软件控制基本上可以实现设计者对立体声收音机的各方面要求。这个制作的电路原理框图如图1所示。

立体声FM数字收音机的实现

本立体声FM数字收音机的设计目标是通过MCS-51单片机的控制，实现可自动搜索并存储10个电台节目，也可手动搜索并存储。所收听电台的频率和台号可在显示模块中的LCD上显示，音量通过音量加、减按键自主控制，并能存储关机时设定的数据，左右声道音频信号通过外接的功放输出。

1．硬件实现

本设计的硬件部分由单片机控制模块、收音模块、功放模块、显示模块四部分组成。

设计的关键就在控制模块和收音模块，从图1可以看到控制模块仅仅通过I^{2}C总线与收音模块连接并控制收音机的工作。笔者选用了ATMEL公司的单片机AT89S8252对TEA5768HL进行控制，AT89S8252是一个低功耗高性能的CMOS八位微处理器，片内有8KB的FLASH和2KB的EEPROM，为电台的存储和读取带来了方便。笔者用单片机P1口的两个I/O脚来模拟I^{2}C总线的SDA和SCL的时序分别与单片收音机芯片的7脚和8脚通信。用户只需使用按键来操作收音机，MCU检测到键盘信号后通过I^{2}C总线与TEA5768HL进行通信从而实现所要求的功能，TEA5768HL输出的左右声道音频信号通过功放模块（TDA7057）输出到扬声器。具体硬件结构如图2所示。硬件技术的关键在于元件的选用和PCB的设计。

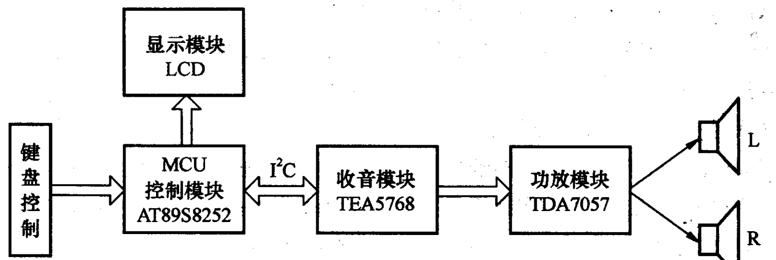


图1

2．软件设计

软件主要由初始化系统、按键循环检测、检测到某按键时实现此按键功能三部分构成。TEA5768HL芯片内部有5个功能寄存器，对收音机的控制并实现其功能就是通过I^{2}C总线读写这5个功能寄存器的值来完成的。在本设计中，这些部分都要频繁地通过I^{2}C总线与单片机通信，所以熟悉I^{2}C总线的通信协议并熟练运用非常重要，也是本设计的关键。由于要对所收到电台的频率和台号进行显示，另一个调用频繁的就是显示模块，它使用通用的LCD显示模块即可。系统的主流程图如图3所示。

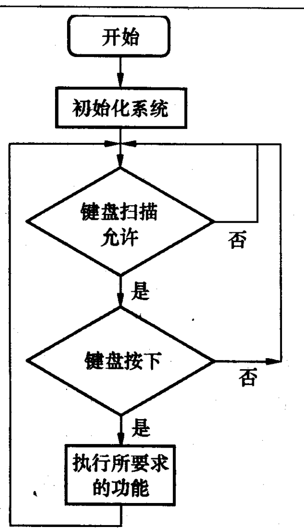


图3

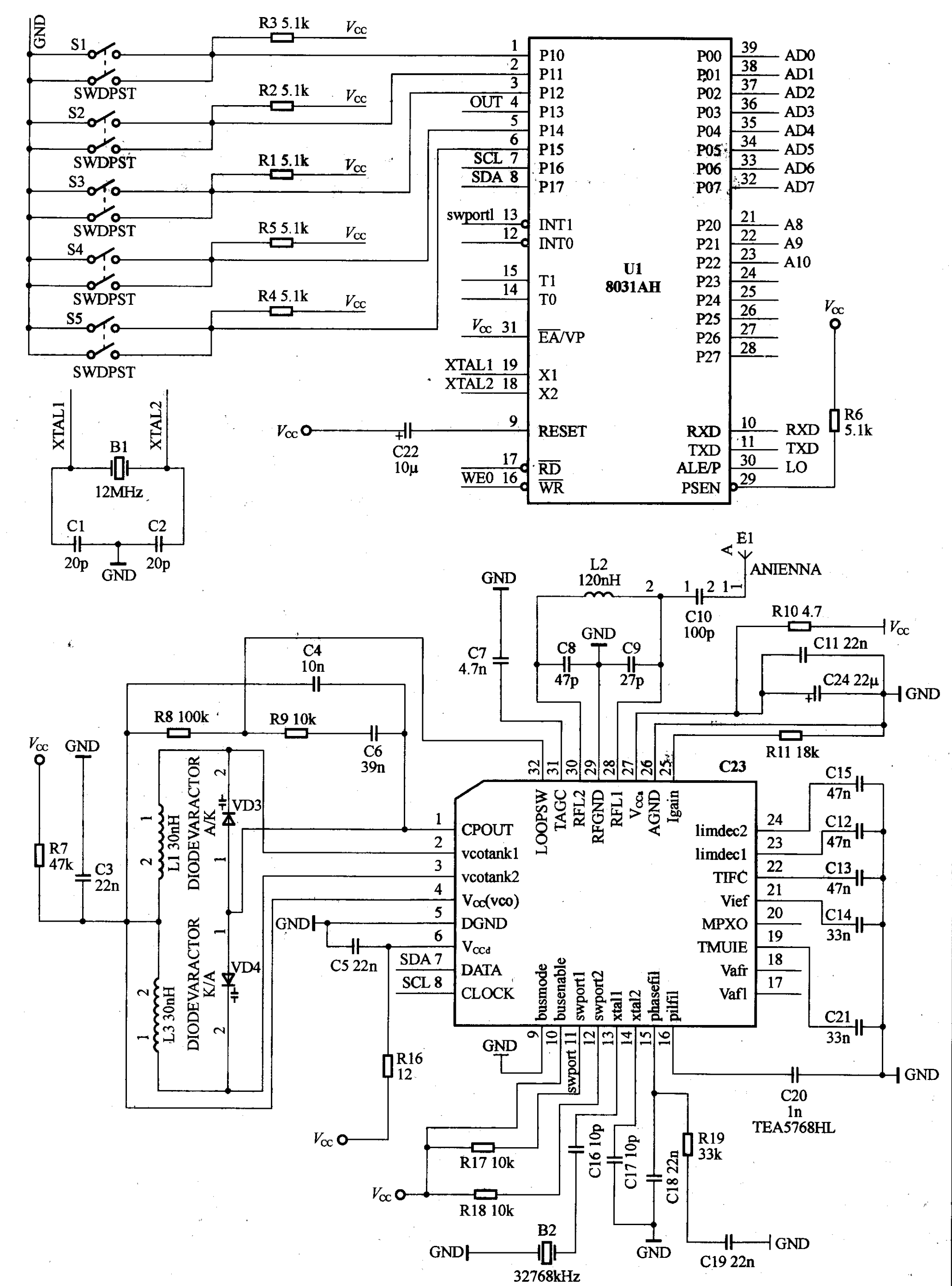


图 2 TEA5768HL 与单片机的硬件连接图

首先是初始化系统，这部分需要做的工作是对单片机里的存储单元进行合理的地址分配。对于存储电台，可根据需要在AT89S8252的片内EEPROM中开辟一定的空间，并采取一定的格式进行存储以方便取用其中的数据。然后是初始化音量，此收音机的音量是通过按键来控制的，音量的大小通过软件和硬件结合的方式来控制。最后是初始化频道，作为用户，希望一打开收音机就能听到电台，所以这一步也必不可少。

然后要进行的是按键循环检测，如基本的按键循环检测程序一样进行设计，但有效合理低成本地使用按键是我们需要考虑的问题，这时应该按照人们的一般习惯来设计按键功能。

最后也是一个主要的部分就是当检测到某个按键时，应该按照事先的设计实现其功能。在设计功能时应考虑到使用此收音机的用户群的情况，在本设计中，设计了一个只需按一个按键，即可自动的搜索并存储10个电台（可以按需要扩展个数）的功能。通过I²C总线对TEA5768中5个寄存器的读写完成了所设计的各功能，读者可以根据实际情况按照同样的方法扩展其他功能，例如静音、立体声／单声道切换等功能。

总结

以TEA5768HL为核心芯片的立体声FM数字收音机，PCB布板和硬件调试都较传统收音机简单很多，但性能可靠的硬件仍然是必须的，软件控制的关键就是MCU通过I²C总线对其内部寄存器进行控制，从而达到设计者所要求的功能。该芯片功能较齐全，而且收音效果比较好，由于该收音机的体积很小可以内嵌于手机、MP3、PDA等多种便携式产品中，而且它的制作对于高频和模拟电路经验较缺乏的爱好者也是非常适合的。

有关TEA5768HL芯片的详细资料可到www.semiconductors.philips.com/acrobat/literature/9397/75009421.pdf上查询。

CONTENTS

1 FEATURES

- High sensitivity due to integrated low-noise RF input amplifier
- FM mixer for conversion to IF of the US/Europe (87.5 to 108 MHz) and Japanese (76 to 91MHz) FM band
- Preset tuning to receive Japanese TV audio up to 108 MHz
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- FM IF selectivity performed internally
- No external discriminator needed due to fully integrated FM demodulator
- Crystal reference frequency oscillator; the oscillator operates with a 32.768 kHz clock crystal or with a 13 MHz crystal and with an externally applied 6.5 MHz reference frequency
- PLL synthesizer tuning system
- I^2C-bus
- 7-bit IF counter output via the I^2C-bus
- 4-bit level information output via the I^2C-bus
- Soft mute
- Signal dependent mono to stereo blend [Stereo Noise Cancelling (SNC)]
- Signal dependent High Cut Control (HCC)
- Soft mute, SNC and HCC can be switched off via the I^2C-bus
- Adjustment-free stereo decoder
- Autonomous search tuning function
- Standby mode
- Two software programmable ports
- Bus enable line to switch the bus input and output lines into 3-state mode
- Automotive temperature range (at V_{CCA}, $V_{CC(VCO)}$ and V_{CCD} = 5 V).

2 GENERAL DESCRIPTION

The TEA5768HL is a single-chip electronically tuned FM stereo radio for low-voltage application with fully integrated IF selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small and low cost external components. The radio can be tuned to the European, US and Japanese FM bands.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5768HL	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4 QUICK REFERENCE DATA

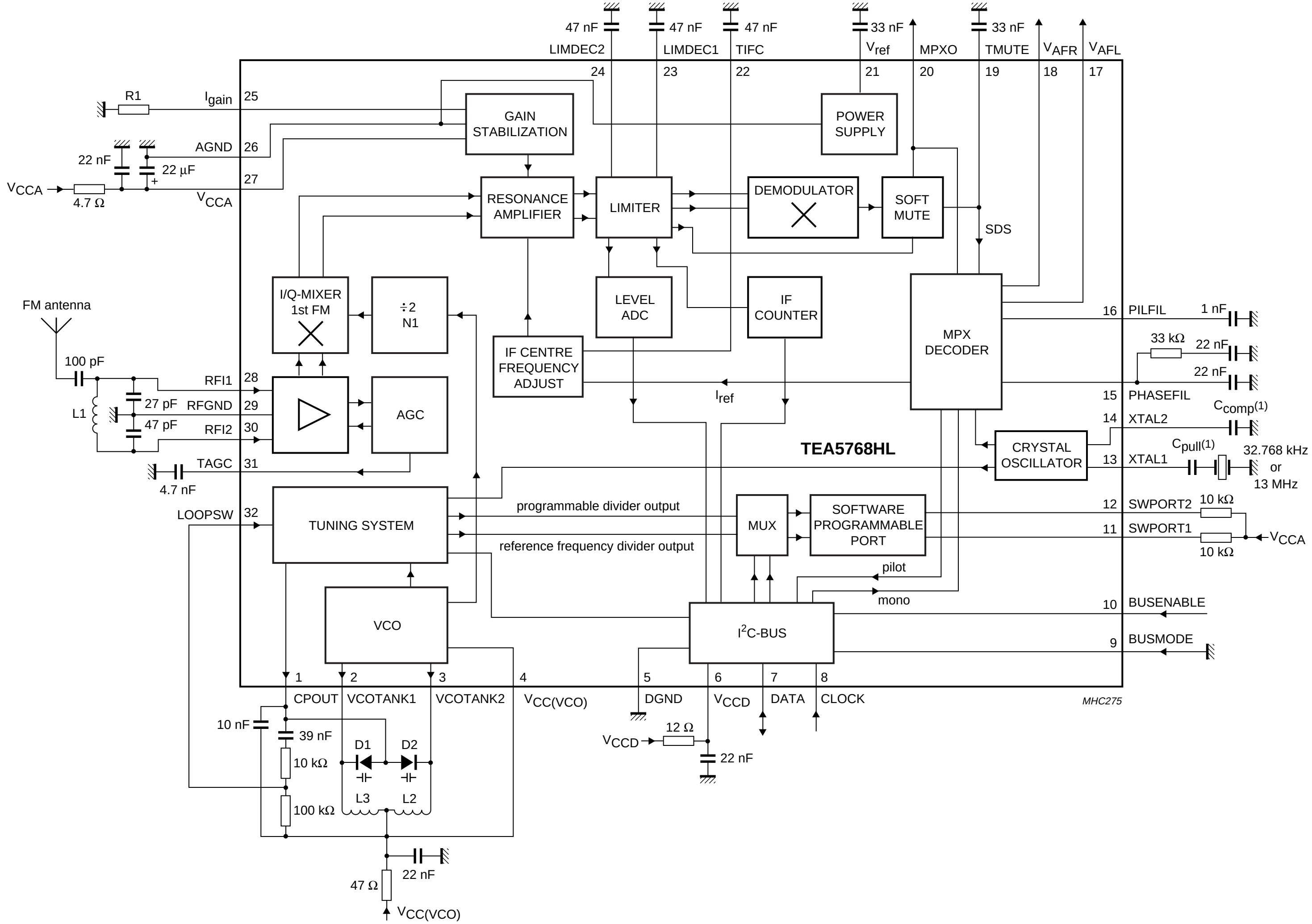
$V_{CCA} = V_{CC(VCO)} = V_{CCD}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
I_{CCA}	analog supply current	operating; V_{CCA} = 3 V	6.0	8.4	10.5	mA
		standby mode; V_{CCA} = 3 V	–	3	6	µA
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operating; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	560	750	940	µA
		standby mode; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	–	1	2	µA
I_{CCD}	digital supply current	operating; V_{CCD} = 3 V	2.1	3.0	3.9	mA
		standby mode; V_{CCD} = 3 V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
$f_{FM(ant)}$	FM input frequency		76	–	108	MHz
T_{amb}	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD}$ = 2.5 V	–10	–	+75	°C
		$V_{CCA} = V_{CC(VCO)} = V_{CCD}$ = 5 V	–40	–	+85	°C
FM overall system parameters; see Fig.5						
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 µs; L = R; B_{AF} = 300 Hz to 15 kHz	–	2	3.5	µV
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{RF} = 76 to 108 MHz; note 1	32	36	–	dB
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{RF} = 76 to 108 MHz; note 1	39	43	–	dB
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.4	1	%

Note

1. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.

5 BLOCK DIAGRAM



The component list is given Chapter 14.

(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
CPOUT	1	charge pump output of synthesizer PLL
VCOTANK1	2	voltage controlled oscillator tuned circuit output 1
VCOTANK2	3	voltage controlled oscillator tuned circuit output 2
$V_{CC(VCO)}$	4	voltage controlled oscillator supply voltage
DGND	5	digital ground
V_{CCD}	6	digital supply voltage
DATA	7	bus data line input/output
CLOCK	8	bus clock line input
BUSMODE	9	bus mode select input
BUSENABLE	10	bus enable input
SWPORT1	11	software programmable port 1
SWPORT2	12	software programmable port 2
XTAL1	13	crystal oscillator input 1
XTAL2	14	crystal oscillator input 2
PHASEFIL	15	phase detector loop filter
PILFIL	16	pilot detector low-pass filter
V_{AFL}	17	left audio frequency output voltage
V_{AFR}	18	right audio frequency output voltage
TMUTE	19	time constant for soft mute
MPXO	20	FM demodulator MPX signal output
V_{ref}	21	reference voltage
TIFC	22	time constant for IF centre adjust
LIMDEC1	23	decoupling IF limiter 1
LIMDEC2	24	decoupling IF limiter 2
I_{gain}	25	gain control current for IF filter
AGND	26	analog ground
V_{CCA}	27	analog supply voltage
RFI1	28	RF input 1
RFGND	29	RF ground
RFI2	30	RF input 2
TAGC	31	time constant RF AGC
LOOPSW	32	switch output of synthesizer PLL loop filter

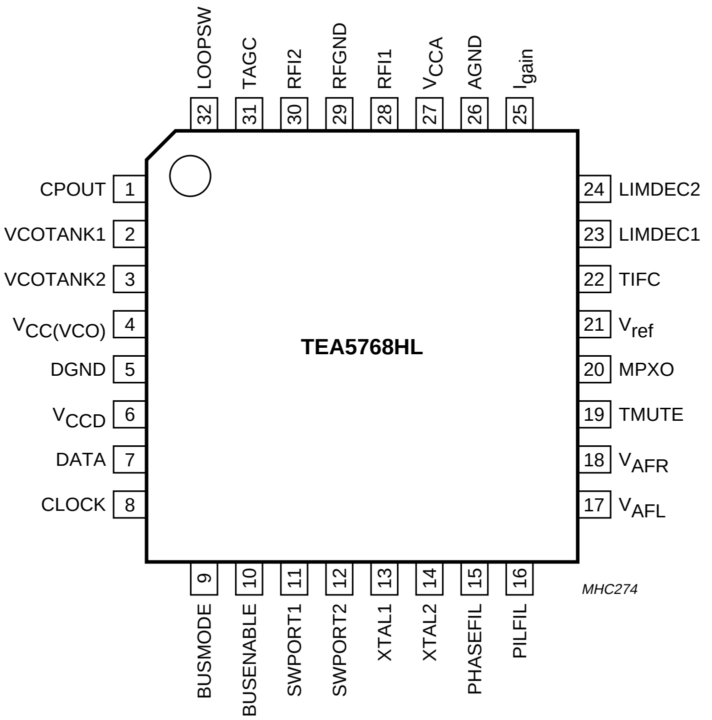


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Low-noise RF amplifier

The LNA input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

7.2 FM mixer

The FM quadrature mixer converts the FM RF (76 to 108 MHz) to an IF of 225 kHz.

7.3 VCO

The varactor tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 to 217 MHz.

7.4 Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or a 13 MHz crystal. The temperature drift of standard 32.768 kHz clock crystals limits the operational temperature range from –10 to +60 °C.

The PLL synthesizer can be clocked externally with a 32.768 kHz, a 6.5 MHz or a 13 MHz signal via pin XTAL2.

The crystal oscillator generates the reference frequency for:

- The reference frequency divider for the synthesizer PLL
- The timing for the IF counter
- The free-running frequency adjustment of the stereo decoder VCO
- The centre frequency adjustment of the IF filters.

7.5 PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz or a 13 MHz reference frequency generated by the crystal oscillator or applied to the IC from an external source. The synthesizer can also be clocked via pin XTAL2 at 6.5 MHz. The PLL tuning system can perform an autonomous search tuning function.

7.6 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

项目开发 芯片解密 零件配单 TEL:15013652265 QQ:38537442

7.7 IF filter

Fully integrated IF filter.

7.8 FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

7.9 Level voltage generator and analog-to-digital converter

The FM IF analog level voltage is converted to 4 bits digital data and output via the I²C-bus.

7.10 IF counter

The IF counter outputs a 7-bit count result via the I²C-bus.

7.11 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels. The soft mute function can be switched off via the I²C-bus.

7.12 MPX decoder

The PLL stereo decoder is adjustment-free. The stereo decoder can be switched to mono via the I²C-bus.

7.13 Signal dependent mono to stereo blend

With a decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono to stereo blend can also be programmed via the I²C-bus to an RF level depending switched mono to stereo transition. Stereo Noise Cancelling (SNC) can be switched off via the I²C-bus.

7.14 Signal dependent AF response

The audio bandwidth will be reduced with a decreasing RF input level. The function can be switched off via the I²C-bus.

7.15 Software programmable ports

Two software programmable ports (open-collector) can be addressed via the I²C-bus.

The port 1 (pin SWPORT1) function can be changed with write data byte 4 bit 0 (see Table 13). Pin SWPORT1 is then output for the ready flag of read byte 1.

8 I²C-BUS AND BUS-CONTROLLED FUNCTIONS

8.1 I²C-bus specification

Information about the I²C-bus can be found in the brochure *“The I²C-bus and how to use it”* (order number 9398 393 40011).

The standard I²C-bus specification is expanded by the following definitions.

IC address C0: 1100000.

Structure of the I²C-bus logic: slave transceiver.

Subaddresses are not used.

The maximum LOW-level input and the minimum HIGH-level input are specified to $0.2V_{CCD}$ and $0.45V_{CCD}$ respectively.

The pin BUSMODE must be connected to ground.

Note: The bus operates at a maximum clock frequency of 400 kHz. It is not allowed to connect the IC to a bus operating at a higher clock rate.

8.1.1 DATA TRANSFER

Data sequence: address, byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order). The LSB = 0 of the address indicates a WRITE operation to the TEA5768HL.

Bit 7 of each byte is considered as the MSB and has to be transferred as the first bit of the byte.

The data becomes valid bitwise at the appropriate falling edge of the clock. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started.

The IC can be switched into a low current standby mode with the standby bit; the bus is then still active. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the standby mode being programmed, the IC maintains normal operation, but is isolated from the bus lines.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.1.2 POWER-ON RESET

At Power-on reset the mute is set, all other bits are set to LOW. To initialize the IC all bytes have to be transferred.

8.2 I^{2}C-bus protocol

Table 1 Write mode

S(1)	address (write)	A(2)	data byte(s)	A(2)	P(3)

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

S(1)	address (read)	A(2)	data byte 1

Notes

1. S = START condition.
2. A = acknowledge.

Table 3 IC address byte

IC ADDRESS							**MODE**
1	1	0	0	0	0	0	R/$\overline{W}$(1)

Note

1. Read or write mode:
   a) 0 = write operation to the TEA5768HL
   b) 1 = read operation from the TEA5768HL.

8.3 Writing data

Table 4 Write mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 5 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted
6	SM	**Search Mode:** if SM = 1 then in search mode; if SM = 0 then not in search mode
5 to 0	PLL[13:8]	setting of synthesizer programmable counter for search or preset

Table 7 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	setting of synthesizer programmable counter for search or preset

Table 9 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	ML	MR	SWP1

Table 10 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	SUD	**Search Up/Down:** if SUD = 1 then search up; if SUD = 0 then search down
6 and 5	SSL[1:0]	**Search Stop Level:** see Table 11
4	HLSI	**HIGH/LOW Side Injection:** if HLSI = 1 then HIGH side LO injection; if HLSI = 0 then LOW side LO injection
3	MS	**Mono to Stereo:** if MS = 1 then forced mono; if MS = 0 then stereo ON
2	ML	**Mute Left:** if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted
1	MR	**Mute Right:** if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted
0	SWP1	**Software programmable port 1:** if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW

Table 11 Search stop level setting

SSL1	SSL0	SEARCH STOP LEVEL
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

Table 12 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

Table 13 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7	SWP2	**Software programmable port 2:** if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW
6	STBY	**Standby:** if STBY = 1 then in standby mode; if STBY = 0 then not in standby mode
5	BL	**Band Limits:** if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band
4	XTAL	if XTAL = 1 then f_{xtal} = 32.768 kHz; if XTAL = 0 then f_{xtal} = 13 MHz
3	SMUTE	**Soft MUTE:** if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF
2	HCC	**High Cut Control:** if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF
1	SNC	**Stereo Noise Cancelling:** if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF
0	SI	**Search Indicator:** if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1

Table 14 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLLREF	DTC	–	–	–	–	–	–

Table 15 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7	PLLREF	if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled
6	DTC	if DTC = 1 then the de-emphasis time constant is 75 µs; if DTC = 0 then the de-emphasis time constant is 50 µs
5 to 0	–	not used; position is don’t care

8.4 Reading data

Table 16 Read mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 17 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 18 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	RF	**Ready Flag:** if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found
6	BLF	**Band Limit Flag:** if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached
5 to 0	PLL[13:8]	setting of synthesizer programmable counter after search or preset

Table 19 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 20 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	setting of synthesizer programmable counter after search or preset

Table 21 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 22 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	STEREO	**Stereo indication:** if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception
6 to 0	PLL[13:8]	IF counter result

Table 23 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 24 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 4	LEV[3:0]	level ADC output
3 to 1	CI[3:1]	**Chip Identification:** these bits have to be set to logic 0
0	–	this bit is internally set to logic 0

Table 25 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	0	0	0	0	0	0	0

Table 26 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	–	reserved for future extensions; these bits are internally set to logic 0

8.5 Bus timing

Table 27 Digital levels and timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Digital inputs					
V_{IH}	HIGH-level input voltage		$0.45V_{CCD}$	–	V
V_{IL}	LOW-level input voltage		–	$0.2V_{CCD}$	V
Digital outputs					
$I_{sink(L)}$	LOW-level sink current		500	–	μA
V_{OL}	LOW-level output voltage	I_{OL} = 500 μA	–	450	mV
Timing (I^2C-bus enabled)					
f_{clk}	clock input frequency		–	400	kHz
t_{HIGH}	clock HIGH time		1	–	μs
t_{LOW}	clock LOW time		1	–	μs

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		–0.3	+8	V
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		–0.3	+8	V
V_{CCD}	digital supply voltage		–0.3	+5	V
V_{CCA}	analog supply voltage		–0.3	+8	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage				
	for all pins except pin DATA	note 1	–200	+200	V
		note 2	–2000	+2000	V
	for pin DATA	note 1	–150	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model (R = 0 Ω, C = 200 pF).
2. Human body model (R = 1.5 kΩ, C = 100 pF).

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	80	K/W

11 DC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltages						
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
Supply currents						
I_{CCA}	analog supply current	operating				
		$V_{CCA} = 3$ V	6.0	8.4	10.5	mA
		$V_{CCA} = 5$ V	6.2	8.6	10.7	mA
		standby mode				
		$V_{CCA} = 3$ V	–	3	6	μA
		$V_{CCA} = 5$ V	–	3.2	6.2	μA
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operating				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	560	750	940	μA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	570	760	950	μA
		standby mode				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	–	1	2	μA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	–	1.2	2.2	μA
I_{CCD}	digital supply current	operating				
		$V_{CCD} = 3$ V	2.1	3.0	3.9	mA
		$V_{CCD} = 5$ V	2.25	3.15	4.05	mA
		standby mode; $V_{CCD} = 3$ V				
		bus enable line HIGH	30	56	80	μA
		bus enable line LOW	11	19	26	μA
		standby mode; $V_{CCD} = 5$ V				
		bus enable line HIGH	50	78	105	μA
		bus enable line LOW	20	33	45	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC operating points						
V_{CPOUT}	unloaded DC voltage		0.1	–	$V_{CC(VCO)} - 0.1$	V
V_{XTAL1}		data byte 4 bit 4 = 1	1.64	1.72	1.8	V
		data byte 4 bit 4 = 0	1.68	1.75	1.82	V
V_{XTAL2}		data byte 4 bit 4 = 1	1.64	1.72	1.8	V
		data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$			0.4	1.2	$V_{CCA} - 0.4$	V
V_{PILFIL}			0.65	0.9	1.3	V
V_{VAFL}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{VAFR}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{TMUTE}		V_{RF} = 0 V	1.5	1.65	1.8	V
V_{MPXO}		f_{RF} = 98 MHz; V_{RF} = 1 mV	680	815	950	mV
V_{Vref}			1.45	1.55	1.65	V
V_{TIFC}			1.34	1.44	1.54	V
$V_{LIMDEC1}$			1.86	1.98	2.1	V
$V_{LIMDEC2}$			1.86	1.98	2.1	V
V_{Igain}			480	530	580	mV
V_{RFI1}			0.93	1.03	1.13	V
V_{RFI2}			0.93	1.03	1.13	V
V_{TAGC}		V_{RF} = 0 V	1	1.57	2	V

12 AC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD}$ = 2.7 V; T_{amb} = 25 °C; measured in the circuit of Fig.5; all AC values are given in RMS; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f_{osc}	oscillator frequency		150	–	217	MHz
Crystal oscillator						
CIRCUIT INPUT: PIN XTAL2						
$V_{i(osc)}$	oscillator input voltage	oscillator externally clocked	140	–	350	mV
R_i	input resistance	oscillator externally clocked				
		data byte 4 bit 4 = 0	2	3	4	kΩ
		data byte 4 bit 4 = 1	230	330	430	kΩ
C_i	input capacitance	oscillator externally clocked				
		data byte 4 bit 4 = 0	3.9	5.6	7.3	pF
		data byte 4 bit 4 = 1	5	6	7	pF
CRYSTAL: 32.768 kHz						
f_r	series resonance frequency	data byte 4 bit 4 = 1	–	32.768	–	kHz
$\Delta f/f_r$	frequency deviation		-20×10^{-6}	–	$+20 \times 10^{-6}$	
C_0	shunt capacitance		–	–	3.5	pF
R_S	series resistance		–	–	80	kΩ
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	$-10\ °C < T_{amb} < +60\ °C$	-50×10^{-6}	–	$+50 \times 10^{-6}$	
CRYSTAL: 13 MHz						
f_r	series resonance frequency	data byte 4 bit 4 = 0	–	13	–	MHz
$\Delta f/f_r$	frequency deviation		-30×10^{-6}	–	$+30 \times 10^{-6}$	
C_0	shunt capacitance		–	–	4.5	pF
C_{mot}	motional capacitance		1.5	–	3.0	fF
R_S	series resistance		–	–	100	Ω
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	$-40\ °C < T_{amb} < +85\ °C$	-30×10^{-6}	–	$+30 \times 10^{-6}$	
Synthesizer						
PROGRAMMABLE DIVIDER						
N_{prog}	programmable divider ratio	data byte 1 = XX111111; data byte 2 = 11111111	–	–	8191	
		data byte 1 = XX010000; data byte 2 = 00000000	2048	–	–	
ΔN_{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio	data byte 4 bit 4 = 0	–	260	–	
		data byte 5 bit 7 = 1; data byte 4 bit 4 = 0	–	130	–	
		data byte 4 bit 4 = 1	–	1	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PIN CPOUT						
I_{sink}	charge pump peak sink current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ – 0.2 V; $f_{VCO} > f_{ref} \times N_{prog}$	–	0.5	–	µA
I_{source}	charge pump peak source current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ – 0.2 V; $f_{VCO} < f_{ref} \times N_{prog}$	–	–0.5	–	µA
IF counter						
V_{RF}	RF input voltage for correct IF count		–	12	18	µV
N_{IF}	IF counter length		–	7	–	bit
$N_{precount}$	IF counter prescaler ratio		–	64	–	
$T_{count(IF)}$	IF counter period	f_{xtal} = 32.768 kHz	–	15.625	–	ms
		f_{xtal} = 13 MHz	–	15.754	–	ms
$RES_{count(IF)}$	IF counter resolution	f_{xtal} = 32.768 kHz	–	4.096	–	kHz
		f_{xtal} = 13 MHz	–	4.0625	–	kHz
IF_{count}	IF counter result for search tuning stop	f_{xtal} = 32.768 kHz	31	–	3E	HEX
		f_{xtal} = 13 MHz	32	–	3D	HEX
Pins DATA, CLOCK, BUSMODE and BUSENABLE						
R_i	input resistance		10	–	–	MΩ
Software programmable ports						
PIN SWPORT1						
$I_{sink(max)}$	maximum sink current	data byte 4 bit 0 = 0; data byte 5 bit 0 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	µA
$I_{leak(max)}$	maximum leakage current	data byte 4 bit 0 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	µA
PIN SWPORT2						
$I_{sink(max)}$	maximum sink current	data byte 5 bit 7 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	µA
$I_{leak(max)}$	maximum leakage current	data byte 5 bit 1 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	µA
FM signal channel						
FM RF INPUT						
R_i	input resistance at pins RFI1 and RFI2 to RFGND		75	100	125	Ω
C_i	input capacitance at pins RFI1 and RFI2 to RFGND)		2.5	4	6	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	–	2	3.5	μV
$IP3_{in}$	in-band 3rd-order intercept point related to $V_{RFI1-RFI2}$ (peak value)	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tune} = 76 to 108 MHz	81	84	–	dBμV
$IP3_{out}$	out-band 3rd-order intercept point related to $V_{RFI1-RFI2}$ (peak value)	Δf_1 = 4 MHz; Δf_2 = 8 Hz; f_{tune} = 76 to 108 MHz	82	85	–	dBμV
RF AGC						
V_{RF1}	RF input voltage for start of AGC	f_{RF1} = 93 MHz; f_{RF2} = 98 MHz; V_{RF2} = 50 dBμV; $\left\lvert\frac{\Delta V_{TMUTE}}{V_{RF1}}\right\rvert < \frac{14\ mV}{3\ dB\mu V}$; note 1	66	72	78	dBμV
IF filter						
f_{IF}	IF filter centre frequency		215	225	235	kHz
B_{IF}	IF filter bandwidth		85	94	102	kHz
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{tune} = 76 to 108 MHz; note 2	39	43	–	dB
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{tune} = 76 to 108 MHz; note 2	32	36	–	dB
S_{+100}	HIGH side 100 kHz selectivity	Δf = +100 kHz; f_{tune} = 76 to 108 MHz; note 2	8	12	–	dB
S_{-100}	LOW side 100 kHz selectivity	Δf = –100 kHz; f_{tune} = 76 to 108 MHz; note 2	8	12	–	dB
IR	image rejection	f_{tune} = 76 to 108 MHz; V_{RF} = 50 dBμV	24	30	–	dB
FM IF level detector and mute voltage						
V_{RF}	RF input voltage for start of level ADC	read mode data byte 4 bit 4 = 1	2	3	5	μV
ΔV_{step}	level ADC step size		2	3	5	dB
PIN TMUTE						
V_{level}	level output DC voltage	V_{RF} = 0 μV	1.55	1.65	1.80	V
		V_{RF} = 3 μV	1.60	1.70	1.85	V
$V_{level(slope)}$	slope of level voltage	V_{RF} = 10 to 500 μV	150	165	180	$\frac{mV}{20\ dB}$
R_o	output resistance		280	400	520	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator: pin MPXO						
V_{MPXO}	demodulator output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.5	1.5	%
α_{AM}	AM suppression	V_{RF} = 300 µV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	40	–	–	dB
R_o	demodulator output resistance		–	–	500	Ω
I_{sink}	demodulator output sink current		–	–	30	µA
Soft mute						
$V_{i(RF)}$	RF input voltage for soft mute start	α_{mute} = 3 dB; data byte 4 bit 3 = 1	3	5	10	µV
α_{mute}	mute attenuation	V_{RF} = 1 µV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz; data byte 4 bit 3 = 1	10	20	30	dB
MPX decoder						
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
R_{AFL}; R_{AFR}	left and right audio frequency output resistance		–	–	50	Ω
$I_{sink(AFL)}$; $I_{sink(AFR)}$	left and right audio frequency output sink current		170	–	–	µA
$V_{MPXIN(max)}$	input overdrive margin	THD < 3%	4	–	–	dB
V_{AFL}/V_{AFR}	left and right audio frequency output voltage difference	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–1	–	+1	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	–	dB

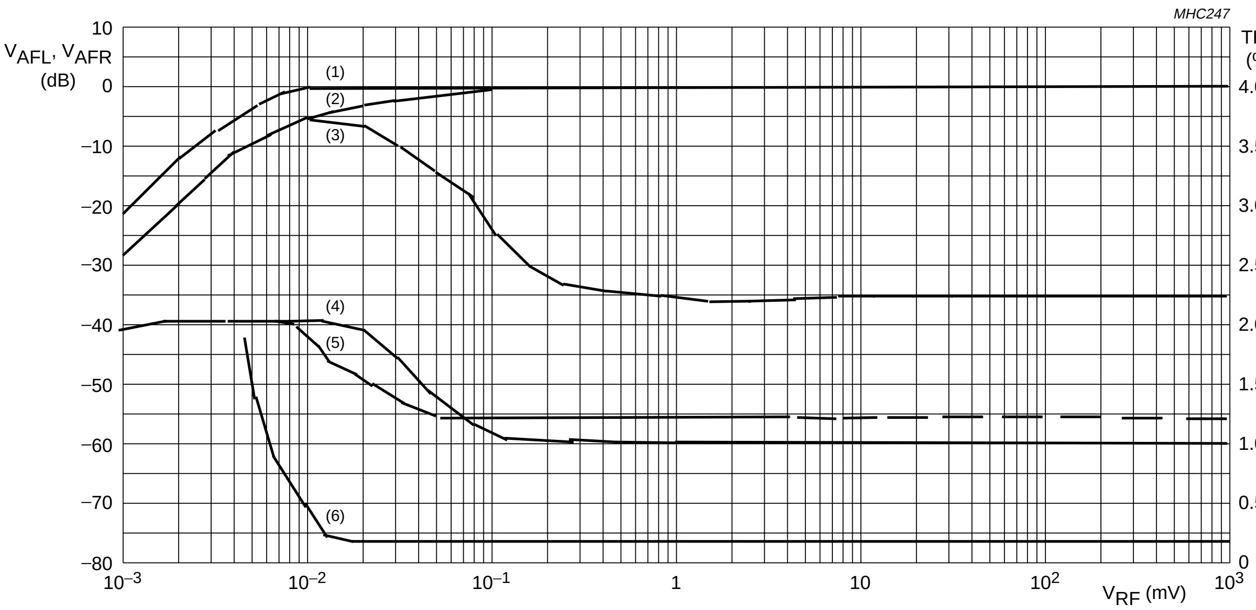
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	–	0.4	1	%
α_{pilot}	pilot suppression measured at pins V_{AFL} and V_{AFR}	related to Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	40	50	–	dB
Δf_{pilot}	stereo pilot frequency deviation	V_{RF} = 1 mV; read mode; data byte 3				
		bit 7 = 1	–	3.6	5.8	kHz
		bit 7 = 0	1	3	–	kHz
$\frac{\Delta f_{pilot1}}{\Delta f_{pilot2}}$	pilot switch hysteresis	V_{RF} = 1 mV	2	–	–	dB
High cut control						
TC_{de-em}	de-emphasis time constant	V_{RF} = 1 mV				
		data byte 5 bit 2 = 0	38	50	62	μs
		data byte 5 bit 2 = 1	57	75	93	μs
		V_{RF} = 1 μV				
		data byte 5 bit 2 = 0	114	150	186	μs
		data byte 5 bit 2 = 1	171	225	279	μs
Mono to stereo blend control						
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 45 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	4	10	16	dB
Mono to stereo switched						
$\alpha_{cs(stereo)}$	stereo channel separation switching from mono to stereo with increasing RF input level	V_{RF} = 1 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0	24	–	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation switching from stereo to mono with decreasing RF input level	V_{RF} = 20 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0	–	–	1	dB

项目开发 芯片解密 零件配单 TEL:15013652265 QQ:38537442

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BUS-DRIVEN MUTE FUNCTIONS						
Tuning mute						
α_{mute}	V_{AFL} and V_{AFR} muting depth	data byte 1 bit 7 = 1	–60	–	–	dB
$\alpha_{mute(R)}$	V_{AFR} muting depth	data byte 3 bit 1 = 1	–80	–	–	dB
$\alpha_{mute(L)}$	V_{AFL} muting depth	data byte 3 bit 2 = 1	–80	–	–	dB

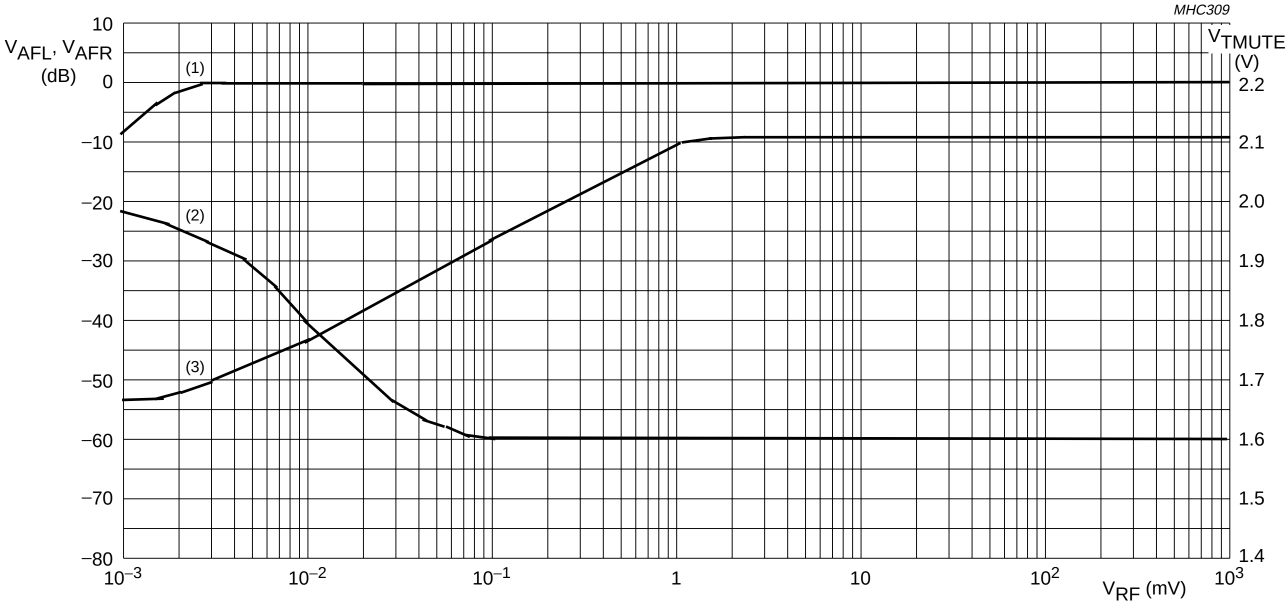
Notes

1. V_{RF} in Fig.5 is replaced by V_{RF1} + V_{RF2}. The radio is tuned to 98 MHz (HIGH side injection).
2. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.



(1) Mono signal; soft mute on.
(2) Left channel with modulation left; SNC on.
(3) Right channel with modulation left; SNC on.
(4) Noise in mono mode; soft mute on.
(5) Noise in stereo mode; SNC on.
(6) Total harmonic distortion; Δf = 75 kHz; L = R; f_{mod} = 1 kHz.

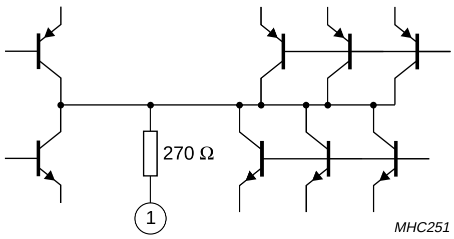
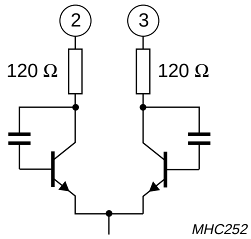
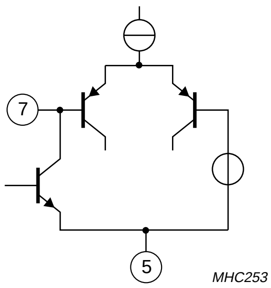
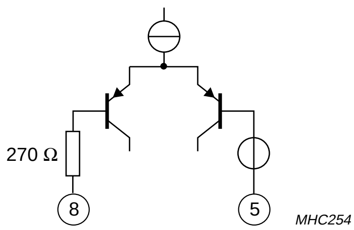
Fig.3 FM characteristics 1.

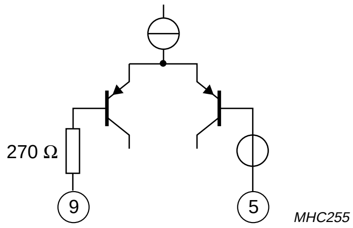
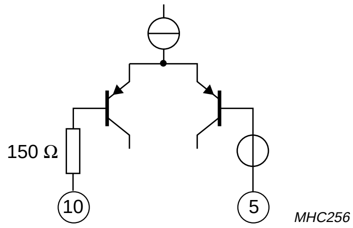
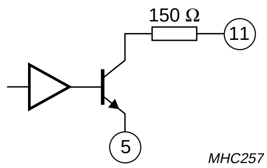
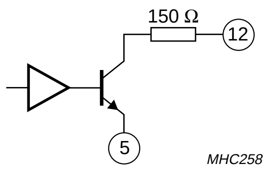
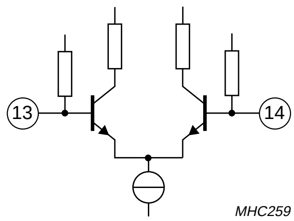
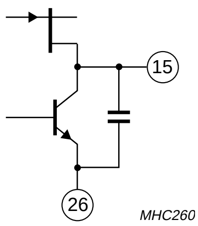


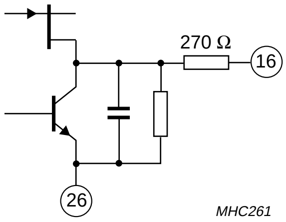
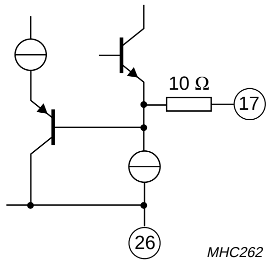
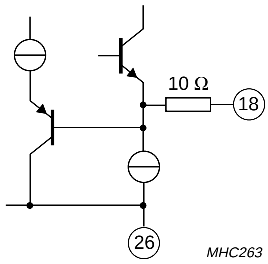
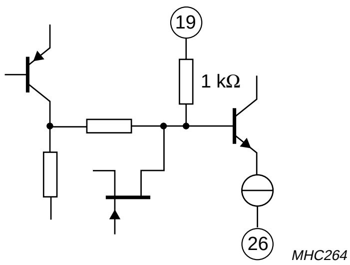
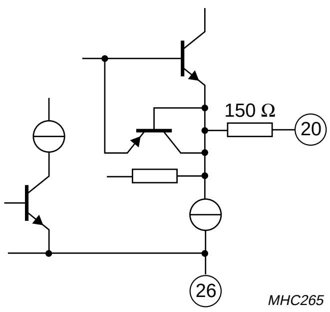
(1) Mono signal; no soft mute.
(2) Noise in mono mode; no soft mute.
(3) Level voltage; V_{CCA} = 2.7 V.

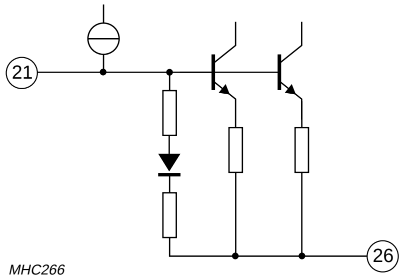
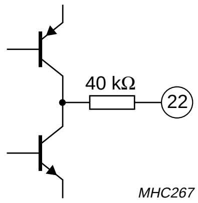
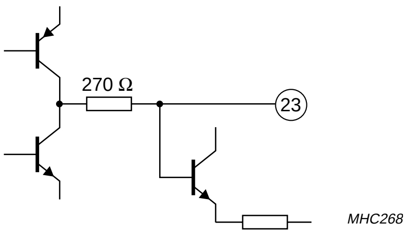
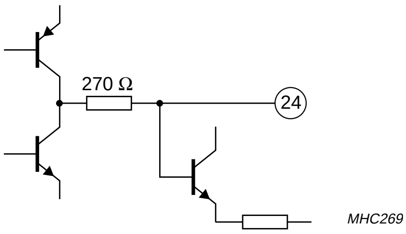
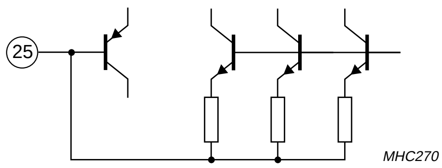
Fig.4 FM characteristics 2.

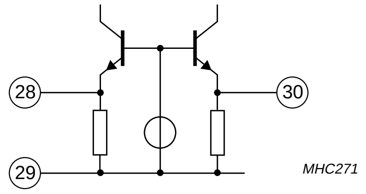
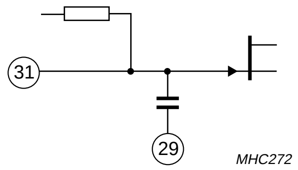
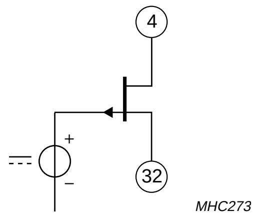
13 INTERNAL PIN CONFIGURATION

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	CPOUT	
2	VCOTANK1	
3	VCOTANK2	
4	$V_{CC(VCO)}$	
5	DGND	
6	V_{CCD}	
7	DATA	
8	CLOCK	

PIN	SYMBOL	EQUIVALENT CIRCUIT
9	BUSMODE	
10	BUSENABLE	
11	SWPORT1	
12	SWPORT2	
13	XTAL1	
14	XTAL2	
15	PHASEFIL	

PIN	SYMBOL	EQUIVALENT CIRCUIT
16	PILFIL	
17	V_{AFL}	
18	V_{AFR}	
19	TMUTE	
20	MPXO	

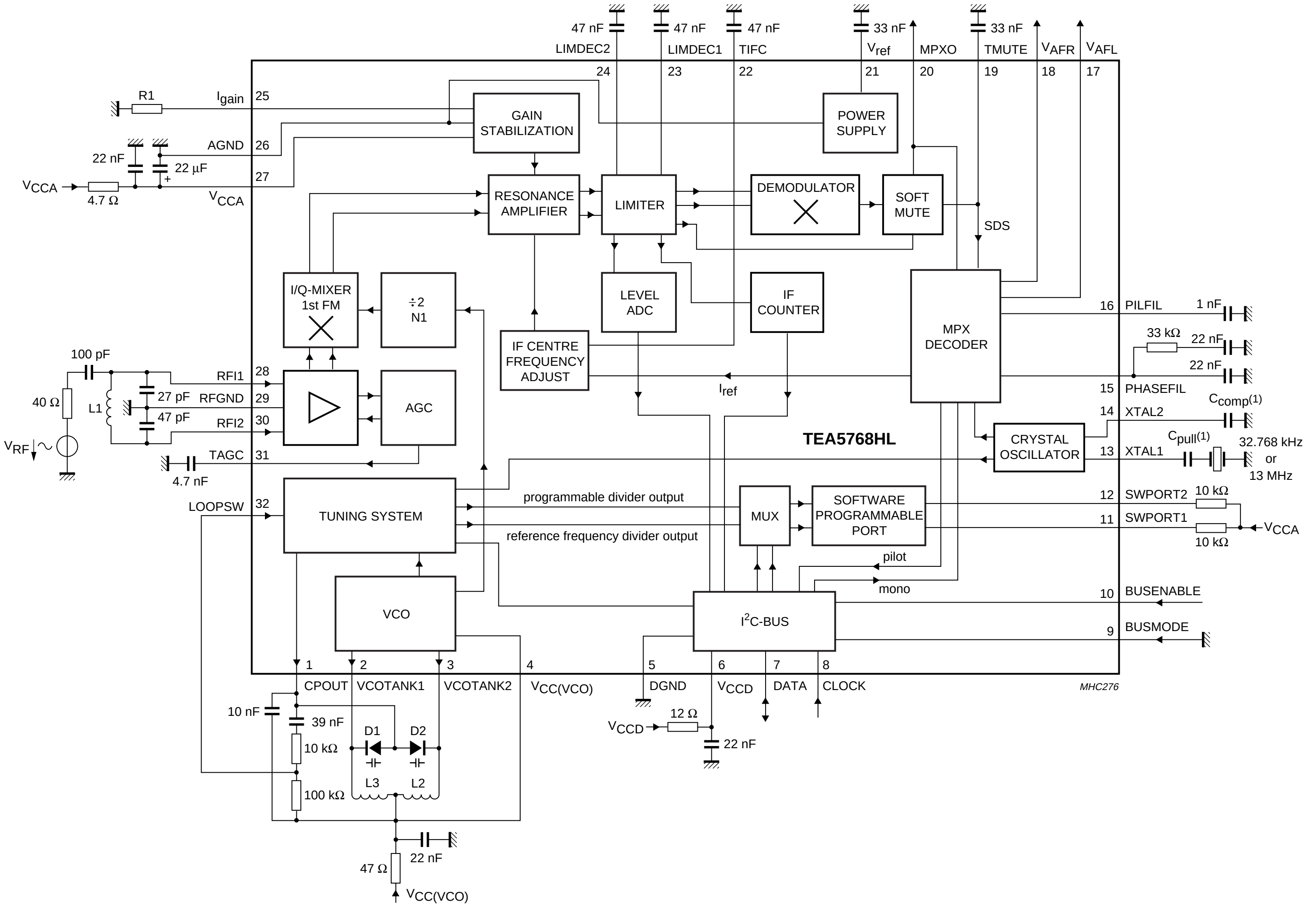
PIN	SYMBOL	EQUIVALENT CIRCUIT
21	V_{ref}	
22	TIFC	
23	LIMDEC1	
24	LIMDEC2	
25	I_{gain}	
26	AGND	
27	V_{CCA}	

PIN	SYMBOL	EQUIVALENT CIRCUIT
28	RFI1	
29	RFGND	
30	RFI2	
31	TAGC	
32	LOOPSW	

14 APPLICATION INFORMATION

Table 28 Component list for Figs 1 and 5

COMPONENT	PARAMETER	VALUE	TOLERANCE	TYPE	MANUFACTURER
R1	resistor with low temperature coefficient	18 kΩ	±1%	RC12G	Philips
D1 and D2	varicap for VCO tuning	–	–	BB202	Philips
L1	RF band filter coil	120 nH	±2%	Q_{min} = 40	
L2 and L3	VCO coil	33 nH	±2%	Q_{min} = 40	
XTAL13	13 MHz crystal	–	–	NX4025GA	
C_{pull}	pulling capacitor for NX4025GA	10 pF	–		
XTAL32.768	32.768 kHz crystal	–	–		

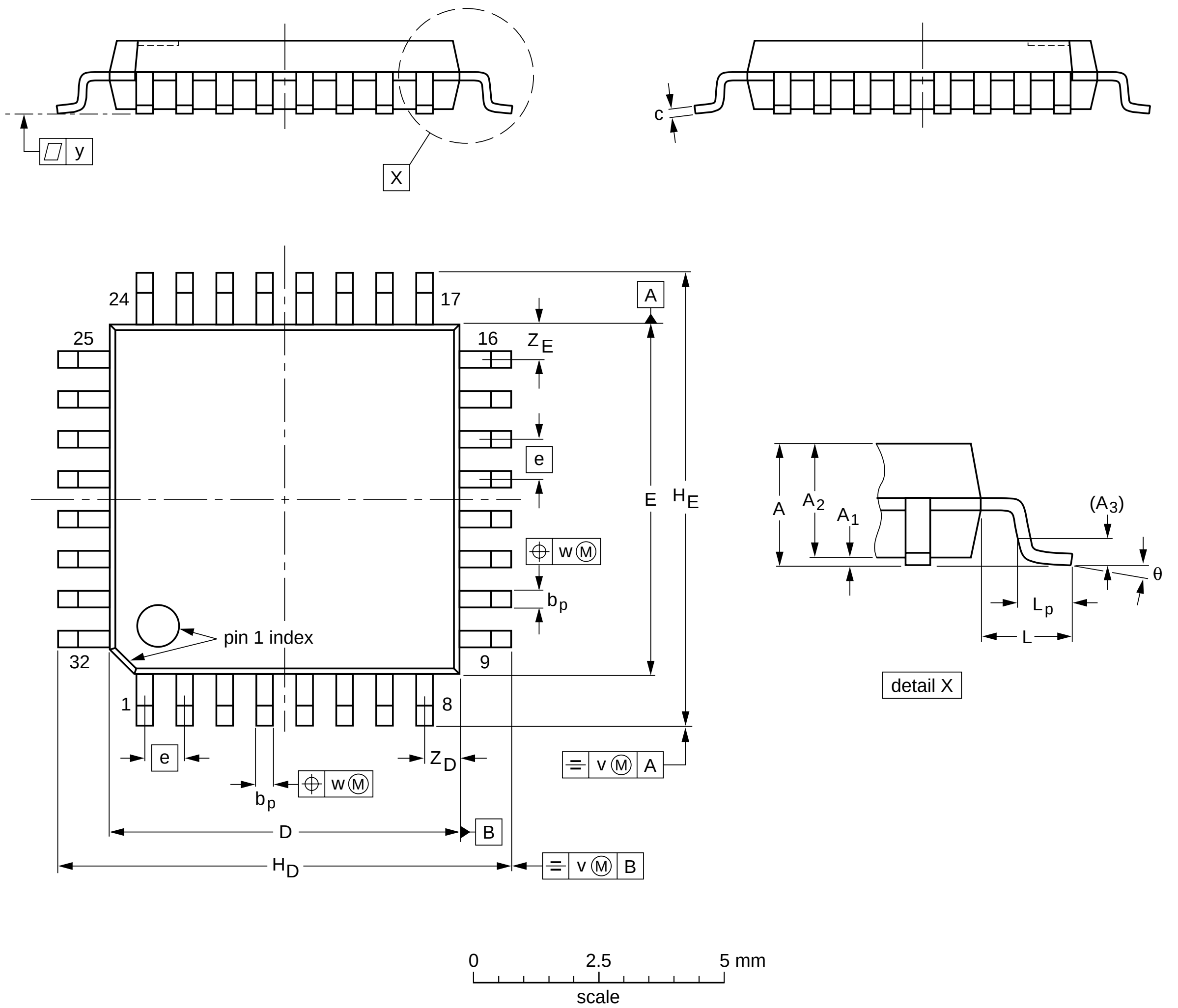


(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig.5 Test circuit.

15 PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_D	H_E	L	L_p	v	w	y	Z_D (1)	Z_E (1)	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1	136E03	MS-026				~~99-12-27~~ 00-01-19

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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NOTES

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TEA5767/68

single-chip FM stereo radio

Philips Semiconductors' digitally tuned TEA5767/68 FM stereo receiver IC is based on an innovative architecture concept that simplifies radio design, significantly reducing the number of external components. Delivering the highest performance levels, this one-chip radio solution occupies minimal PCB area (9x9 mm) making it ideal for all space-critical and low voltage applications such as mobile phones and MP3 players.

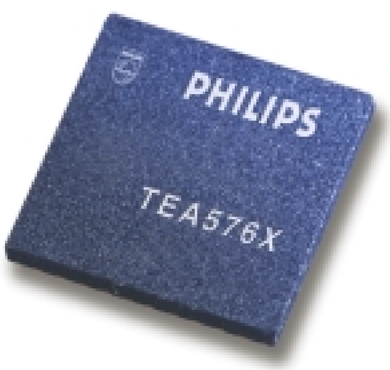
The single-chip TEA5767/68 is a miniature, digitally tuned radio IC that utilizes an entirely new radio architecture concept that replaces passive components and complex circuitry, with on-board silicon, drastically reducing the overall bill of materials and making design-in easier. It requires zero external alignments, resulting in shorter design times and lower manufacturing costs due to simplified component placement and reduced logistics overhead. Also, being adjustment free, it delivers increased quality and reliability, both in manufacture and throughout its lifetime in your end application.

As well as offering increased functionality in handheld devices, the radio IC is ideal for integration in a wide range of applications, where its minimal interaction with the rest of your application helps avoid reception / transmission interference. The TEA5767/68 also features very low power consumption and its small footprint makes it ideal for applications where board space is at a premium.

Capable of tuning to European, US and Japanese FM bands, the TEA5767/68 does not need an external FM discriminator and handles IF selectivity entirely on-chip.

Applications

- FM stereo receiver in MP3 players, portable audio devices and mobile phones
- Miniature FM radio
- Mini- and micro-sized audio systems
- Home Hi-Fi



Key features

- Only 18 external components (19 passive components replaced by silicon)
- No alignments necessary
- Fully integrated FM IF selectivity and demodulation
- Signal dependent mono / stereo blend (stereo noise cancelling)
- Adjustment free stereo decoder
- Soft mute and signal dependent high cut control (HCC)
- Autonomous Search Tune (AST) to decrease bus communication
- Software switchable low / high injection local oscillator
- Two software programmable ports
- 32.768 kHz / 6.5 MHz / 13 MHz software switchable oscillator
- Package/interface options
  - TEA5767HL with 3-wire bus – LQFP32
  - TEA5768HL with I²C-bus – LQFP32
  - TEA5767HN with switchable 3-wire / I²C-bus – small HVQFN40
- Standby mode switched via bus
- 2.5 V minimum supply voltage
- Automotive temperature range (at 5 V_{CC})

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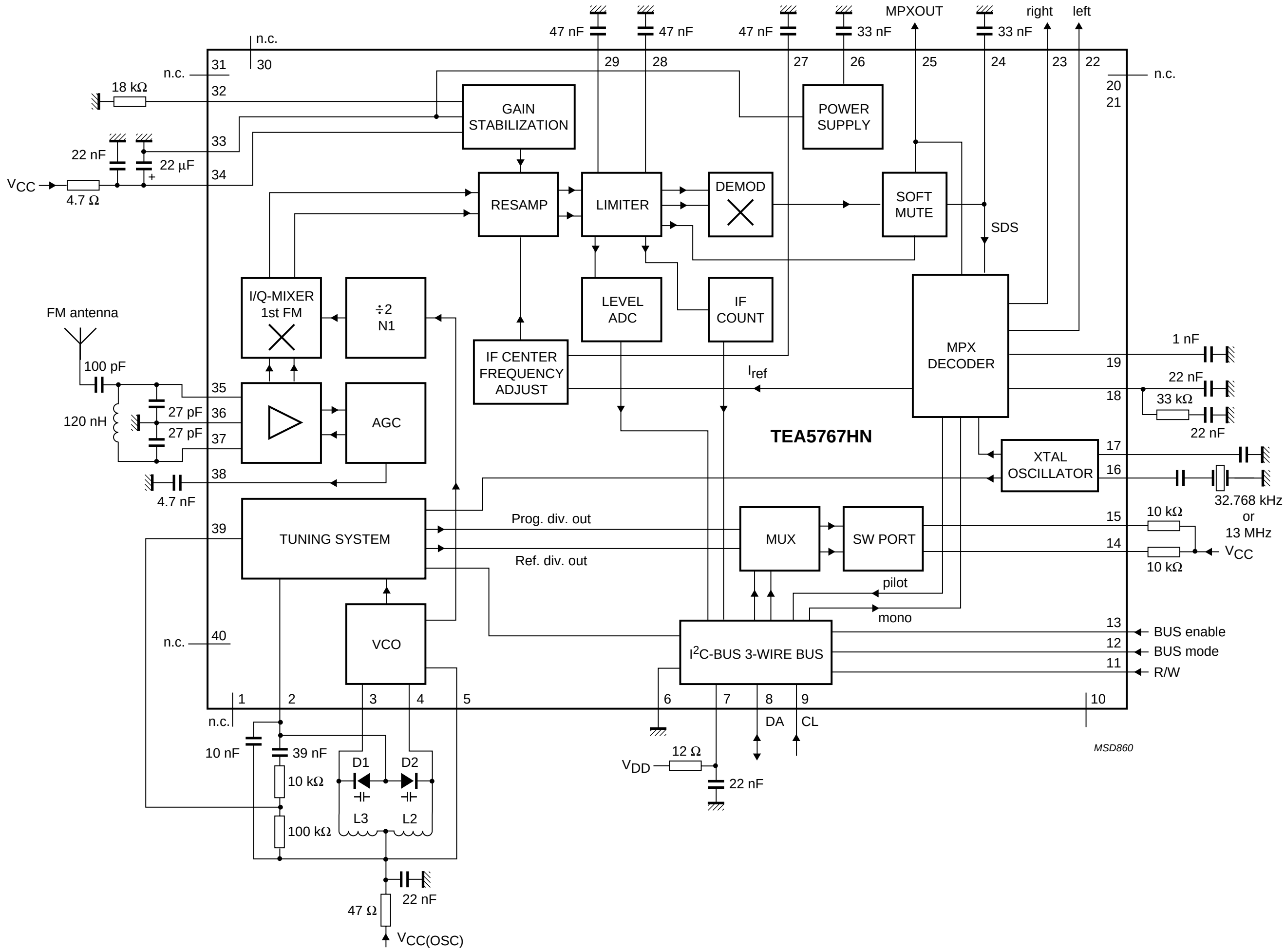

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