●元器件卡片

超高速运放 THS3001

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随着通信和多媒体技术的迅猛发展，对高速集成电路的要求不断提高，THS3001 就是美国德州仪器公司为适应这种形势而生产的超高速运算放大器，它采用电流模技术制造，是一种电流负反馈运算放大器，它以其独特的性能赢得了电子工程师的极大关注。THS3001 除了具有目前最高的转换速率外，还可使用 ±15V 电源，其输出信号幅度可达 ±12V，它的推出为电子工程人员提供了极大方便。

THS3001 具有高达 6500V/μs 的转换速率，420MHz 的 －3dB 带宽和良好的带内平坦度，在 110MHz 时，增益仅下降 0.1dB；大信号应用时具有 40ns 的建立时间；差分增益误差小于 0.01%，差分相位误差小于 0.02%；非线性失真小于 －96dB；电源电压可在 ±4.5～±15V 之间选择，单电源工作时可在 9～30V 之间使用；输出电压最大可达 ±12V。THS3001 的最大共模输入电压可接近 $\pm V_{CC}$，最大差模输入电压可达 ±6V，最大输出电流达 100mA。

THS3001 以其上述优异的技术指标被广泛应用于图象处理系统、通信系统、高清晰电视电路、高速 ADC 或 DAC 缓冲器、高频脉冲放大和高质量的视频放大等方面。它的超高速特性和大信号输出范围是一般高速运放所不能比拟的。

THS3001 采用表面安装 8 引脚封装形式，各引脚排列如图 1 所示。图 2 所示是 THS3001 的频响曲线。THS3001 在脉冲大信号输入时的响应曲线如图3 所示。在使用 THS3001 时有以下几点需要特别指出：

(1) THS3001 的最大闭环增益为 5 时能表现出最好的性能。

(2) THS3001 工作在反相放大状态时的频响比同相放大状态时好。

(3) 负反馈电阻 R_F 对频响和波形失真有较大影响，因此应使用表 1 所推存的值。（下转第 48 页）

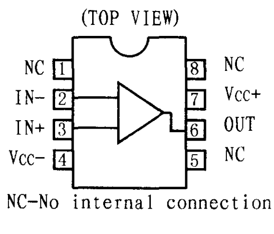


图 1　THS3001 的引脚排列图

表 1　最佳频响的 R_F 选择

增益	$R_F(V_{CC}=\pm5V)$	$R_F(V_{CC}=\pm15V)$
1	1kΩ	1kΩ
2，－1	680Ω	750Ω
－2	620Ω	620Ω
5	560Ω	620Ω

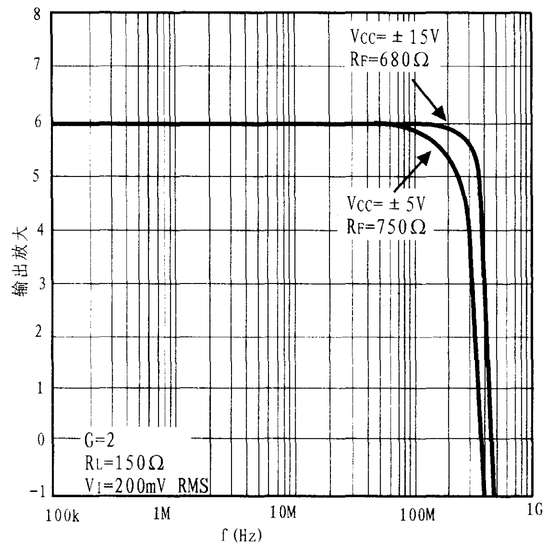


图 2　THS3001 的频响曲线

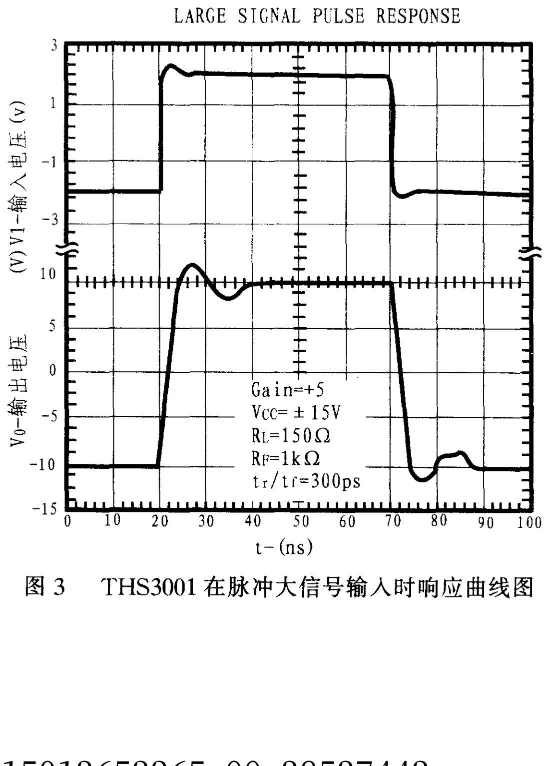


图 3　THS3001 在脉冲大信号输入时响应曲线图

(上接第41页)

(4)当放大的信号频率较高(在几MHz以上)时,若将示波器探头开关放在1:1状态下去测量输出波形,由于探头的影响将产生约100~200pF的电容量并接入输入端,这对高频信号而言,将呈现出较低的阻抗,其结果将使THS3001的输出发生过载发热甚至烧坏,因此,建议把示波器探头开关放在10:1状态,这样,对于THS3001来说,相当于接入了一个较大阻抗的负载。因而可有效防止芯片损坏。

笔者利用THS3001成功地设计了一个1Hz~100MHz的高频函数发生器,在电源电压为±10V时,输入信号为10MHz方波,信号峰峰值为1.5V,输出信号峰峰值为6.5V,具体电路如图4。

此外,德州仪器公司还推出了THS4001、THS4062、THS6002、THS6012、THS6022等型号,它们的转换速率分别为400V/μs、400V/μs、1000V/μs、1300V/μt和1900V/μs,其3dB带宽分别为270MHz、180MHz、140MHz、140MHz和210MHz。电源电压均可以从±5V到±15V,其中THS4001、THS4062为电压负反馈运放,其余为电流负反馈运放。

收稿日期:2000-07-25
咨询编号:001214

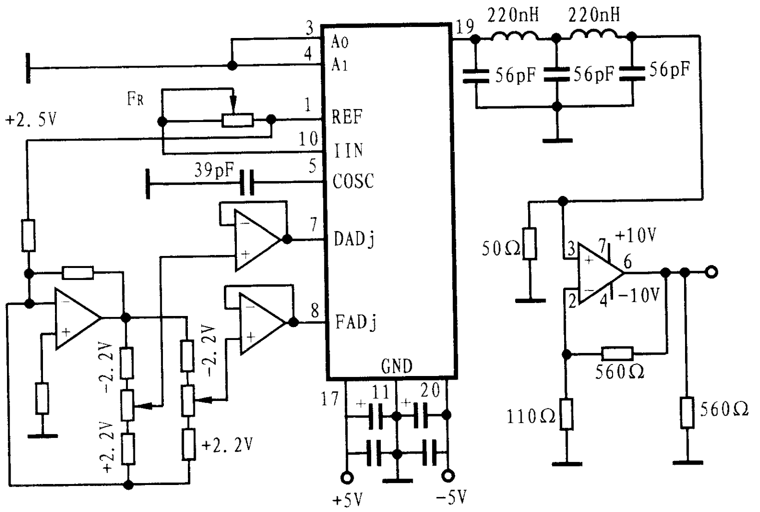


图4 THS3001高频函数发生器电路图

420-MHz HIGH-SPEED CURRENT-FEEDBACK AMPLIFIER

Check for Samples: THS3001

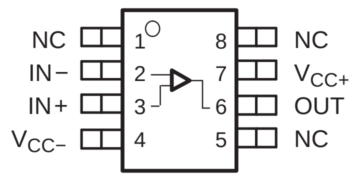
FEATURES

- **High Speed:**
  - **420-MHz Bandwidth (G = 1, -3 dB)**
  - **6500-V/μs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive: I_O = 100 mA**
- **Excellent Video Performance**
  - **115-MHz Bandwidth (0.1 dB, G = 2)**
  - **0.01% Differential Gain**
  - **0.02° Differential Phase**
- **Low 3-mV (max) Input Offset Voltage**
- **Very Low Distortion:**
  - **THD = –96 dBc at f = 1 MHz**
  - **THD = –80 dBc at f = 10 MHz**
- **Wide Range of Power Supplies:**
  - **V_{CC} = ±4.5 V to ±16 V**
- **Evaluation Module Available**

APPLICATIONS

- **Communication**
- **Imaging**
- **High-Quality Video**

THS3001
D OR DGN PACKAGE
(TOP VIEW)



NC − No internal connection

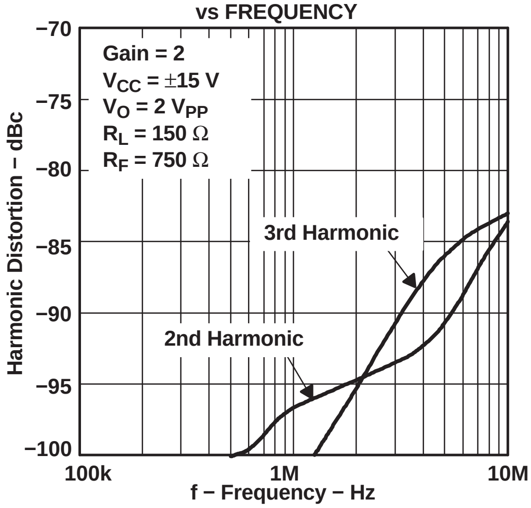
RELATED DEVICES

THS4011 /2	290-MHz VFB High-Speed Amplifier
THS6012	500-mA CFB HIgh-Speed Amplifier
THS6022	250-mA CFB High-Speed Amplifier

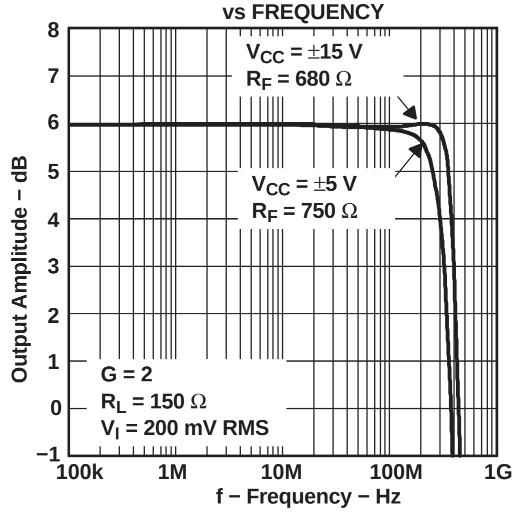
DESCRIPTION

The THS3001 is a high-speed current-feedback operational amplifier, ideal for communication, imaging, and high-quality video applications. This device offers a very fast 6500-V/μs slew rate, a 420-MHz bandwidth, and 40-ns settling time for large-signal applications requiring excellent transient response. In addition, the THS3001 operates with a very low distortion of –96 dBc, making it well suited for applications such as wireless communication basestations or ultrafast ADC or DAC buffers.

HARMONIC DISTORTION
vs FREQUENCY



OUTPUT AMPLITUDE
vs FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

T_A	PACKAGED DEVICE			TRANSPORT MEDIA, QUANTITY	EVALUATION MODULE
	SOIC (D)	MSOP (DGN)	MSOP SYMBOL		
0°C to 70°C	THS3001CD	THS3001CDGN	ADP	Rails, 75	THS3001EVM
	THS3001CDR	THS3001CDGNR		Tape and Reel, 2500	--
		THS3001HVCDGN	BNK	Rails, 75	--
		THS3001HVCDGNR		Tape and Reel, 2500	--
-40°C to 85°C	THS3001ID	THS3001IDGN	ADQ	Rails, 75	--
	THS3001IDR	THS3001IDGNR		Tape and Reel, 2500	--
		THS3001HVIDGN	BNJ	Rails, 75	--
		THS3001HVIDGNR		Tape and Reel, 2500	--

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			THS3001	THS3001HV	UNITS
V_{SS}	Supply voltage, V_{CC+} to V_{CC-}		33	37	V
V_I	Input voltage		$\pm V_{CC}$	$\pm V_{CC}$	V
I_O	Output current		175	175	mA
V_{ID}	Differential input voltage		±6	±6	V
	Continuous total power dissipation		See Dissipation Rating Table		
T_J	Maximum junction temperature (2)		150	150	°C
T_J	Maximum junction temperature, continuous operation, long term reliability(3)		125	125	°C
T_A	Operating free-air temperature	THS3001C, THS3001HVC	0 to 70	0 to 70	°C
		THS3001I, THS3001HVI	–40 to 85	–40 to 85	°C
T_{stg}	Storage temperature		–65 to 125	–65 to 125	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (1) (°C/W)	POWER RATING (2)	
			$T_A \leq 25°C$	$T_A = 85°C$
D (8)	38.3	97.5	1.02 W	410 mW
DGN (8)	4.7	58.4	1.71 W	685 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

				MIN	NOM	MAX	UNIT
V_{SS}	Supply voltage, V_{CC+} and V_{CC-}	Split supply	THS3001C, THS3001I	±4.5		±16	V
		Single supply		9		32	
		Split supply	THS3001HVC, THS3001HVI	±4.5		±18.5	
		Single supply		9		37	
T_A	Operating free-air temperature	THS3001C, THS3001HVC		0		70	°C
		THS3001I, THS3001HVI		-40		85	

ELECTRICAL CHARACTERISTICS

At T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS (1)		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range		Split supply	THS3001C THS3001I	±4.5		±16.5	V
				THS3001HVx	±4.5		±18.5	
			Single supply	THS3001C THS3001I	9		33	
				THS3001HVx	9		37	
I_{CC}	Quiescent current		V_{CC} = ±5 V	T_A = 25°C		5.5	7.5	mA
				T_A = full range			8.5	
			V_{CC} = ±15 V	T_A = 25°C		6.6	9	
				T_A = full range			10	
			V_{CC} = ±18.5 V, THS3001HV	T_A = 25°C		6.9	9.5	
				T_A = full range			10.5	
V_O	Output voltage swing		V_{CC} = ±5 V	R_L = 150 Ω	±2.9	±3.2		V
				R_L = 1 kΩ	±3	±3.3		
			V_{CC} = ±15 V	R_L = 150 Ω	±12.1	±12.8		
				R_L = 1 kΩ	±12.8	±13.1		
I_O	Output current(2)		V_{CC} = ±5 V,	R_L = 20 Ω		100		mA
			V_{CC} = ±15 V,	R_L = 75 Ω	85	120		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	3	mV
				T_A = full range			4	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V			5		µV/°C
I_{IB}	Input bias current	Positive (IN+)	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	10	µA
				T_A = full range			15	
		Negative (IN-)		T_A = 25°C		1	10	
				T_A = full range			15	
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3	±3.2		V
			V_{CC} = ±15 V		±12.9	±13.2		
	Open loop transresistance		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ			1.3		MΩ
			V_{CC} = ±15 V, V_O = ±7.5 V, R_L = 1 kΩ			2.4		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V, V_{CM} = ±2.5 V		62	70		dB
			V_{CC} = ±15 V, V_{CM} = ±10 V		65	73		
PSRR	Power supply rejection ratio		V_{CC} = ±5 V	T_A = 25°C	65	76		dB
				T_A = full range	63			
			V_{CC} = ±15 V	T_A = 25°C	69	76		dB
				T_A = full range	67			

(1) Full range = 0°C to 70°C for the THS3001C and -40°C to 85°C for the THS3001I.
(2) Observe power dissipation ratings to keep the junction temperature below absolute maximum when the output is heavily loaded or shorted. See Absolute Maximum Ratings table.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS (1)	MIN	TYP	MAX	UNIT
R_I	Input resistance	Positive (IN+)			1.5		MΩ
		Negative (IN-)			15		Ω
C_I	Differential input capacitance				7.5		pF
R_O	Output resistance		Open loop at 5 MHz		10		Ω
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2		1.6		nV/√Hz
I_n	Input current noise	Positive (IN+)	V_{CC} = ±5 V or ±15 V, f = 10 kHz, G = 2		13		pA/√Hz
		Negative (IN-)			16		

OPERATING CHARACTERISTICS

T_A = 25°C, R_L = 150 Ω , R_F = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate (1)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V	G = –5		1700		V/µs
			G = 5		1300		
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V	G = –5		6500		
			G = 5		6300		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 0 V to 10 V Step	Gain = –1,		40		ns
	Settling time to 0.1%	V_{CC} = ±5 V, 0 V to 2 V Step,	Gain = –1,		25		
THD	Total harmonic distortion	V_{CC} = ±15 V, f_c = 10 MHz,	$V_{O(PP)}$ = 2 V, G = 2		–80		dBc
	Differential gain error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.015%		
			V_{CC} = ±15 V		0.01%		
	Differential phase error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.01°		
			V_{CC} = ±15 V		0.02°		
BW	Small signal bandwidth (-3 dB)	G = 1, R_F = 1 kΩ	V_{CC} = ±5 V		330		MHz
			V_{CC}= ±15 V		420		MHz
		G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		300		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		385		
		G = 5, R_F = 560 Ω,	V_{CC} = ±15 V		350		
	Bandwidth for 0.1 dB flatness	G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		85		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		115		
	Full power bandwidth (2)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V, R_L = 500 Ω	G = –5		65		MHz
			G = 5		62		
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V, R_L = 500 Ω	G = –5		32		
			G = 5		31		

(1) Slew rate is measured from an output level range of 25% to 75%.
(2) Full power bandwidth is defined as the frequency at which the output has 3% THD.

PARAMETER MEASUREMENT INFORMATION

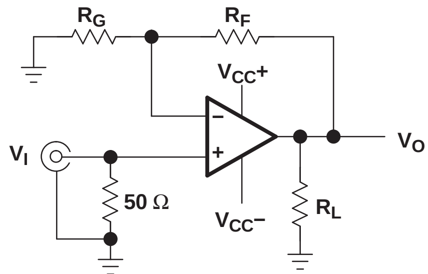


Figure 1. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$\|V_O\|$	Output voltage swing	vs Free-air temperature	2
I_{CC}	Current supply	vs Free-air temperature	3
I_{IB}	Input bias current	vs Free-air temperature	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Common-mode input voltage	6
		vs Common-mode input voltage	7
		vs Frequency	8
	Transresistance	vs Free-air temperature	9
	Closed-loop output impedance	vs Frequency	10
V_n	Voltage noise	vs Frequency	11
I_n	Current noise	vs Frequency	11
PSRR	Power supply rejection ratio	vs Frequency	12
		vs Free-air temperature	13
SR	Slew rate	vs Supply voltage	14
		vs Output step peak-to-peak	15, 16
	Normalized slew rate	vs Gain	17
	Harmonic distortion	vs Peak-to-peak output voltage swing	18, 19
		vs Frequency	20, 21
	Differential gain	vs Loading	22, 23
	Differential phase	vs Loading	24, 25
	Output amplitude	vs Frequency	26-30
	Normalized output response	vs Frequency	31-34
	Small and large signal frequency response		35, 36
	Small signal pulse response		37, 38
	Large signal pulse response		39 - 46

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

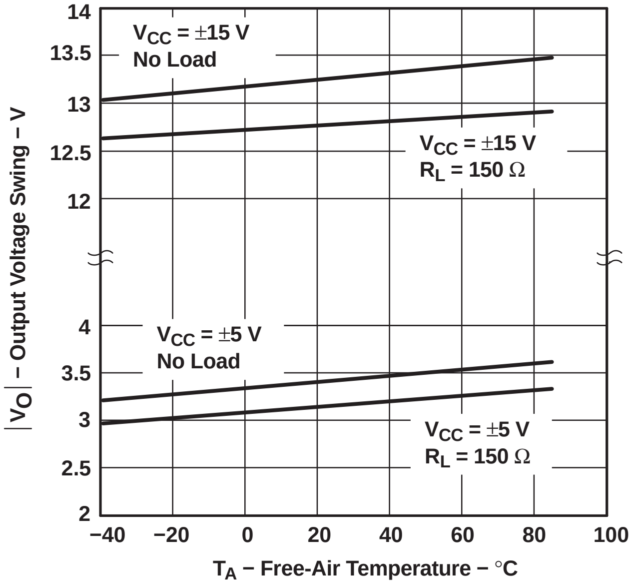


Figure 2.

CURRENT SUPPLY vs FREE-AIR TEMPERATURE

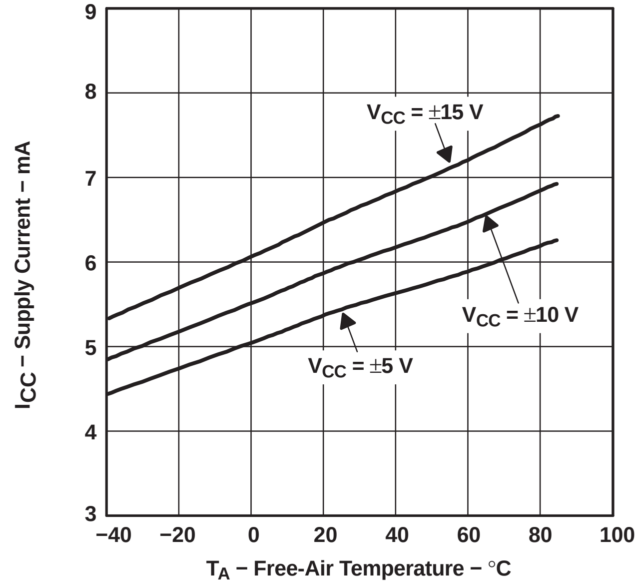


Figure 3.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

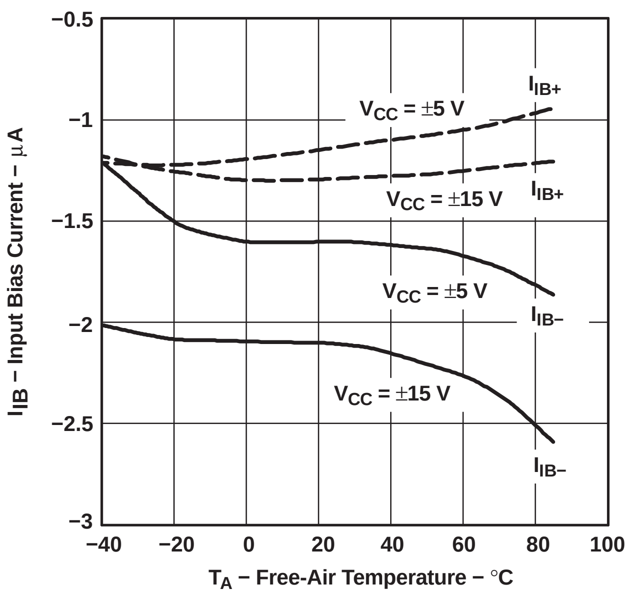


Figure 4.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

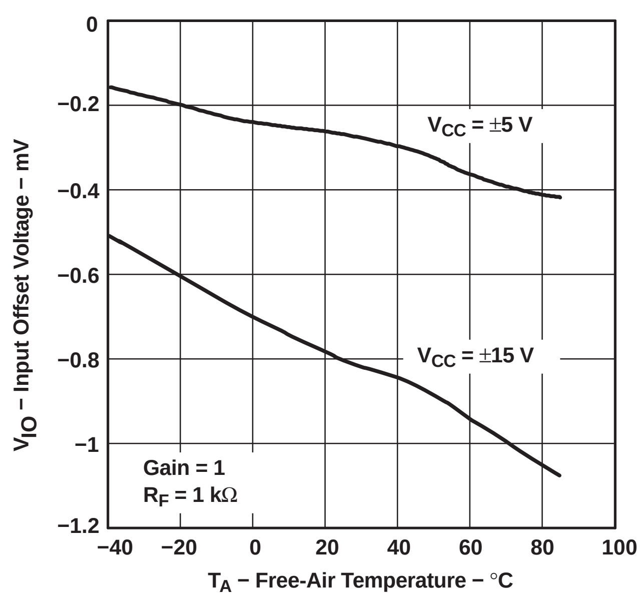


Figure 5.

TYPICAL CHARACTERISTICS (continued)

COMMON-MODE REJECTION RATIO
vs
COMMON-MODE INPUT VOLTAGE

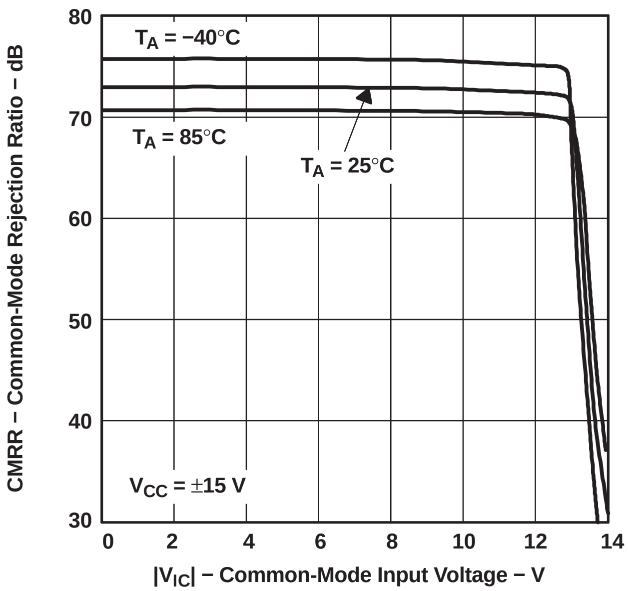


Figure 6.

COMMON-MODE REJECTION RATIO
vs
COMMON-MODE INPUT VOLTAGE

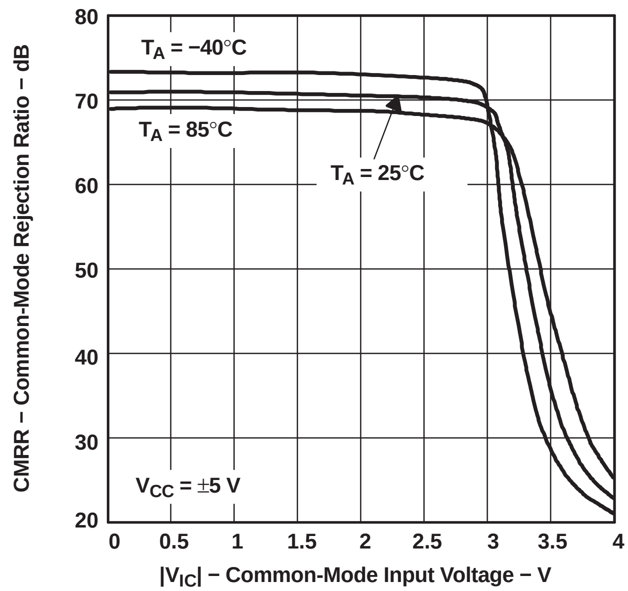


Figure 7.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

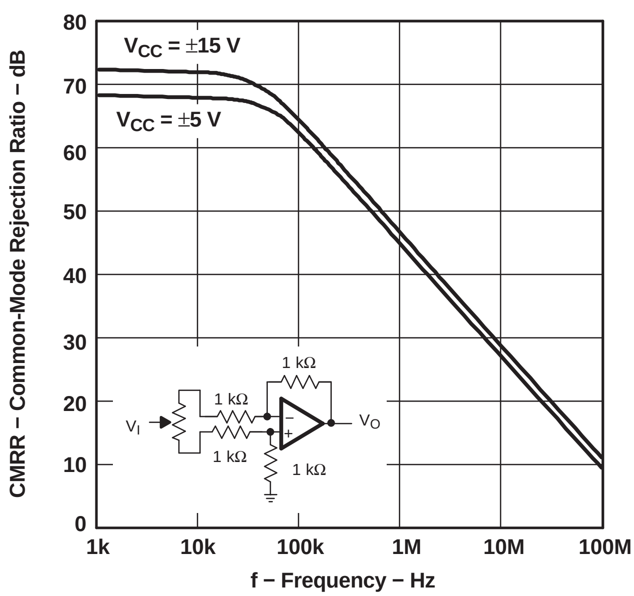


Figure 8.

TRANSRESISTANCE
vs
FREE-AIR TEMPERATURE

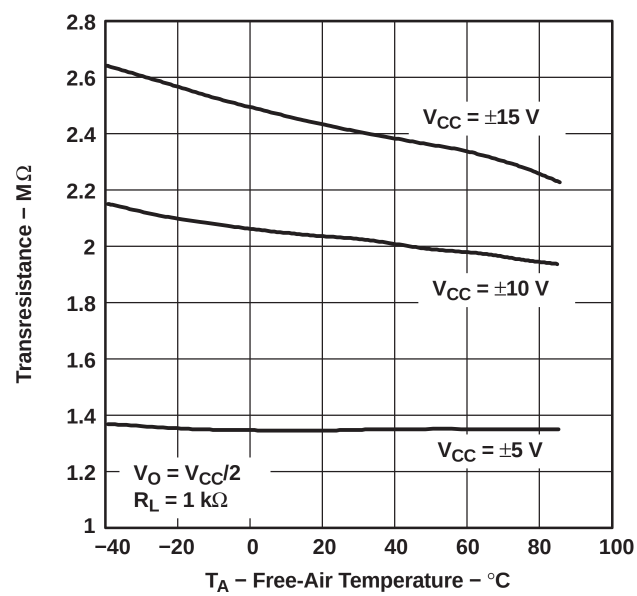


Figure 9.

TYPICAL CHARACTERISTICS (continued)

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

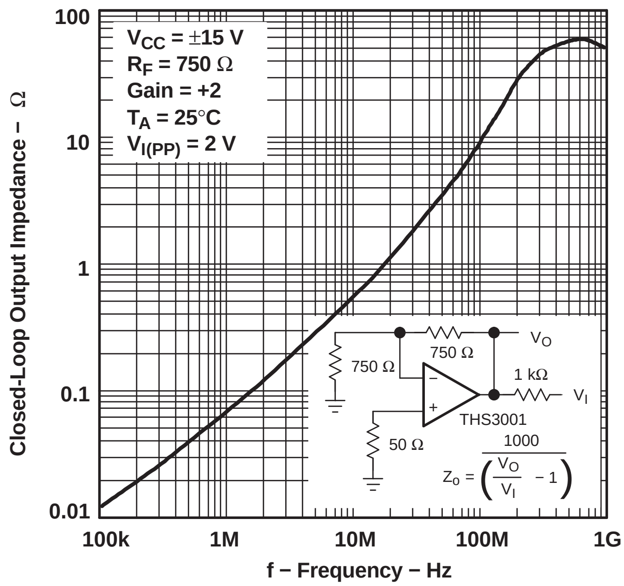


Figure 10.

VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

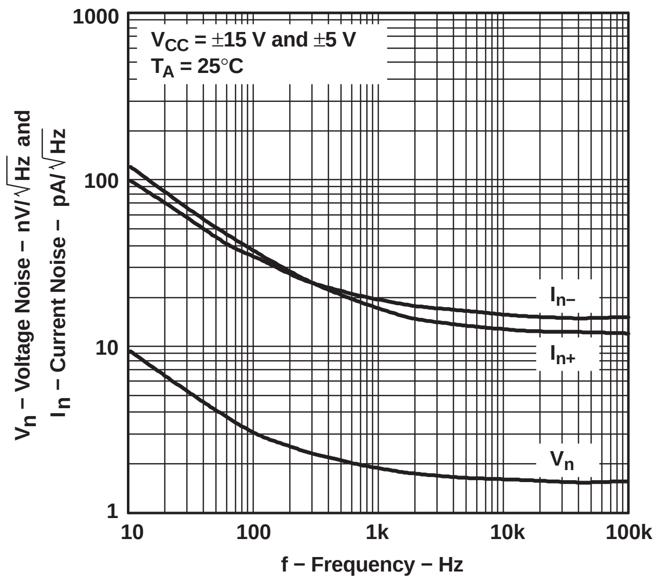


Figure 11.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

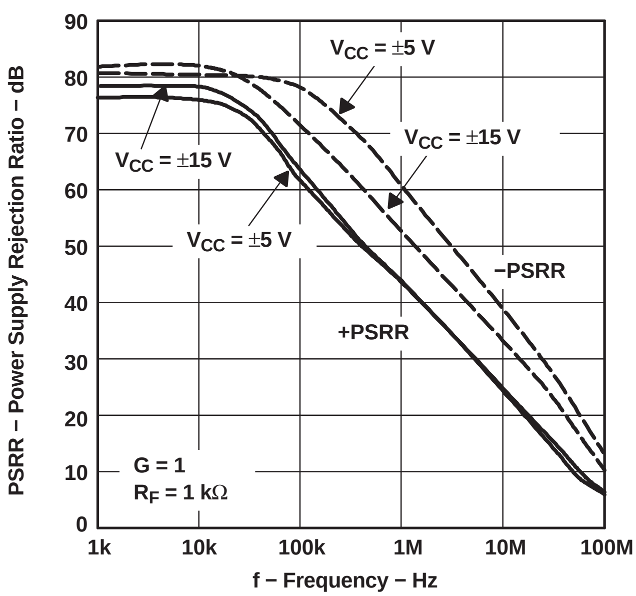


Figure 12.

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

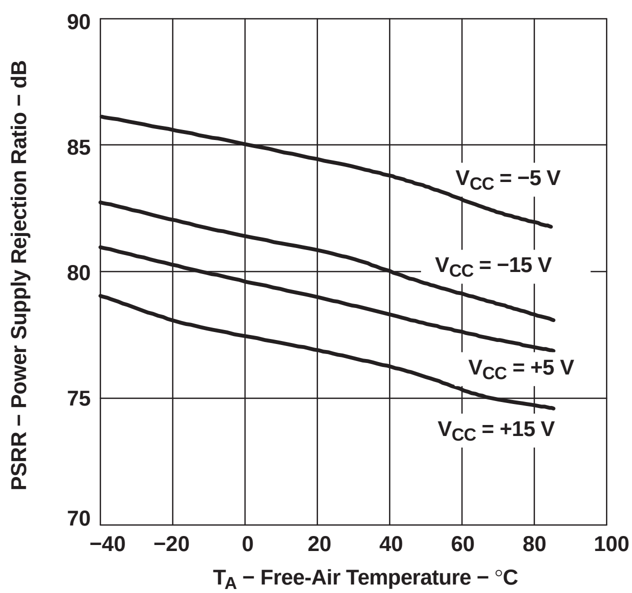


Figure 13.

TYPICAL CHARACTERISTICS (continued)

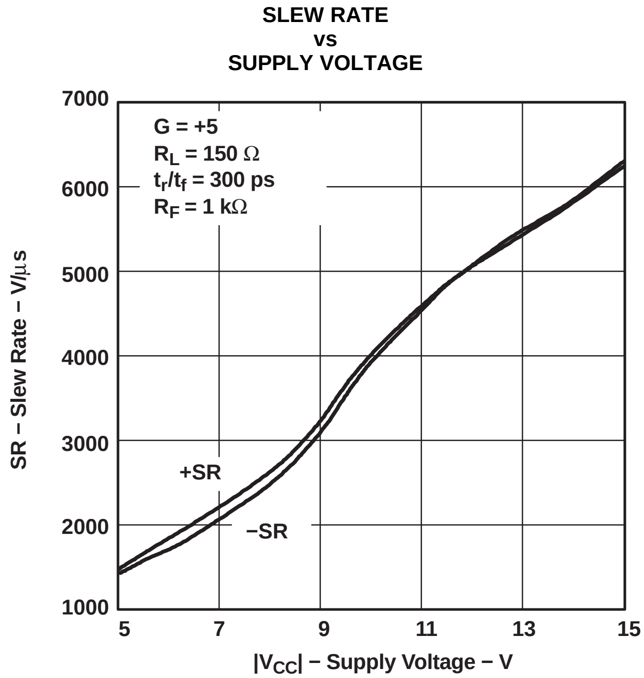


Figure 14.

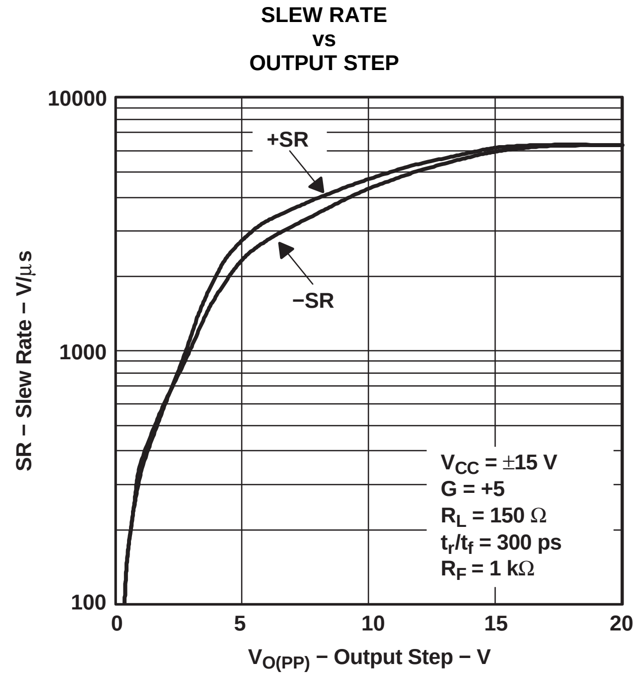


Figure 15.

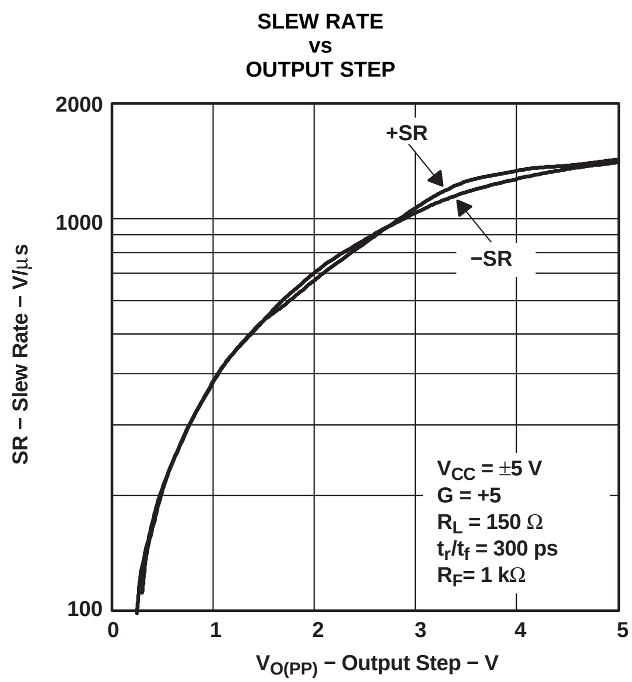


Figure 16.

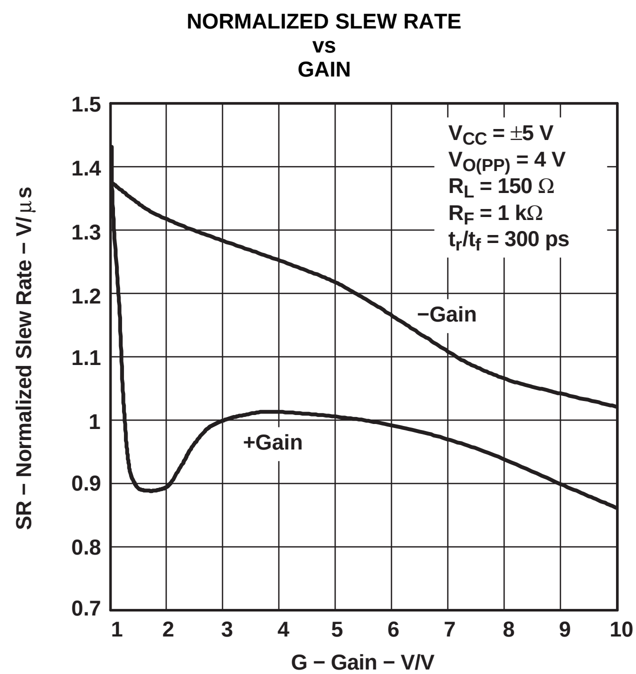


Figure 17.

TYPICAL CHARACTERISTICS (continued)

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

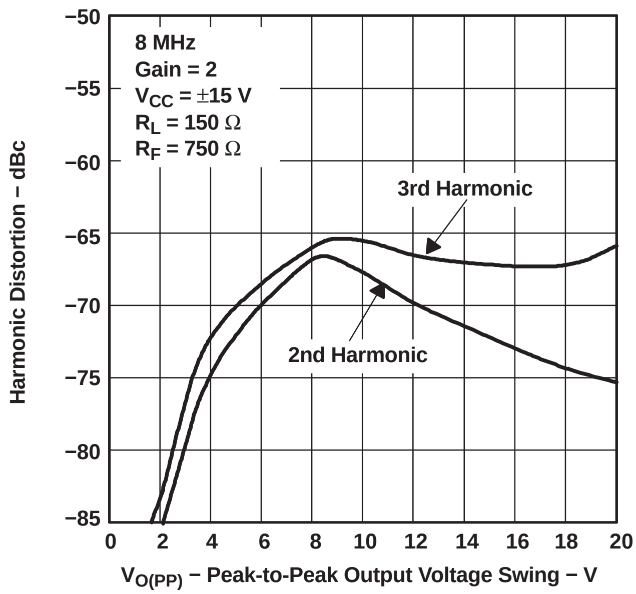


Figure 18.

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

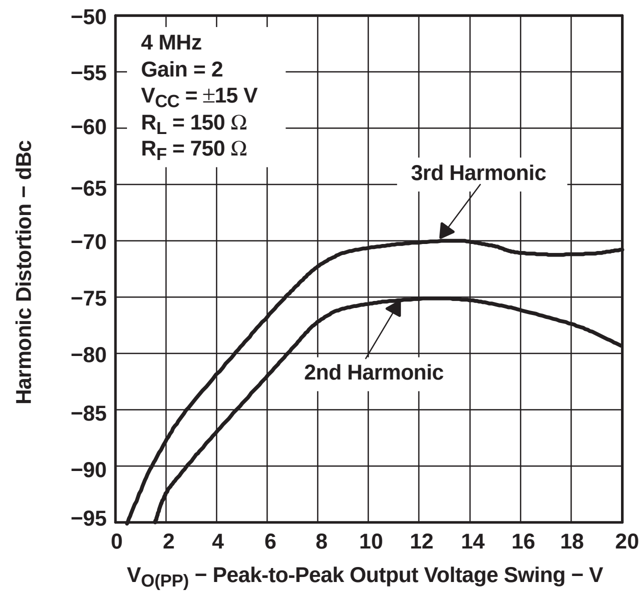


Figure 19.

HARMONIC DISTORTION
vs
FREQUENCY

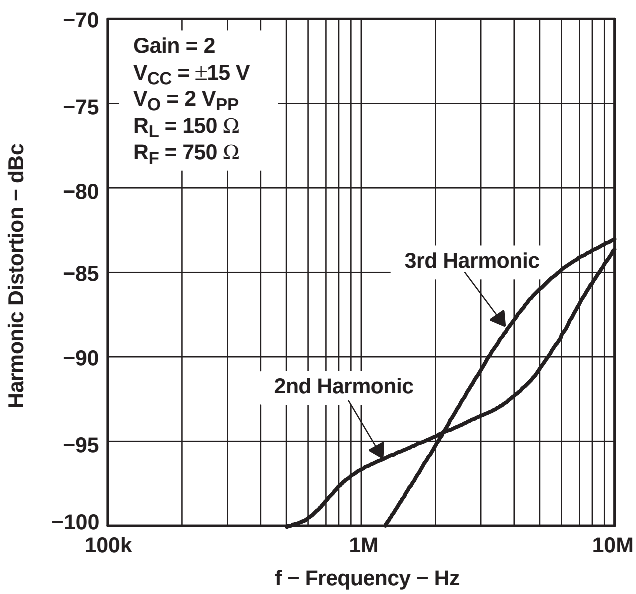


Figure 20.

HARMONIC DISTORTION
vs
FREQUENCY

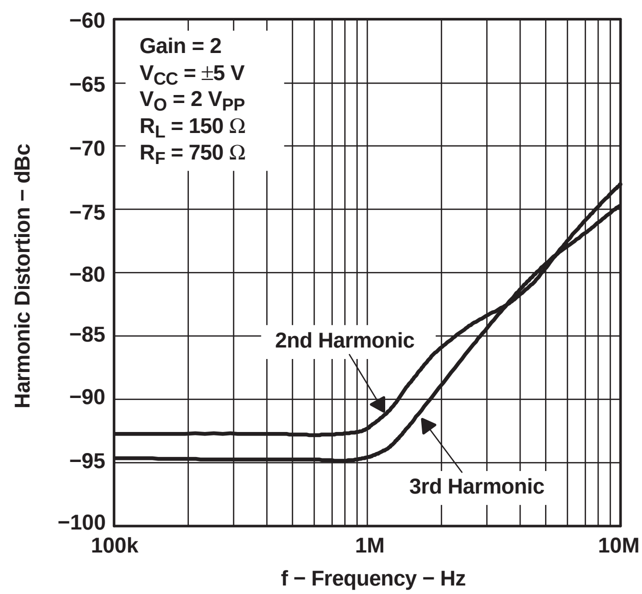


Figure 21.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL GAIN
vs
LOADING

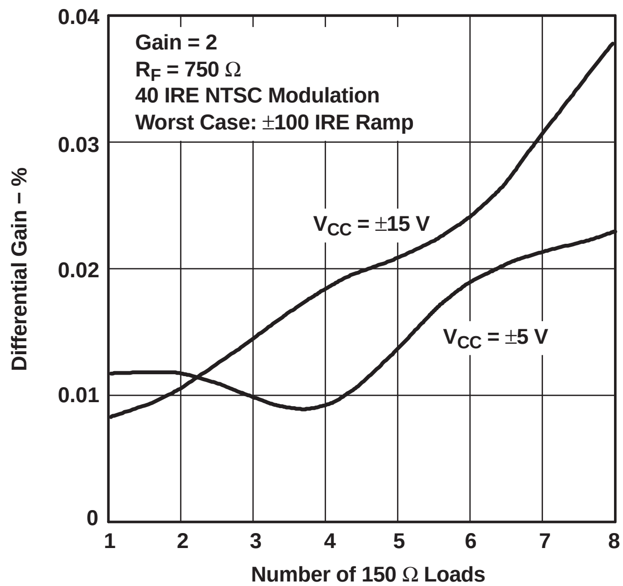


Figure 22.

DIFFERENTIAL GAIN
vs
LOADING

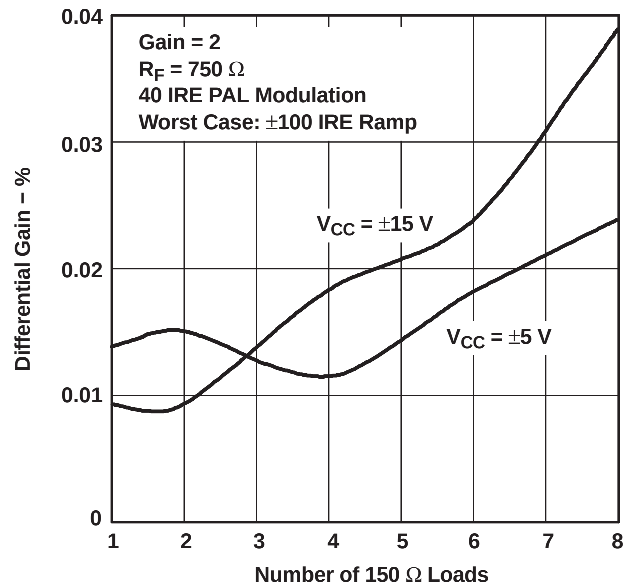


Figure 23.

DIFFERENTIAL PHASE
vs
LOADING

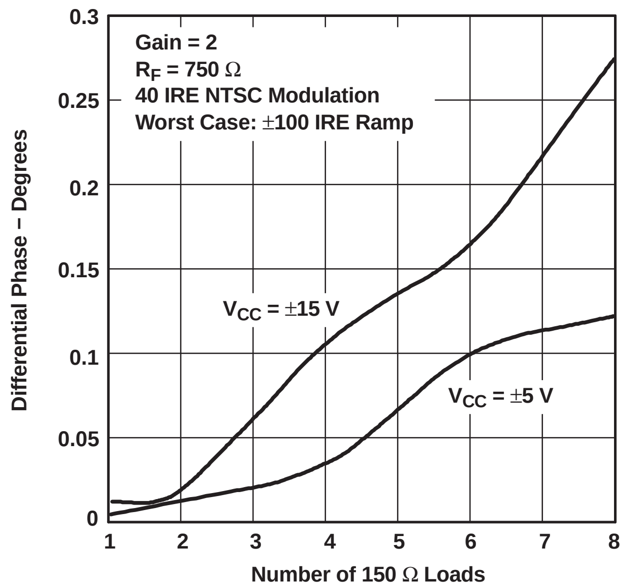


Figure 24.

DIFFERENTIAL PHASE
vs
LOADING

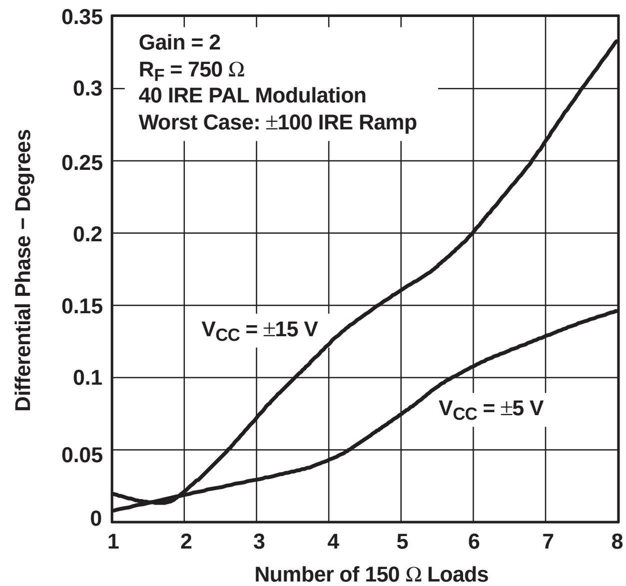


Figure 25.

TYPICAL CHARACTERISTICS (continued)

OUTPUT AMPLITUDE vs FREQUENCY

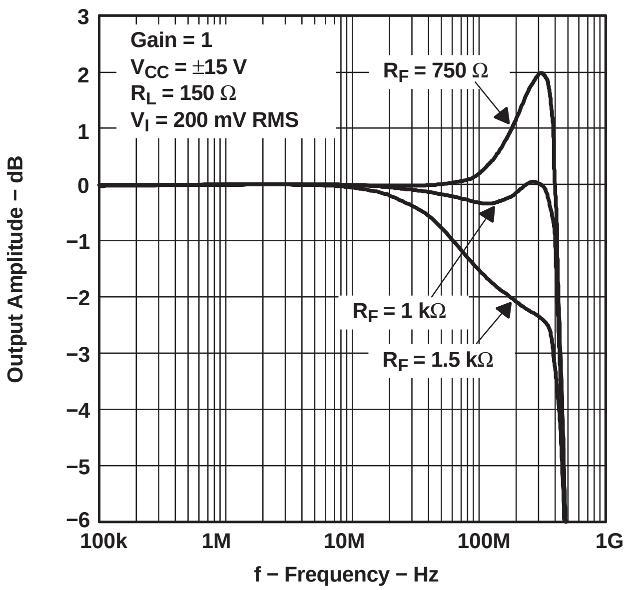


Figure 26.

OUTPUT AMPLITUDE vs FREQUENCY

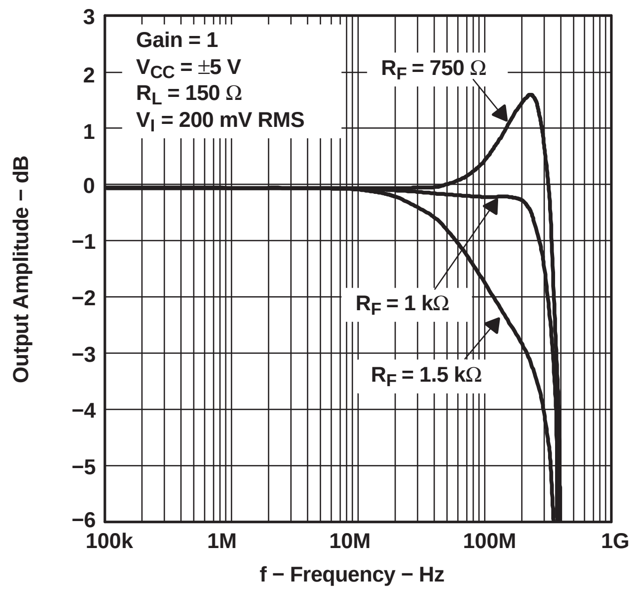


Figure 27.

OUTPUT AMPLITUDE vs FREQUENCY

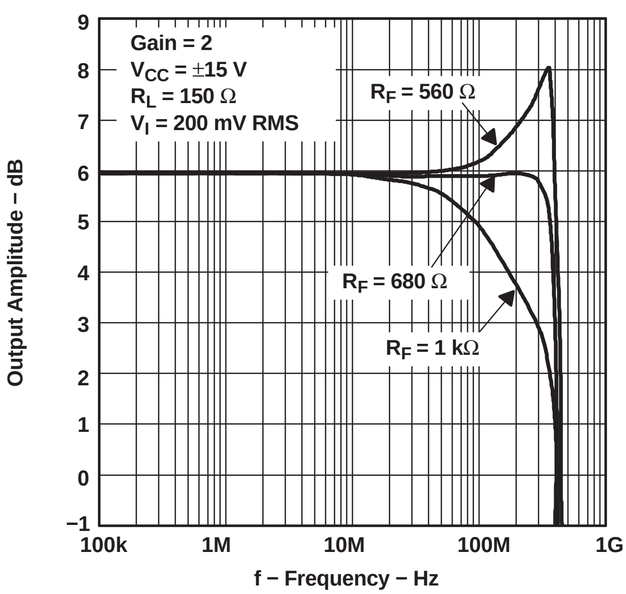


Figure 28.

OUTPUT AMPLITUDE vs FREQUENCY

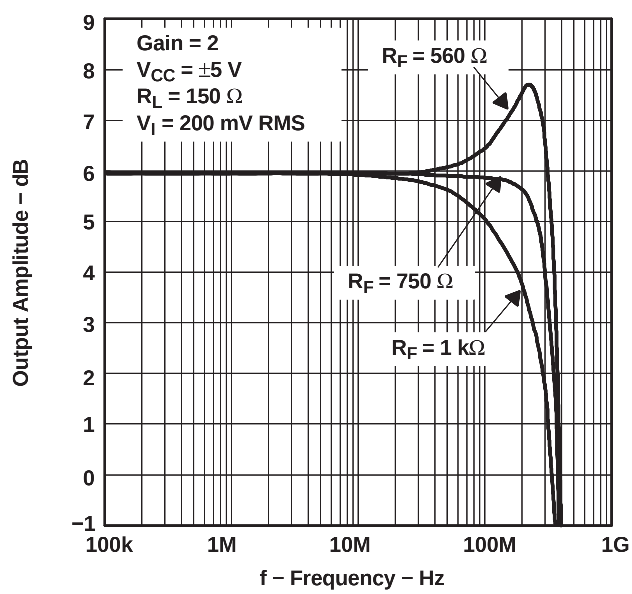


Figure 29.

TYPICAL CHARACTERISTICS (continued)

OUTPUT AMPLITUDE vs FREQUENCY

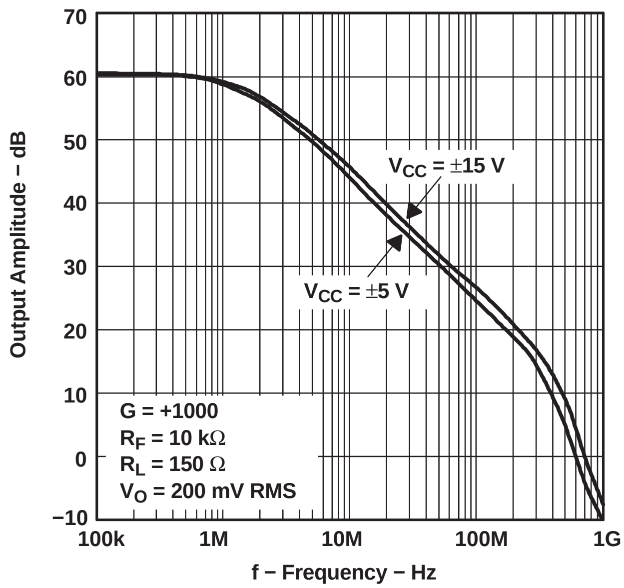


Figure 30.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

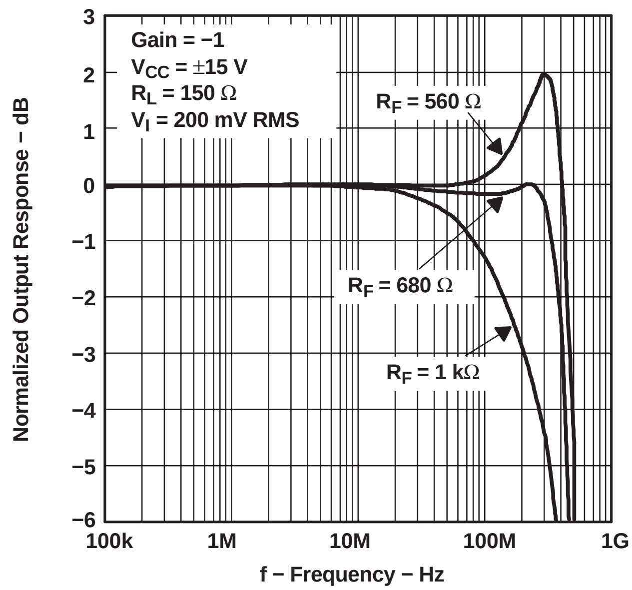


Figure 31.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

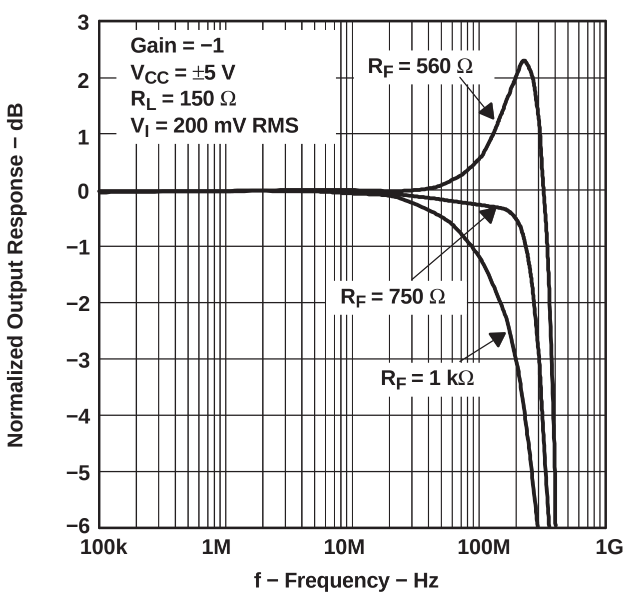


Figure 32.

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

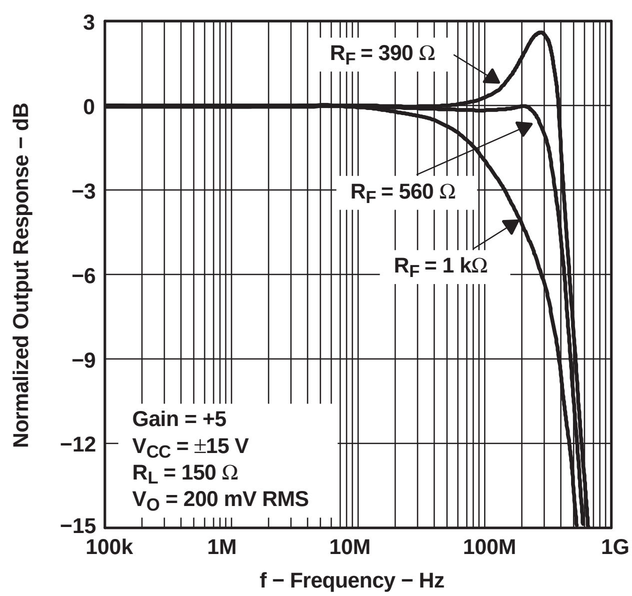


Figure 33.

TYPICAL CHARACTERISTICS (continued)

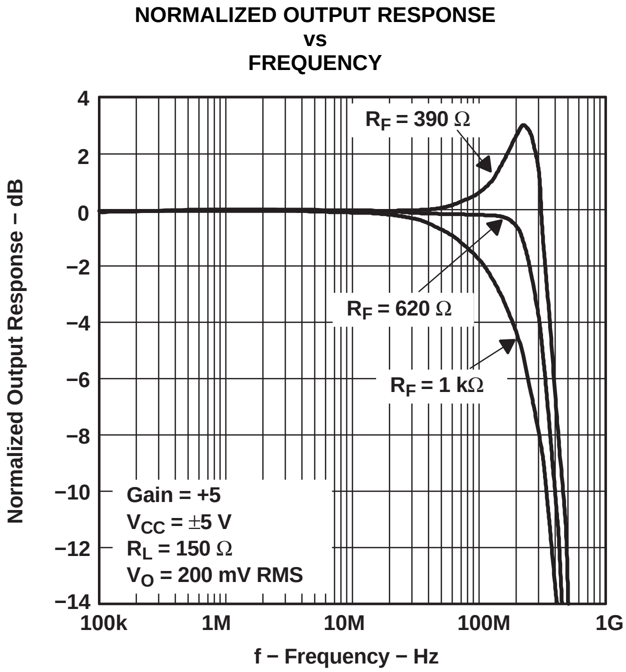


Figure 34.

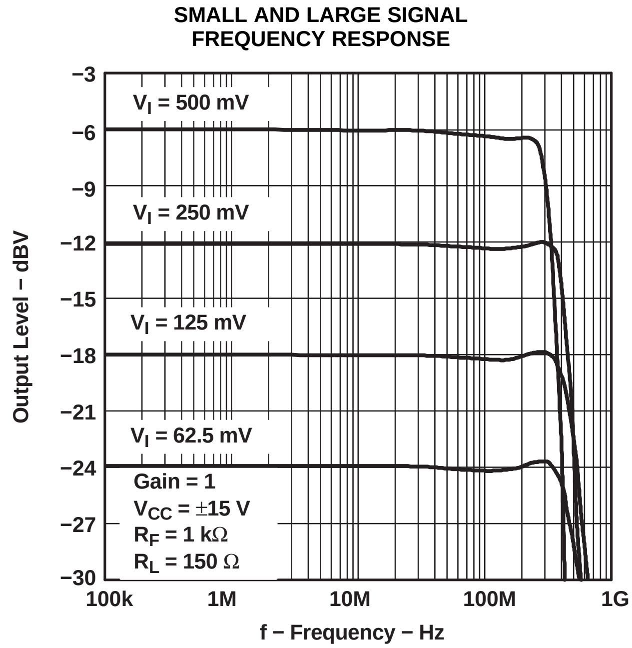


Figure 35.

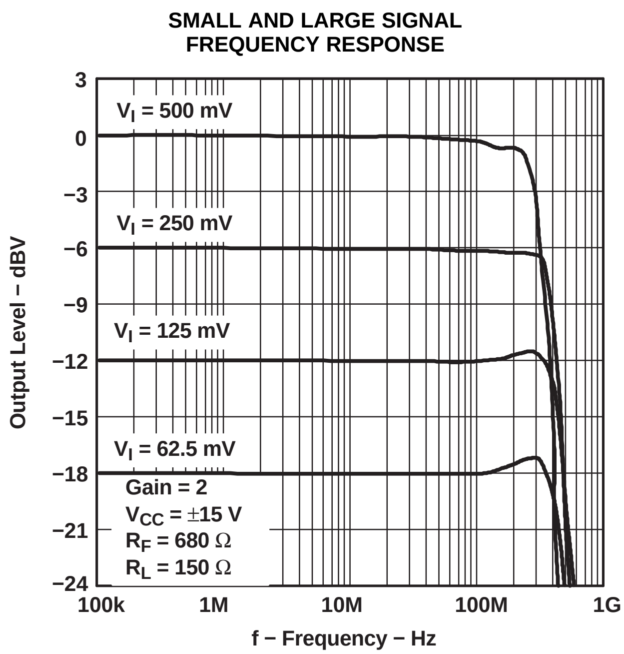


Figure 36.

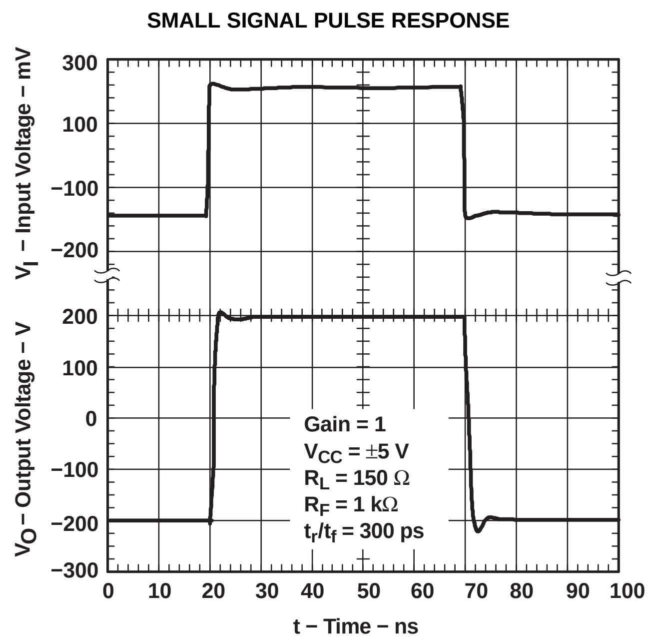


Figure 37.

TYPICAL CHARACTERISTICS (continued)

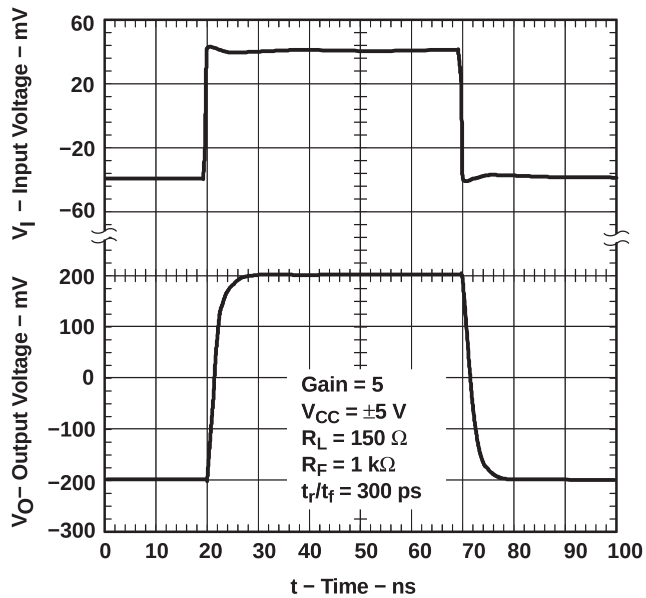


Figure 38.

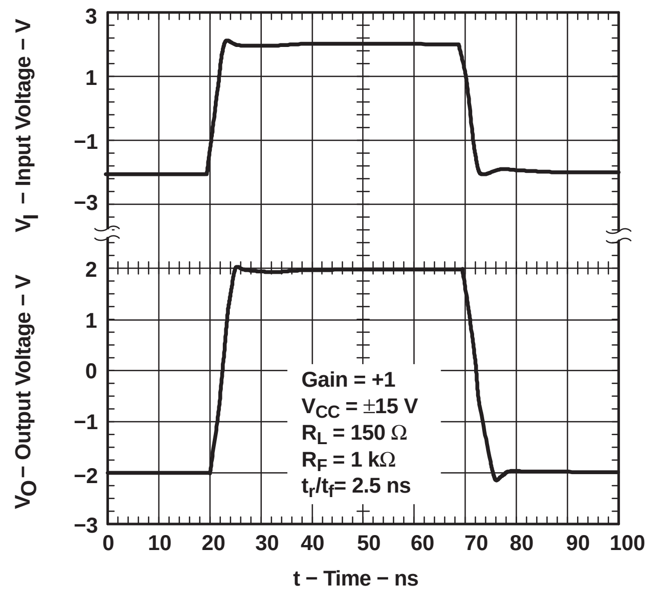


Figure 39.

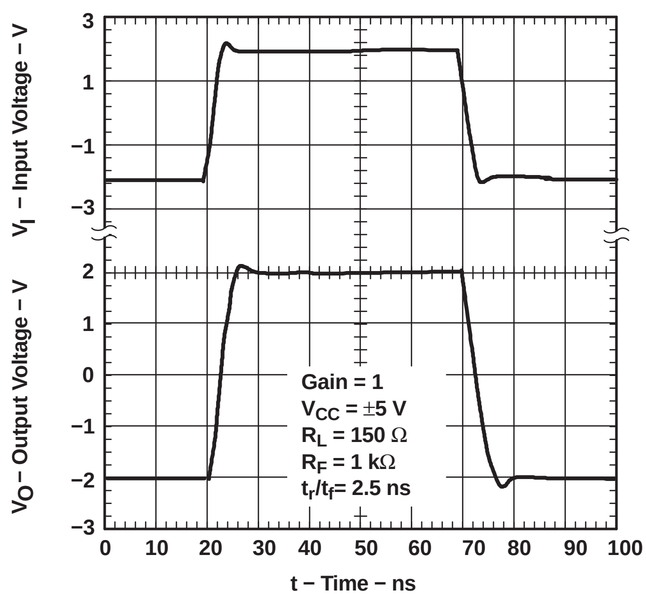


Figure 40.

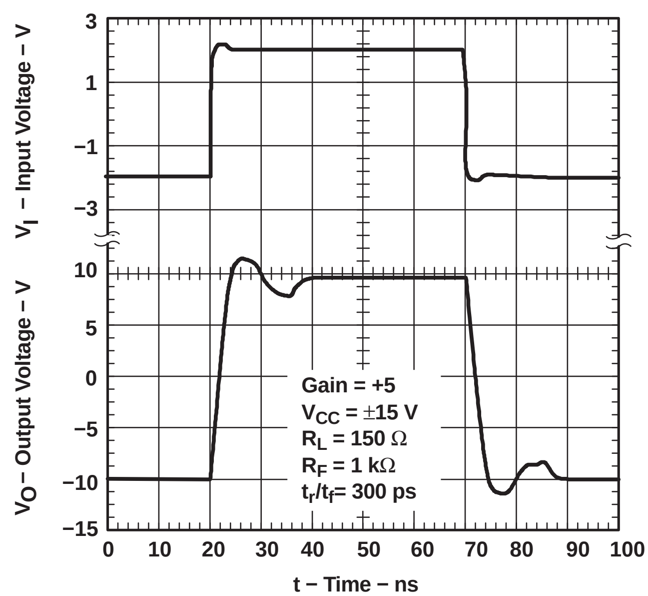


Figure 41.

TYPICAL CHARACTERISTICS (continued)

LARGE SIGNAL PULSE RESPONSE

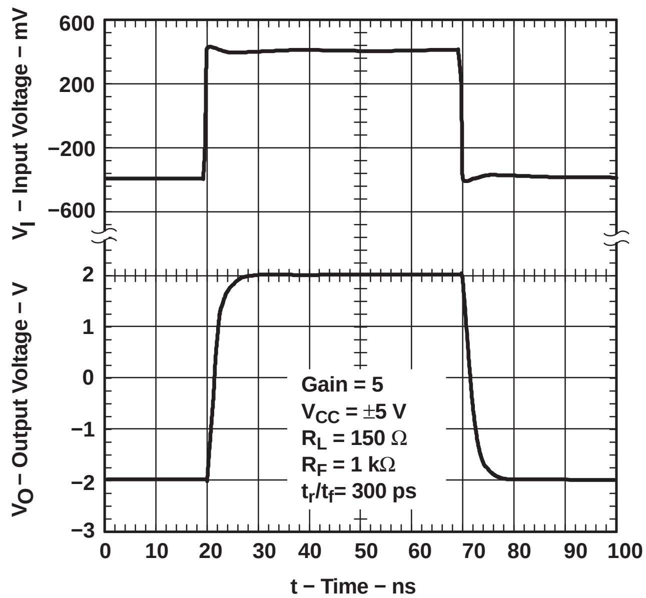


Figure 42.

LARGE SIGNAL PULSE RESPONSE

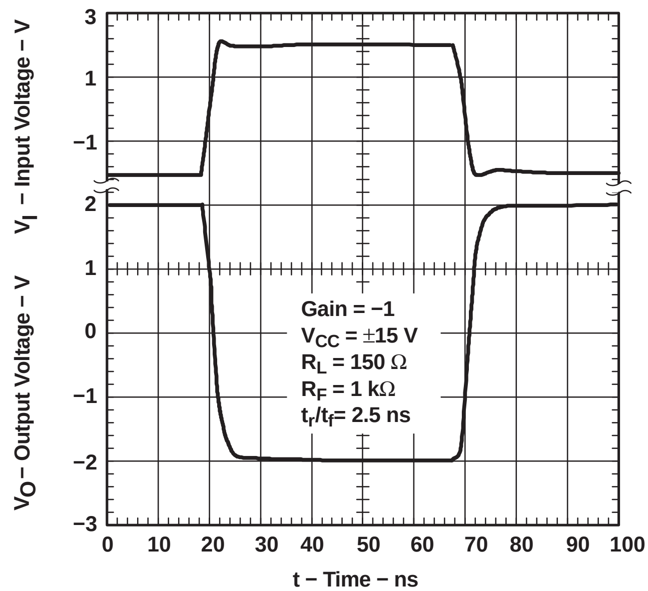


Figure 43.

LARGE SIGNAL PULSE RESPONSE

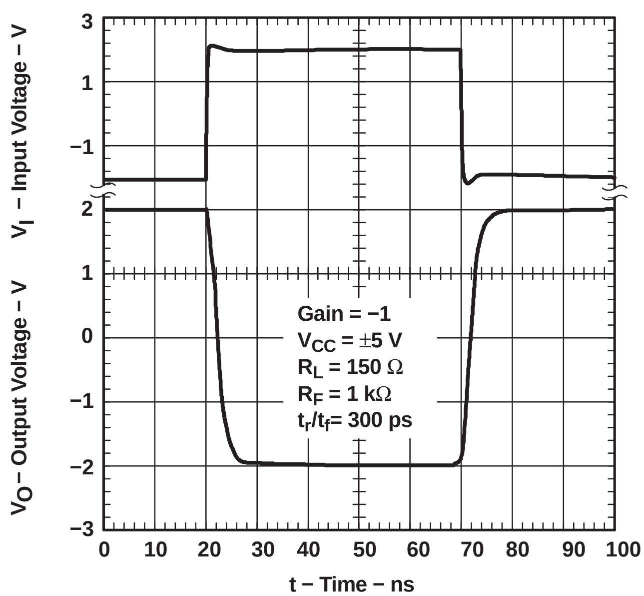


Figure 44.

LARGE SIGNAL PULSE RESPONSE

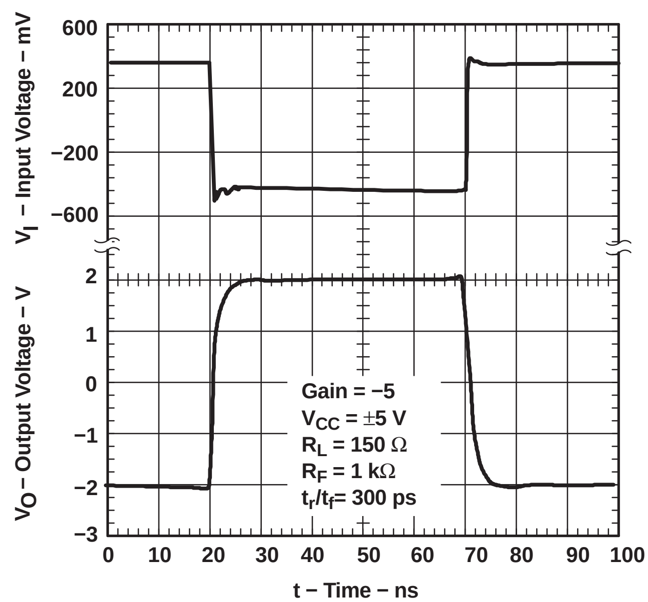


Figure 45.

TYPICAL CHARACTERISTICS (continued)

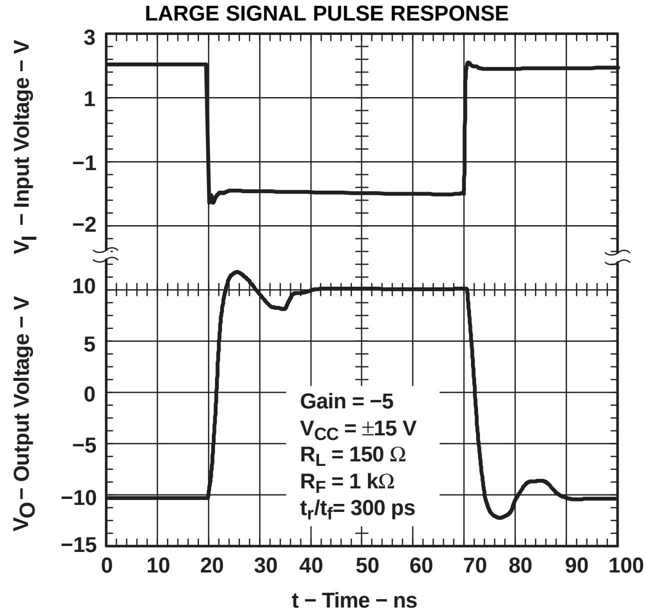


Figure 46.

APPLICATION INFORMATION

THEORY OF OPERATION

The THS3001 is a high-speed, operational amplifier configured in a current-feedback architecture. The device is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 47.

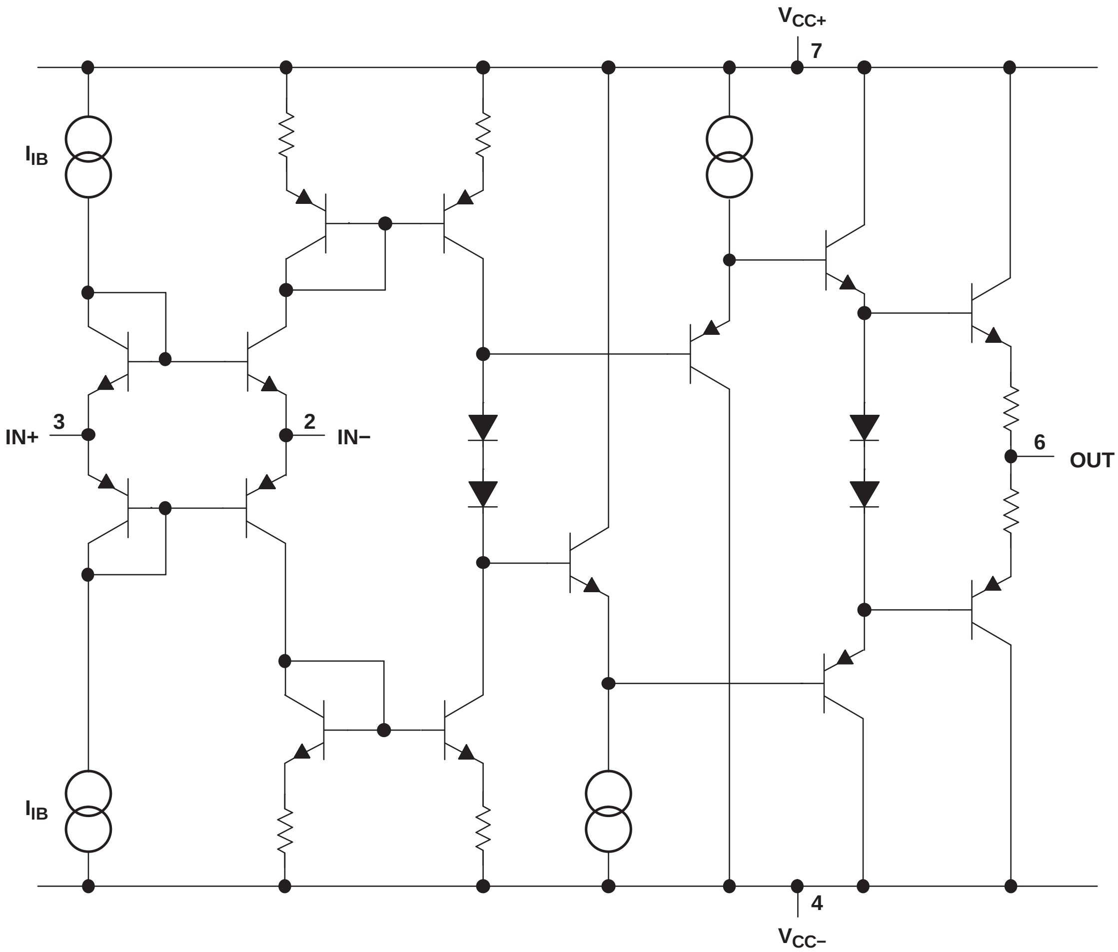


Figure 47. Simplified Schematic

RECOMMENDED FEEDBACK AND GAIN RESISTOR VALUES

The THS3001 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides the excellent isolation and extremely high slew rates that result in superior distortion characteristics.

As with all current-feedback amplifiers, the bandwidth of the THS3001 is an inversely proportional function of the value of the feedback resistor (see Figures 26 to 34). The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 1 kΩ is recommended - a good compromise between bandwidth and phase margin that yields a stable amplifier.

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independent of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage-feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

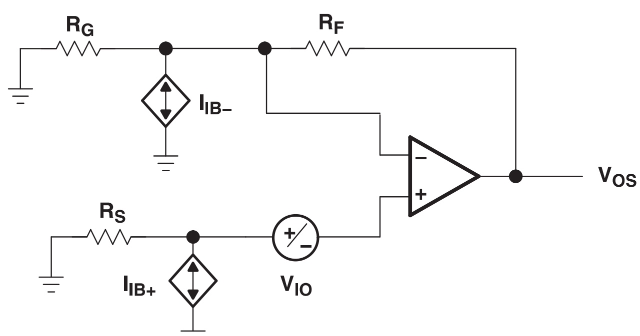
Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion.

Table 1. Recommended Resistor Values for Optimum Frequency Response

GAIN	R_F for V_{CC} = ±15 V	R_F for V_{CC} = ±5 V
1	1 kΩ	1 kΩ
2, -1	680 Ω	750 Ω
2	620 Ω	620 Ω
5	560 Ω	620 Ω

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 48. Output Offset Voltage Model

NOISE CALCULATIONS

Noise can cause errors on small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/√Hz)
- IN+ = Nonverting current noise (pA/√Hz)
- IN- = Inverting current noise (pA/√Hz)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR$_x$)

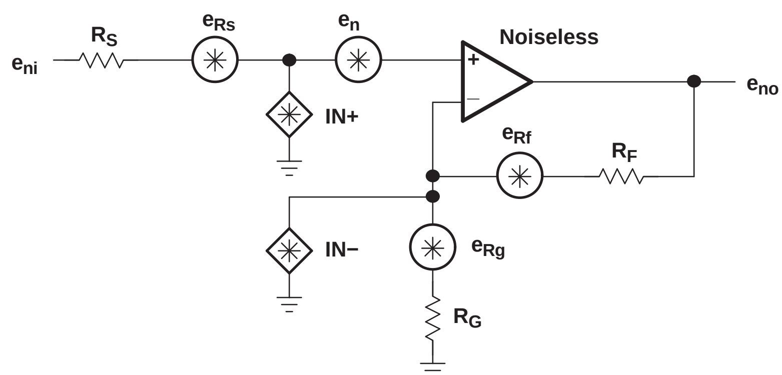


Figure 49. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

SLEW RATE

The slew rate performance of a current-feedback amplifier, like the THS3001, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS3001 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. As can be seen from the specification tables as well as some of the figures in this data sheet, slew-rate performance in the inverting configuration is faster than in the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. Also, if the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes.

Internally, the THS3001 has other factors that impact the slew rate. The amplifier's behavior during the slew-rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1500 V/µs are processed by the input stage in a linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in Figure 50. For slew rates greater than 1500 V/µs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew-rate capabilities. Figure 50 and Figure 51 show waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster-slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input-signal slew rate reduces the effect.

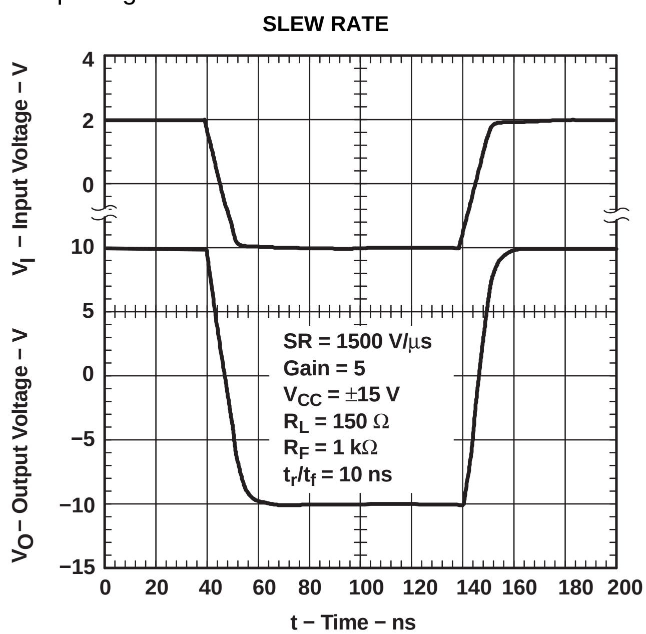


Figure 50.

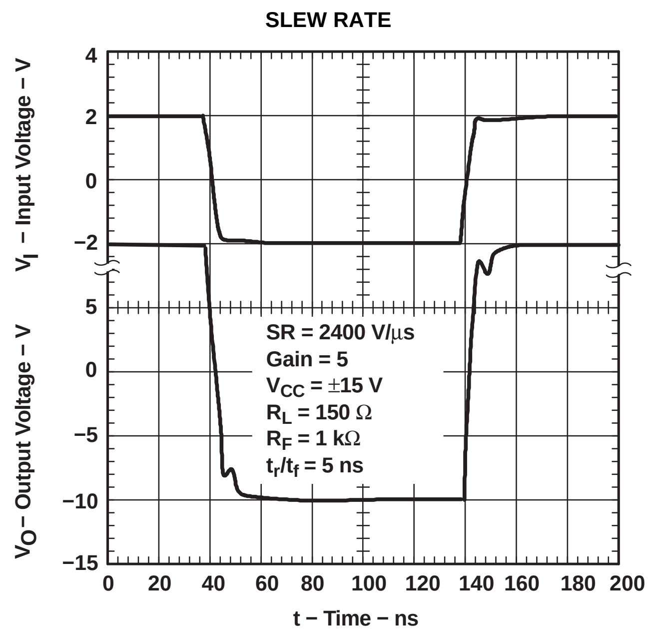


Figure 51.

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS3001 has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 52. A minimum value of 20Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

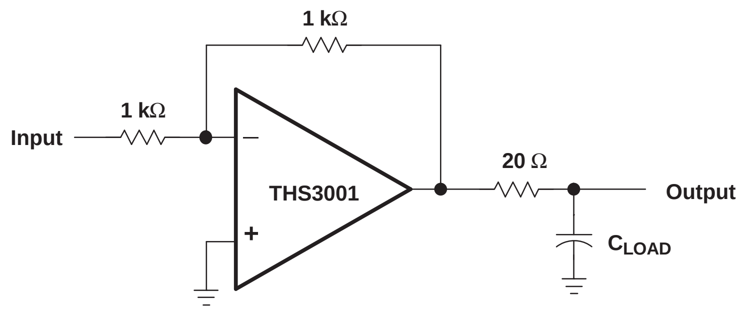


Figure 52. Driving a Capacitive Load

PCB DESIGN CONSIDERATIONS

Proper PCB design techniques in two areas are important to ensure proper operation of the THS3001. These areas are high-speed layout techniques and thermal-management techniques. Because the THS3001 is a high-speed part, the following guidelines are recommended.

- Ground plane - It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection, but should be removed from below the output and negative input pins as noted below.
- The DGN package option includes a thermal pad for increased thermal performance. When using this package, it is recommended to distribute the negative supply as a power plane, and tie the thermal pad to this supply with multiple vias for proper power dissipation. It is not recommended to tie the thermal pad to ground when using split supply (±V) as this will cause worse distortion performance than shown in this data sheet.
- Input stray capacitance - To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 53, which shows what happens when a 1-pF capacitor is added to the inverting input terminal. The bandwidth increases at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, while the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 54, where a 10-pF capacitor adds only 0.35 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially look like a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So proper analysis of adding a capacitor to the inverting input node should be performed for stable operation.

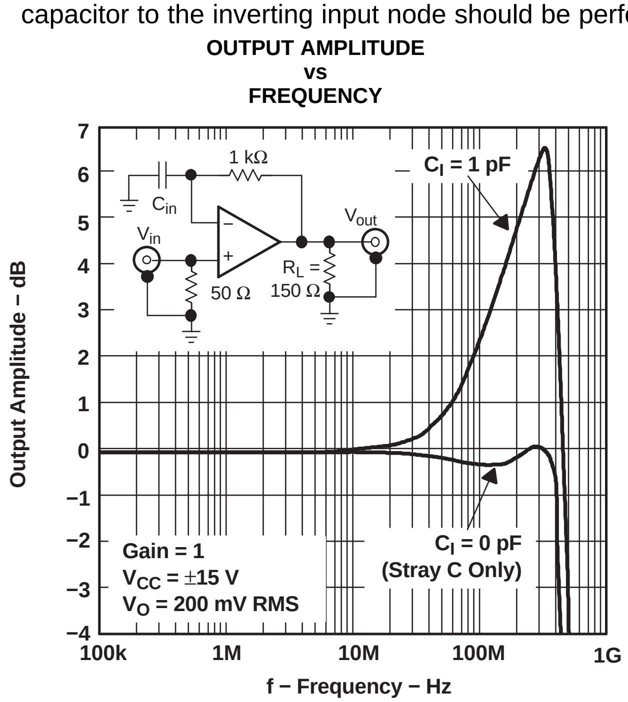


Figure 53.

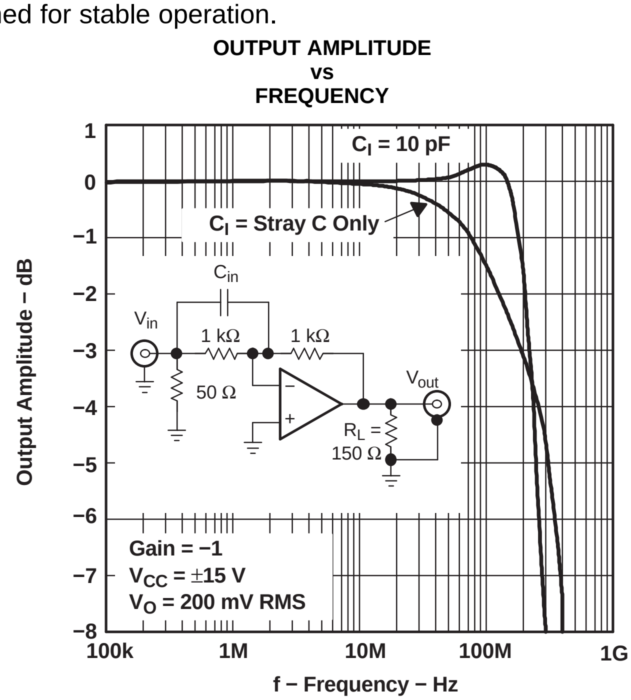


Figure 54.

- Proper power-supply decoupling - Use a minimum 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminal and the ceramic capacitors.

THERMAL INFORMATION

The THS3001 incorporates output-current-limiting protection. Should the output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) is not recommended. Failure of the device is possible under this condition and should be avoided. But, the THS3001 does not incorporate thermal-shutdown protection. Because of this, special attention must be paid to the device's power dissipation or failure may result.

The thermal coefficient θ_{JA} is approximately 169°C/W for the SOIC 8-pin D package. For a given θ_{JA}, the maximum power dissipation, shown in Figure 55, is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS3001 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = Thermal coefficient from die junction to ambient air (°C/W)

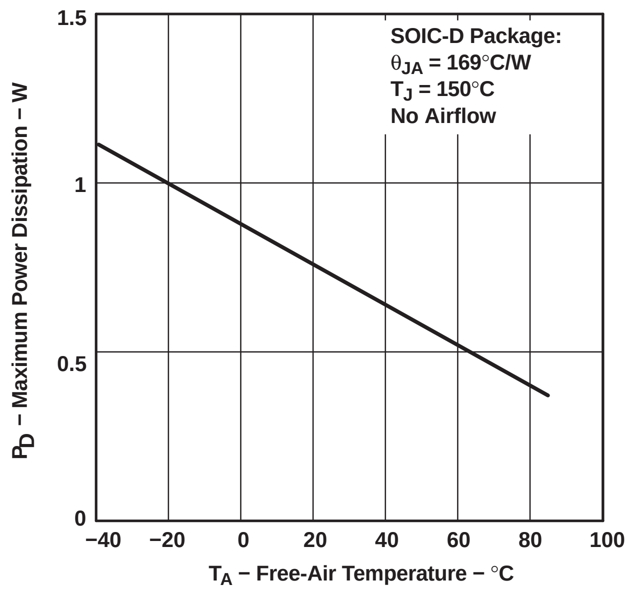
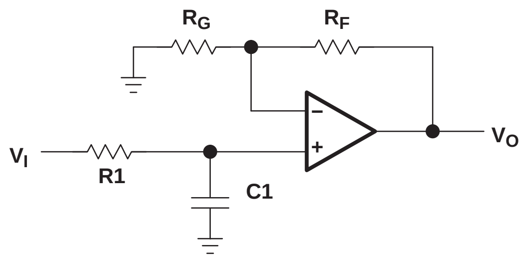


Figure 55. Maximum Power Dissipation vs Free-Air Temperature

GENERAL CONFIGURATIONS

A common error for the first-time CFB user is the creation of a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration will oscillate and is *not* recommended. The THS3001, like all CFB amplifiers, *must* have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 56).

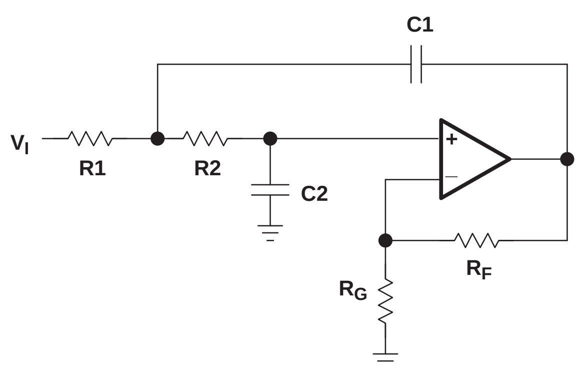


$$f_{-3\,dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 56. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew rates and high bandwidths, CFB amplifiers can create accurate signals and help minimize distortion. An example is shown in Figure 57.



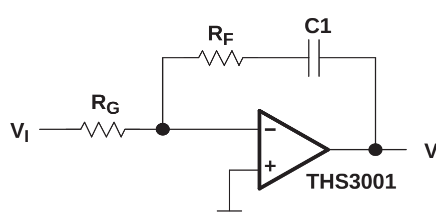
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3\,dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 57. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 58, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 59, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.



$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_FC1}}{S}\right]$$

Figure 58. Inverting CFB Integrator

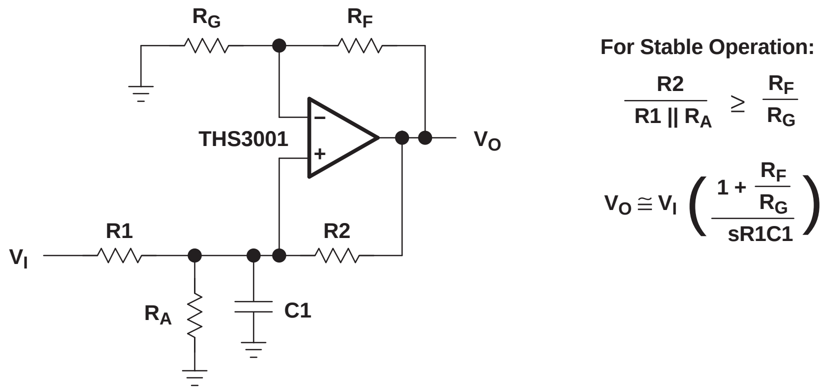


Figure 59. Noninverting CFB Integrator

The THS3001 may also be employed as a good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases (see Figures 22 to 25 for more information). Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

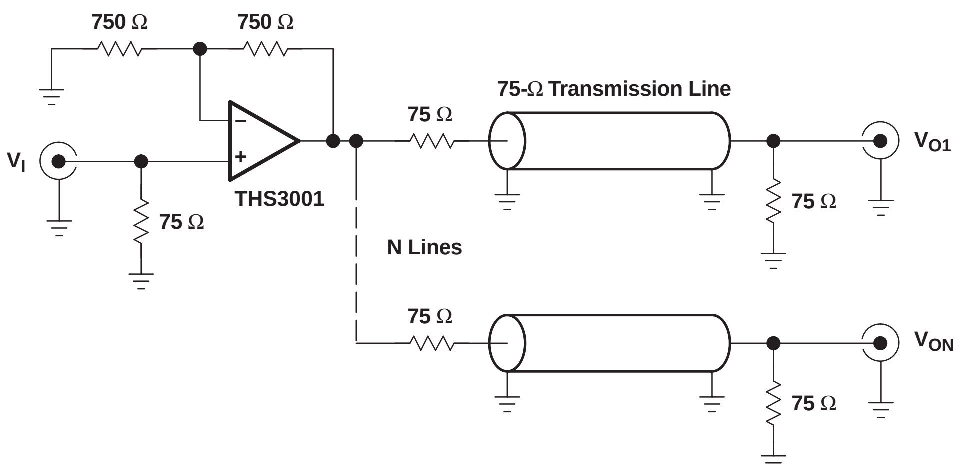


Figure 60. Video Distribution Amplifier Application

EVALUATION BOARD

An evaluation board is available for the THS3001 (THS3001EVM). The board has been configured for low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 61. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more detailed information, refer to the *THS3001 EVM User's Guide* (literature number SLOU021). The evaluation board can be ordered online through the TI web site, or through your local TI sales office or distributor.

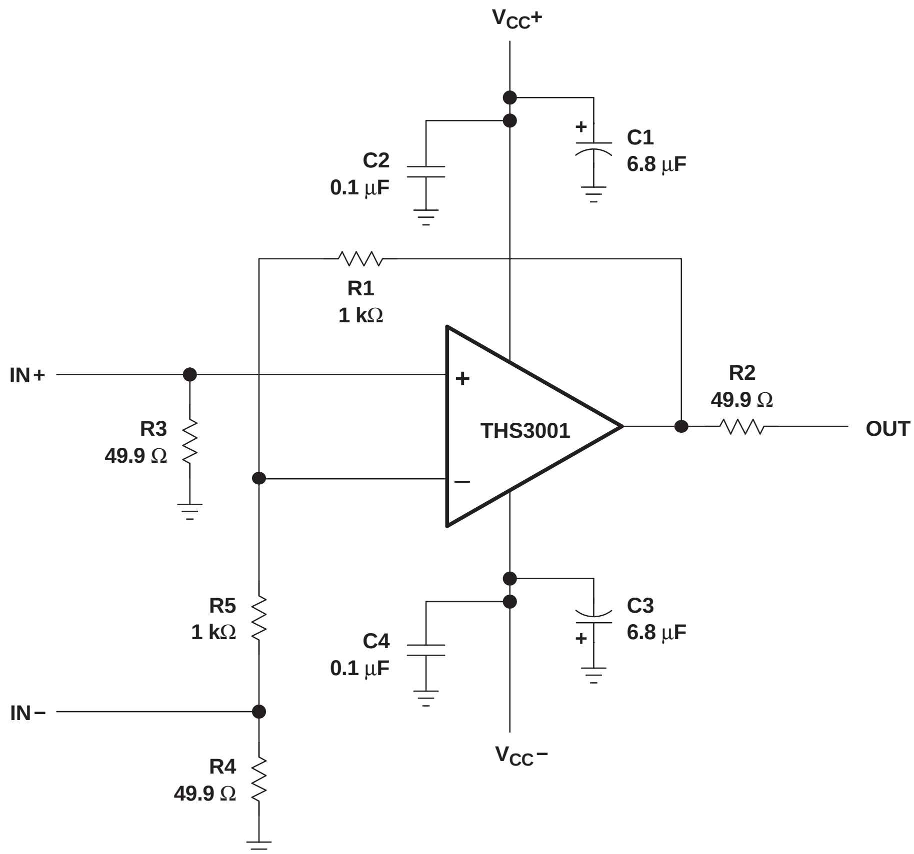


Figure 61. THS3001 Evaluation Board Schematic

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (March, 2008) to Revision H **Page**

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
THS3001CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVCDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVCDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVIDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVIDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVIDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001HVIDGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDGNG4	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDGNRG4	ACTIVE	MSOP-	DGN	8	2500	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
		Power PAD				no Sb/Br)		
THS3001IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3001IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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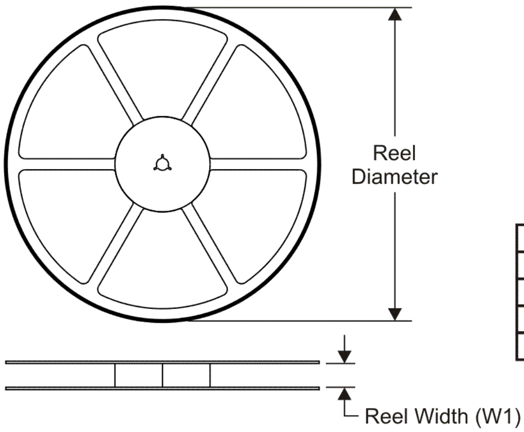
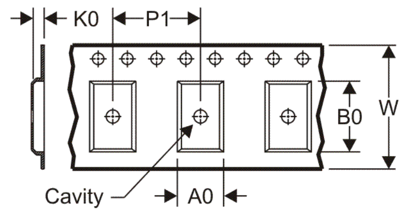
TAPE AND REEL INFORMATION

REEL DIMENSIONS

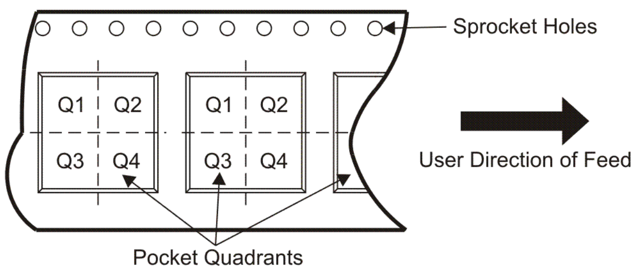


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

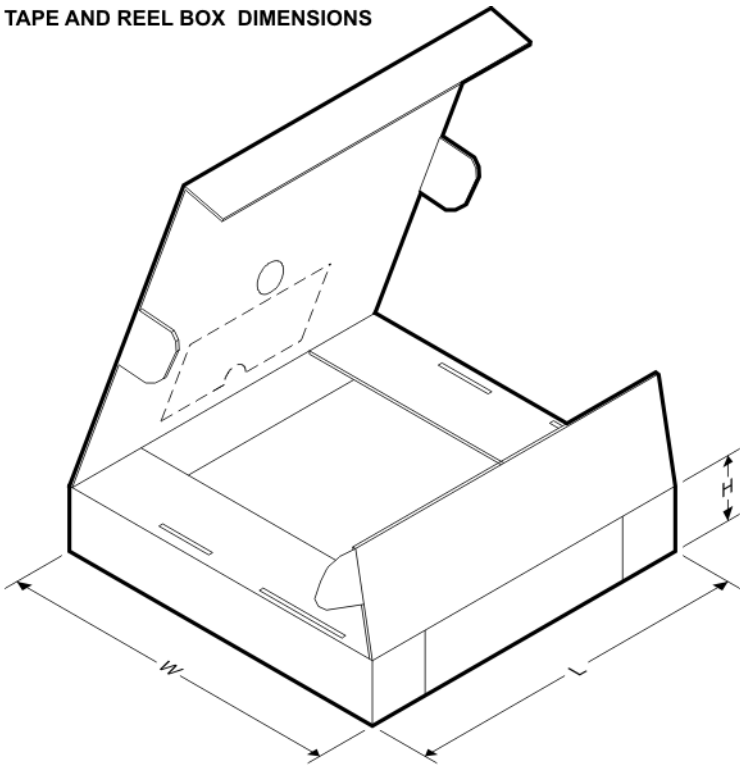
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3001CDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1
THS3001CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3001HVIDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1
THS3001IDGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.2	3.3	1.6	8.0	12.0	Q1
THS3001IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

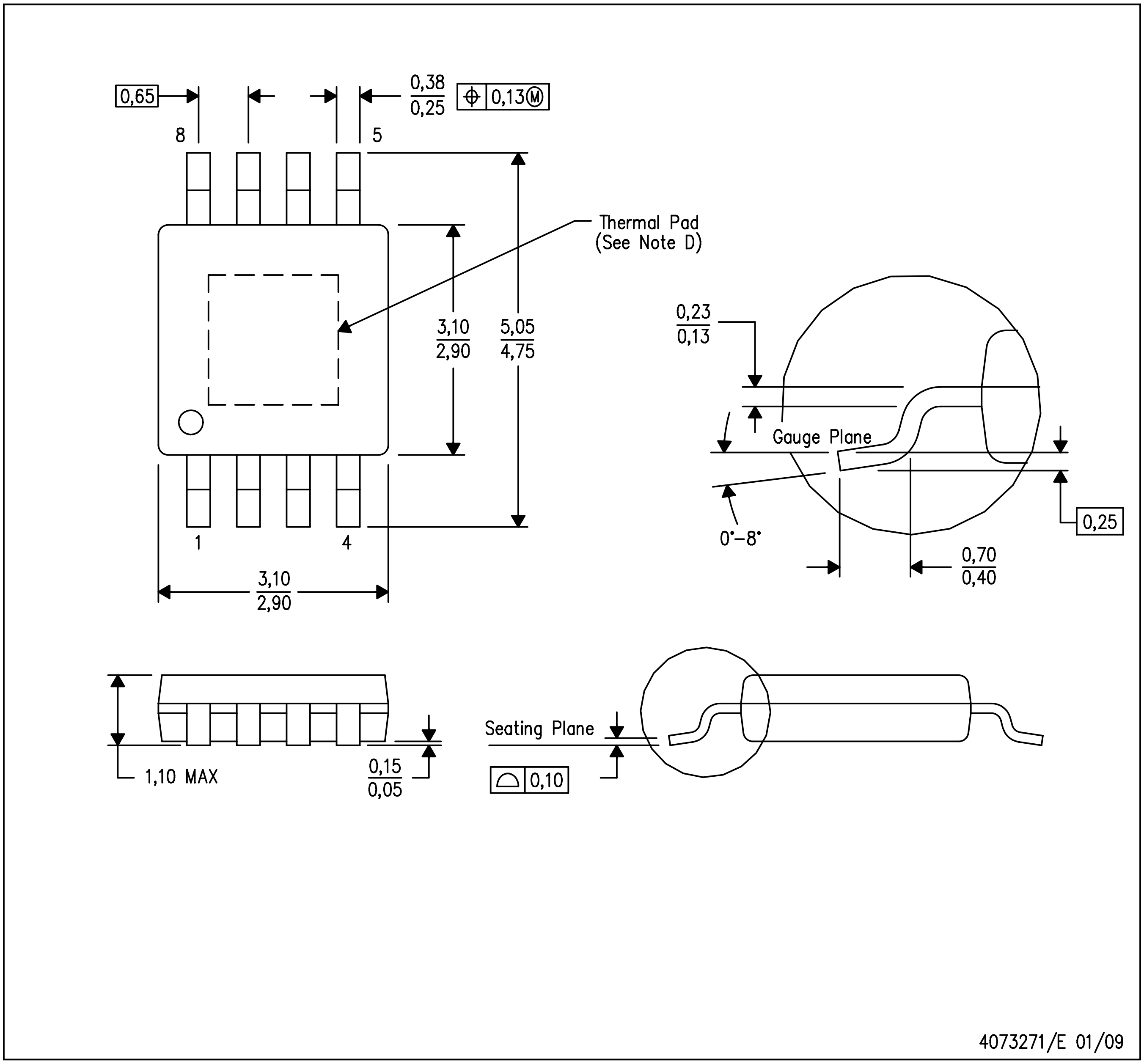
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3001CDGNR	MSOP-PowerPAD	DGN	8	2500	338.1	340.5	21.1
THS3001CDR	SOIC	D	8	2500	346.0	346.0	29.0
THS3001HVIDGNR	MSOP-PowerPAD	DGN	8	2500	338.1	340.5	21.1
THS3001IDGNR	MSOP-PowerPAD	DGN	8	2500	338.1	340.5	21.1
THS3001IDR	SOIC	D	8	2500	346.0	346.0	29.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO-187 variation AA-T

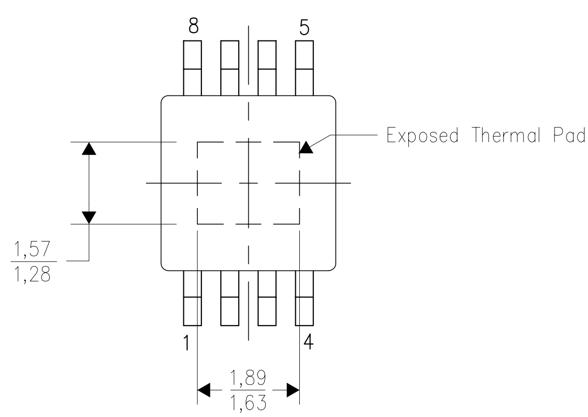
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

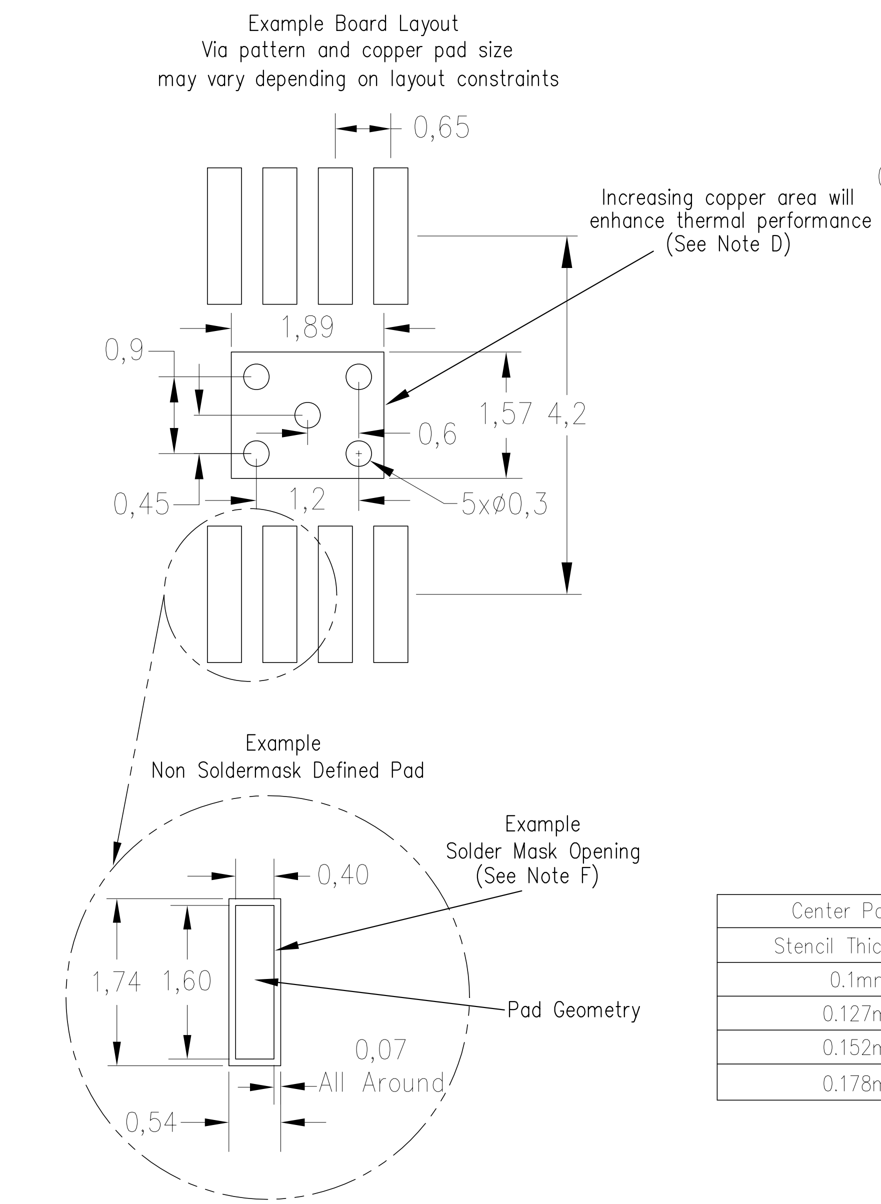


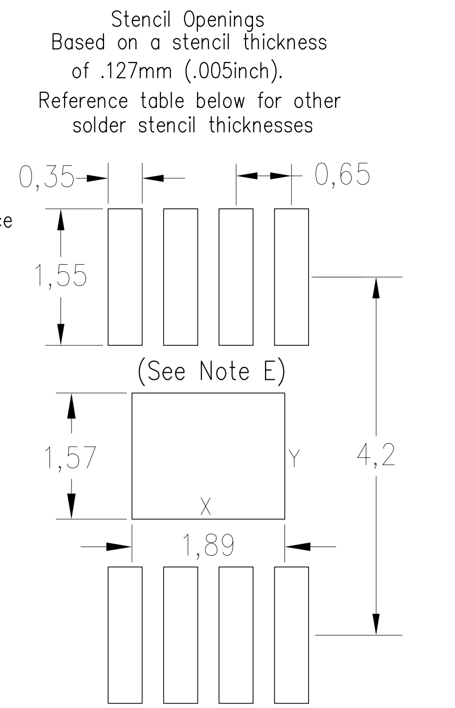
Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDSO-G8) PowerPAD™



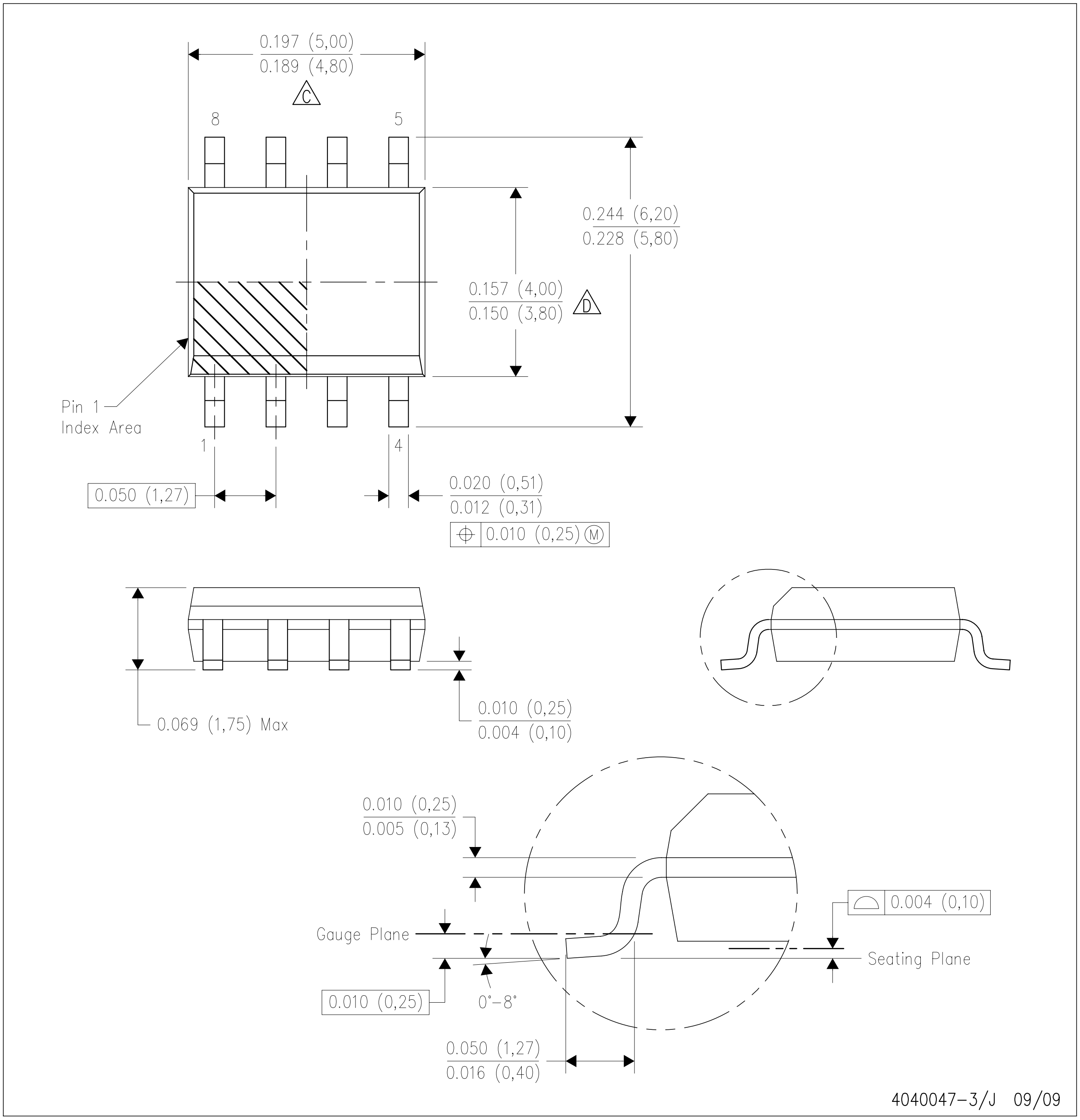


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/D 06/09

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

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Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

TEXAS INSTRUMENTS

THS3001 High Speed Current Feedback Operational Amplifier

User's Guide

March 1999
Mixed-Signal Products

SLOU021A

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Preface

Related Documentation From Texas Instruments

- ***THS3001 HIGH-SPEED CURRENT-FEEDBACK OPERATIONAL AMPLIFIER*** (literature number SLOS217) This is the data sheet for the THS3001 operational amplifier integrated circuit that is used in the THS3001 evaluation module.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Contents

Figures

Tables

Chapter 1

General Information

This chapter details the Texas Instruments (TI™) THS3001 high-speed operational amplifier evaluation module (EVM), SLOP130. It includes a list of EVM features, a brief description of the module illustrated with a pictorial and a schematic diagram, EVM specifications, details on connecting and using the EVM, and a discussion on high-speed amplifier design considerations.

Topic **Page**

1.1 Features

THS3001 operational amplifier EVM features include:

- High Bandwidth — 340 MHz, –3 dB at ±15 V_{CC} & Gain = 2
- ±5-V to ±15-V Operation
- Inverting and Noninverting Single-Ended Inputs
- Module Gain Set to +2 (Noninverting) and –1 (Inverting) — Adjustable Through Component Change.
- Nominal 50-Ω Impedance Inputs and Outputs
- Standard SMA Miniature RF Connectors
- Good Example of High-Speed Amplifier Design and Layout

1.2 Description

The TI THS3001 high-speed current-feedback operational amplifier evaluation module (EVM) is a complete high-speed amplifier circuit. It consists of the TI THS3001 high-speed current-feedback operational amplifier IC, along with a small number of passive parts, mounted on a small circuit board measuring approximately 1.7 inch by 1.4 inch. The EVM uses standard SMA miniature RF connectors for inputs and outputs and is completely assembled, fully tested, and ready to use — just connect it to power, a signal source, and a load (if desired).

Two versions of the THS3001 EVM are available. The original appears in Figure 1–1 and the Rev. A version appears in Figure 1–2.

Figure 1–1. THS3001 Evaluation Module – Original Version

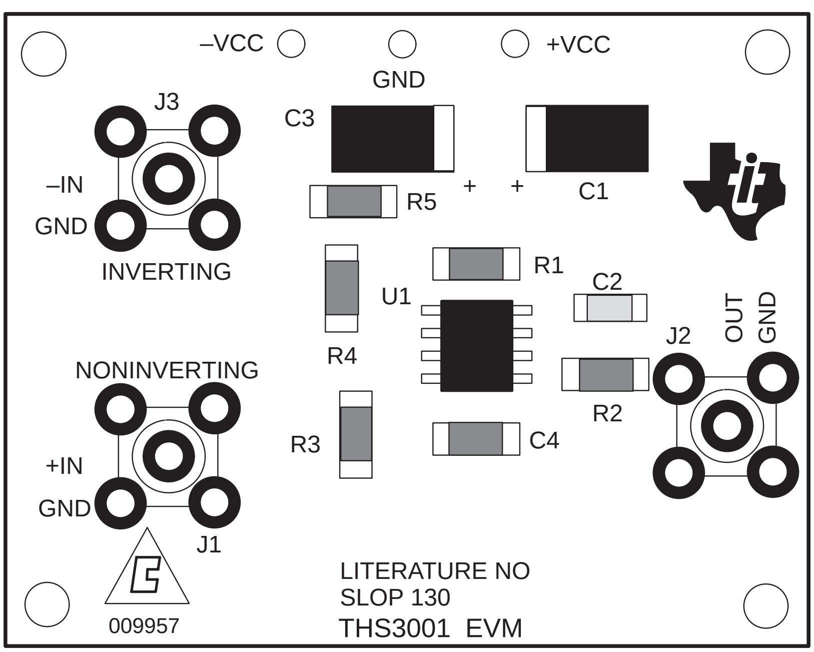
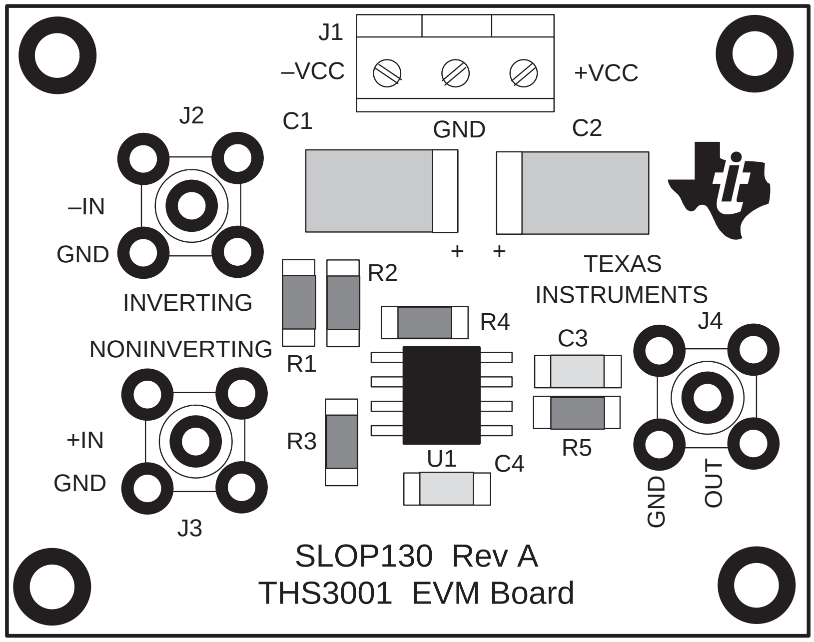


Figure 1–2. THS3001 Rev. A Evaluation Module

Rev. A



The THS3001 EVM is equipped with both noninverting and inverting inputs. The noninverting input is set for a gain of 2 and the inverting input is set for a gain of 1. Each input is terminated with a 50-Ω resistor to provide correct line impedance matching (Figure 1–3 for original version and Figure 1–4 for Rev. A). The amplifier IC output is routed through a 50-Ω resistor both to provide correct line impedance matching and to help isolate capacitive loading on the output of the amplifier. Capacitive loading directly on the output of the IC decreases the amplifier's phase margin and can result in peaking or oscillations.

Figure 1–3. THS3001 EVM Schematic – Original Version

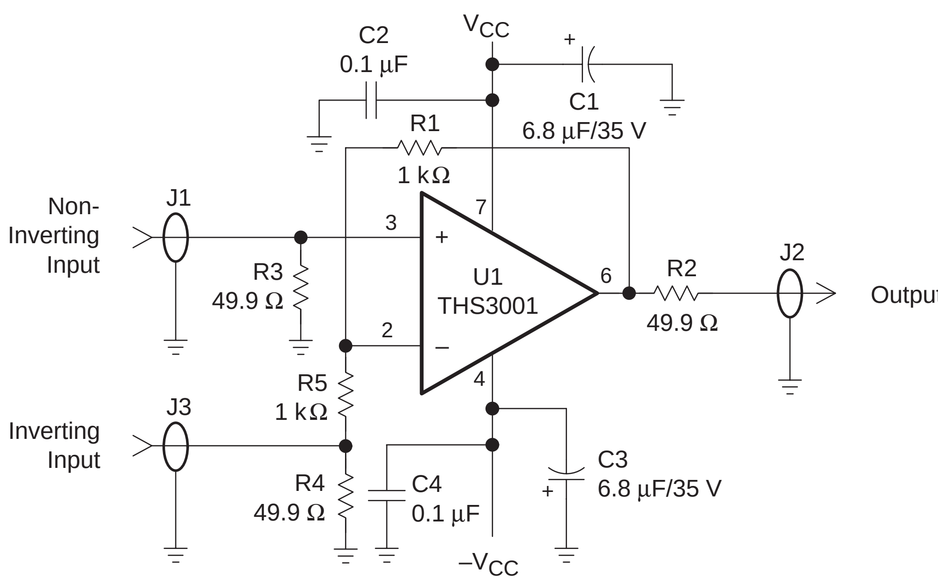
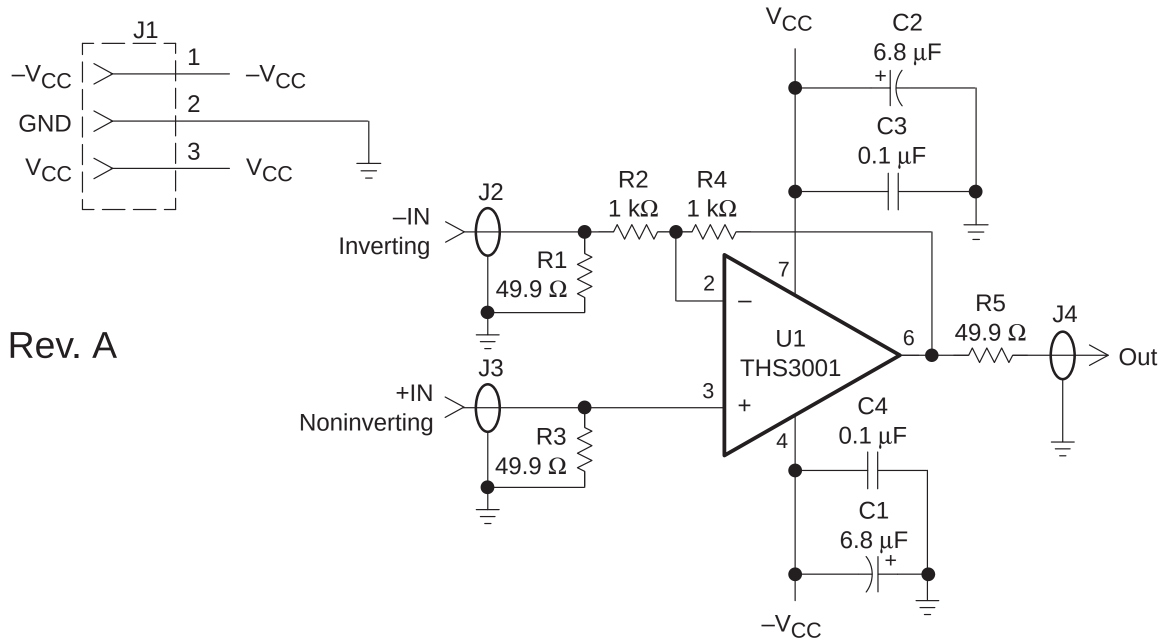


Figure 1–4. THS3001 Rev. A EVM Schematic



Even though the THS3001 is a current-feedback amplifier, the gain of the EVM can easily be changed to support a particular application by simply changing the ratio of resistors R1, R4, and R5 (R1, R2, and R4 for Rev. A) as described in the following equations:

$$Inverting\ Gain = \frac{-R_F}{R_G} = \frac{-R1}{R5} = \frac{-R4}{R2}(Rev.\ A)$$

$$Noninverting\ Gain = 1 + \frac{R_F}{R_G} = 1 + \frac{R1}{R4 + R5} = 1 + \frac{R4}{R2 + R1}(Rev.\ A)$$

In addition, some applications, such as those for video, may require the use of 75-Ω cable and 75-Ω EVM input termination and output isolation resistors.

Any of the resistors on the EVM board can be replaced with a resistor of a different value; however, care must be taken because the surface-mount solder pads on the board are somewhat fragile and will not survive many desoldering/soldering operations.

Because of the current feedback architecture, extra care must be taken to ensure that a feedback resistor is always included in the design. In addition, there must never be a capacitor directly in the feedback path between the amplifier output and the noninverting input. Disregarding this guideline will likely result in a part that oscillates.

Note: External factors can significantly affect the overall gain of the EVM. For example, connecting test equipment with 50-Ω input impedance to the EVM output will divide the output signal level by a factor of 2 (assuming the output isolation resistor on the EVM board remains 50 Ω). Similar effects can occur at the input, depending upon how the input signal sources are configured. The gain equations given above assume no signal loss in either the input or the output.

The EVM circuit board is an excellent example of proper board layout for high-speed amplifier designs and can be used as a guide for user application board layouts.

1.3 THS3001 EVM Specifications

Supply voltage range, $\pm V_{CC}$ . . . . ±5 V to ±15 V
Supply current, I_{CC} . . . . 6.5 mA Typ
Input voltage, V_I . . . . ±VCC, Max
Output drive, I_O . . . . 100 mA, Typ
Continuous power dissipation at T_A = 25°C . . . . 740 mW

For complete THS3001 amplifier IC specifications and parameter measurement information, and additional application information, see the THS3001 data sheet, TI Literature Number SLOS217.

1.4 Using The THS3001 EVM

The THS3001 EVM operates from power-supply voltages ranging from ±5 V to ±15 V. As shipped, the inverting input gain of the module is set to 1, the noninverting input gain is set to 2, and signal inputs on the module are terminated for 50-Ω nominal impedance cables. An oscilloscope is typically used to view and analyze the EVM output signal.

1.4.1 Steps for THS3001 EVM

1) Ensure that all power supplies are set to ***OFF*** before making power supply connections to the THS3001 EVM.
2) Select the operating voltage for the EVM and connect appropriate split power supplies to the pads on the module marked ***–VCC*** and ***+VCC.***
3) Connect the power supply ground to the module pad marked ***GND.***
4) Connect an oscilloscope to the module SMA output connector ***(J2)*** through a 50-Ω nominal impedance cable (an oscilloscope having a 50-Ω input termination is preferred for examining very high frequency signals).
5) Set the power supply to ***ON.***
6) Connect the signal input to either the noninverting input ***(J1)*** for a gain of 2, or to the inverting input ***(J3)*** for a gain of 1.

1.4.2 Steps for THS3001 Rev. A EVM

1) Ensure that all power supplies are set to ***OFF*** before making power supply connections to the THS3001 EVM.
2) Select the operating voltage for the EVM and connect appropriate split power supplies to ***J1*** terminals on the module marked ***–VCC*** and ***+VCC.***
3) Connect the power supply ground to ***J1*** terminal marked ***GND.***
4) Connect an oscilloscope to the module SMA output connector ***(J4)*** through a 50-Ω nominal impedance cable (an oscilloscope having a 50-Ω input termination is preferred for examining very high frequency signals).
5) Set the power supply to ***ON.***
6) Connect the signal input to either the noninverting input ***(J3)*** for a gain of 2, or to the inverting input ***(J2)*** for a gain of 1.

Note that each input connector is terminated with a 50-Ω resistor to ground. With a 50-Ω source impedance, the voltage seen by the THS3001 amplifier IC on the module will be ½ the source signal voltage applied to the EVM.

7) Verify the output signal on the oscilloscope.

Note: The signal shown on an oscilloscope with a 50-Ω input impedance will be ½ the actual THS3001 amplifier IC output voltage. This is due to the voltage division between the output resistor (R2) and the oscilloscope input impedance.

1.5 THS3001 EVM Performance

Figure 1–5 shows the typical frequency response of the THS3001 EVM using the noninverting input (G = 2). Typical values show a –3-dB bandwidth of 340 MHz with a ±15-V power supply and 260 MHz with a ±5-V power supply. They also show a –0.1-dB frequency response of 17 MHz with a ±15-V power supply and 20 MHz with a ±5-V power supply.

Figure 1–5. THS3001 EVM Frequency Response with Gain = 2

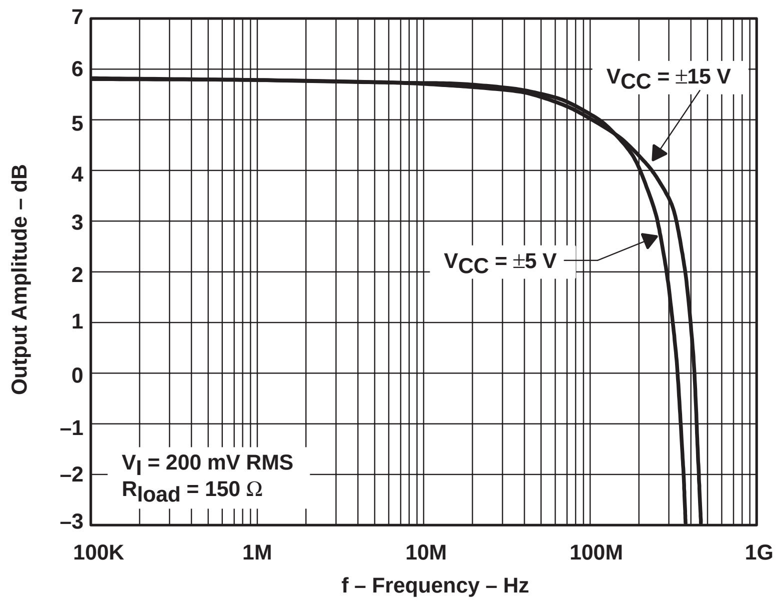
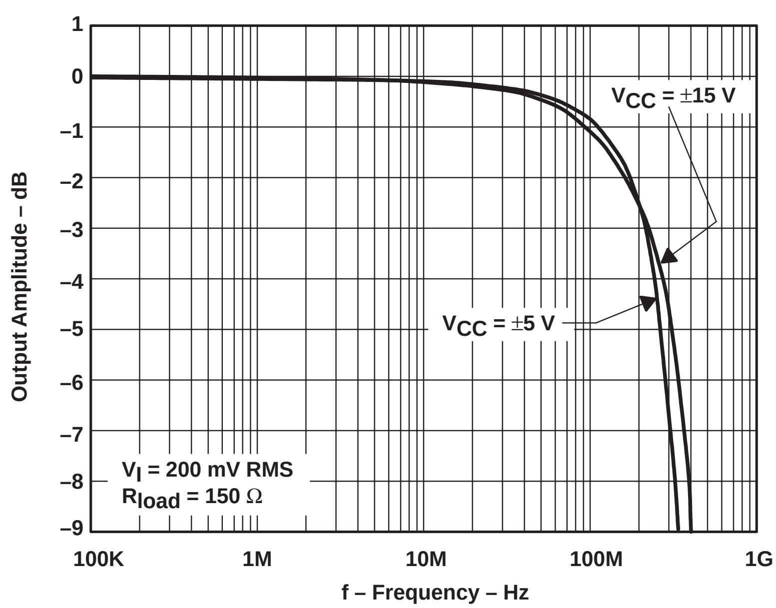


Figure 1–6 shows the typical frequency response of the THS3001 EVM using the inverting input (G = 1). Typical –0.1 dB bandwidths are 15 MHz with a ±15-V power supply and 17 MHz with a ±5-V power supply. Typical –3-dB bandwidths are 220 MHz at ±15-V and 210 MHz at ±5-V.

Figure 1–6. THS3001 EVM Frequency Response with Inverting Gain = 1



1.6 General High-Speed Amplifier Design Considerations

The THS3001 EVM layout has been designed and optimized for use with high-speed signals and can be used as an example when designing THS3001 applications. Careful attention has been given to component selection, grounding, power supply bypassing, and signal path layout. Disregard of these basic design considerations could result in less than optimum performance of the THS3001 high-speed, current-feedback video operational amplifier.

Surface-mount components were selected because of the extremely low lead inductance associated with this technology. Also, because surface-mount components are physically small, the layout can be very compact. This helps minimize both stray inductance and capacitance.

Tantalum power supply bypass capacitors (C1 and C3 for original and C1 and C2 for Rev. A) at the power input pads help supply currents for rapid, large signal changes at the amplifier output. The 0.1 μF power supply bypass capacitors (C2 and C4 for original version and C3 and C4 for Rev. A) were placed as close as possible to the IC power input pins in order to keep the PCB trace inductance to a minimum. This improves high-frequency bypassing and reduces harmonic distortion.

A proper ground plane on both sides of the PCB should always be used with high-speed circuit design. This provides low-inductive ground connections for return current paths. In the area of the amplifier IC input pins, however, the ground plane was removed to minimize stray capacitance and reduce ground plane noise coupling into these pins. This is especially important for the inverting pin while the amplifier is operating in the noninverting mode. Because the voltage at this pin swings directly with the noninverting input voltage, any stray capacitance would allow currents to flow into the ground plane, causing possible gain error and/or oscillation. Capacitance variations at the amplifier IC inverting input pin of less than 1 pF can significantly affect the response of the amplifier.

In general, it is always best to keep signal lines as short and as straight as possible. Sharp 90° corners should be avoided — round corners or a series of 45° bends should be used, instead. Stripline techniques should also be incorporated when signal lines are greater than three inches in length. These traces should be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Such signal lines should also be properly terminated with an appropriate resistor.

Finally, proper termination of all inputs and outputs should be incorporated into the layout. Unterminated lines, such as coaxial cable, can appear to be a reactive load to the amplifier IC. By terminating a transmission line with its characteristic impedance, the amplifier’s load then appears to be purely resistive and reflections are absorbed at each end of the line. Another advantage of using an output termination resistor is that capacitive loads are isolated from the amplifier output. This isolation helps minimize the reduction in amplifier phase-margin and improves the amplifier stability for improved performance such as reduced peaking and settling times.

Chapter 2

Reference

This chapter includes a parts list and PCB layout illustrations for the THS3001 EVM and the THS3001 Rev. A EVM.

Topic **Page**

2.1 THS3001 High-Speed Current-Feedback Video Operational Amplifier EVM Parts List

Table 2–1. THS3001 EVM Parts List

Reference	Description	Size	Manufacturer/Digi-Key Part Number
C1, C3	Capacitor, 6.8 μF, 35 V, SM	D	Sprague 293D685X9035D2T
C2, C4	Capacitor, 0.1 μF, ceramic, 10%, SM	1206	Sprague 11C1201E104M5NT
J1, J2, J3	Connector, SMA 50-Ω vertical PC mount, through-hole		Amphenol ARF1205–ND
R2, R3, R4	Resistor, 49.9 Ω, 1%, 1/10 W, SM	1206	Digi-Key P49.9CTR–ND
R1, R5	Resistor, 1 kΩ, 1%, 1/10 W, SM	1206	Digi-Key P1.0KCTR–ND
U1	IC, THS3001, operational amplifier	SOIC-8	TI THS3001
PCB1	PCB, THS3001 EVM		

2.2 THS3001 EVM Board Layouts

Board layout examples of the THS3001 EVM PCB are shown in the following illustrations. They are not to scale and appear here only as a reference.

Figure 2–1. THS3001 EVM Component Placement Silkscreen and Solder Pads

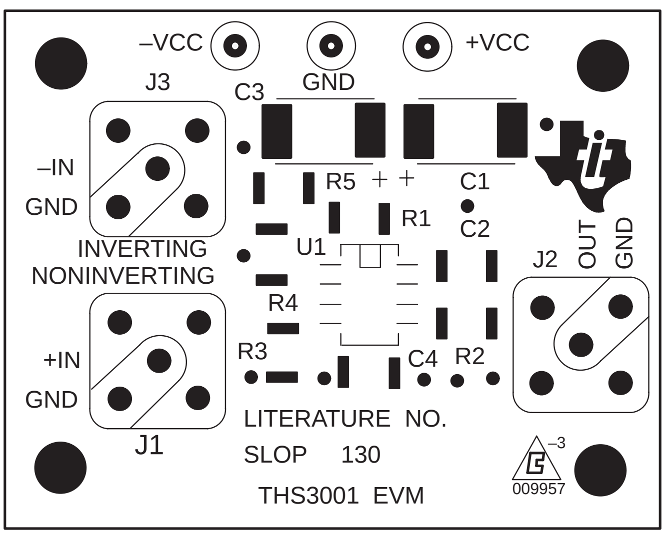


Figure 2–2. THS3001 EVM PC Board Layout – Component Side

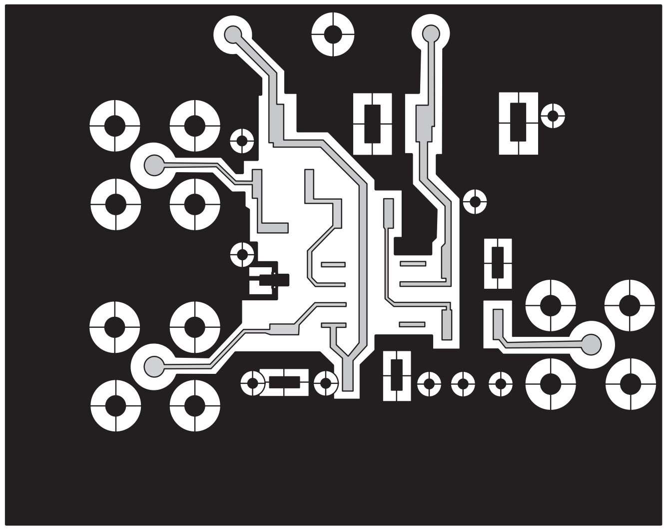
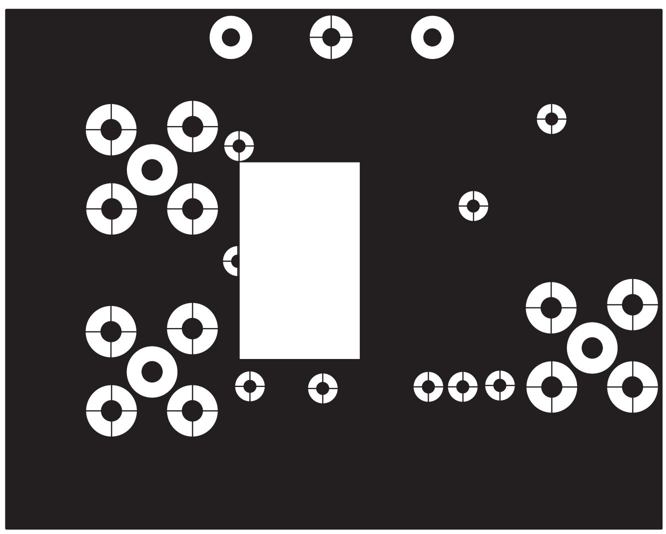


Figure 2–3. THS3001 EVM PC Board Layout – Back Side



2.3 THS3001 Rev. A High-Speed Operational Amplifier EVM Parts List

Table 2–2. THS3001 Rev. A EVM Parts List

Reference	Description	Size	Manufacturer/Digi-Key Part Number
C1, C2	Capacitor, 6.8 µF, 35 V, SM	D	Sprague 293D685X9035D2T
C3, C4	Capacitor, 0.1 µF, ceramic, 10%, SM	1206	Sprague 11C1201E104M5NT
J1	Terminal Block		Digi-Key ED1515–ND
J2, J3, J4	Connector, SMA 50-Ω vertical PC mount, through-hole		Amphenol ARF1205–ND
R1, R3, R5	Resistor, 49.9 Ω, 1%, 1/8 W, SM	1206	Digi-Key P49.9CTR–ND
R2, R4	Resistor, 1 kΩ, 1%, 1/8 W, SM	1206	Digi-Key P1.0KCTR–ND
U1	IC, THS3001, operational amplifier	SOIC-8	TI THS3001
PCB1	PCB, THS3001 Rev. A EVM		

2.4 THS3001 Rev. A EVM Board Layouts

Board layout examples of the THS3001 Rev. A EVM PCB are shown in the following illustrations. They are not to scale and appear here only as a reference.

Figure 2–4. THS3001 Rev. A EVM Component Placement Silkscreen and Solder Pads

Rev. A

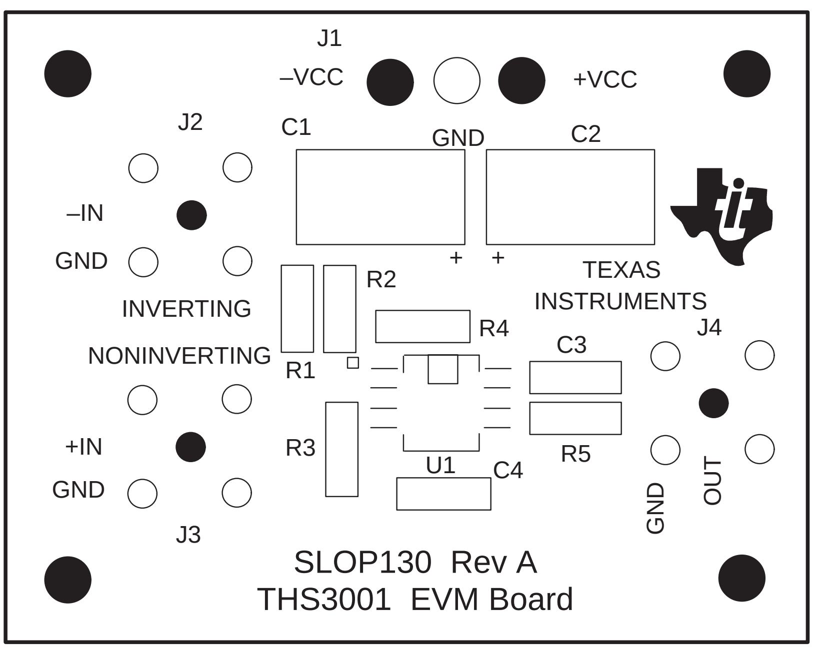


Figure 2–5. THS3001 Rev. A EVM PC Board Layout – Component Side

Rev. A

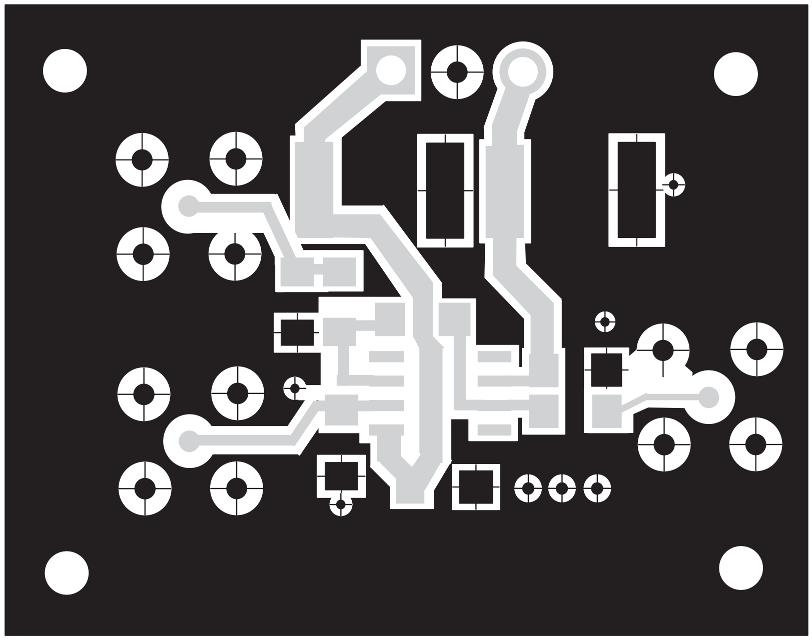


Figure 2–6. THS3001 Rev. A EVM PC Board Layout – Back Side

Rev. A