

# TrueView™ 5725

## Multimedia Processor for HD PTV and LCD TV

The TrueView™ 5725 is a low pin count, low-cost of advanced and highly integrated Digital and Analog Video Display Processor providing the key features needed to design HD-READY, progressive scan or LCD Televisions.

TrueView™ 5725 accepts interlaced or progressive video input and graphic input such as NTSC/PAL, 1080i/720p, and SXGA, etc. in both analog and digital channels. It provides a high quality display output. It is capable of advanced de-interlacing, video enhancement, advanced 3D noise reduction, Y/C cross talk suppression and frame rate conversion. It also provides superior video output quality.

It integrates a complete triple 8-bit pipeline ADC with a clock-recovery and sync separation circuit to generate the sampling clock from HSYNC. An additional 24bit digital input is also provided for applications such as picture in picture (PIP).

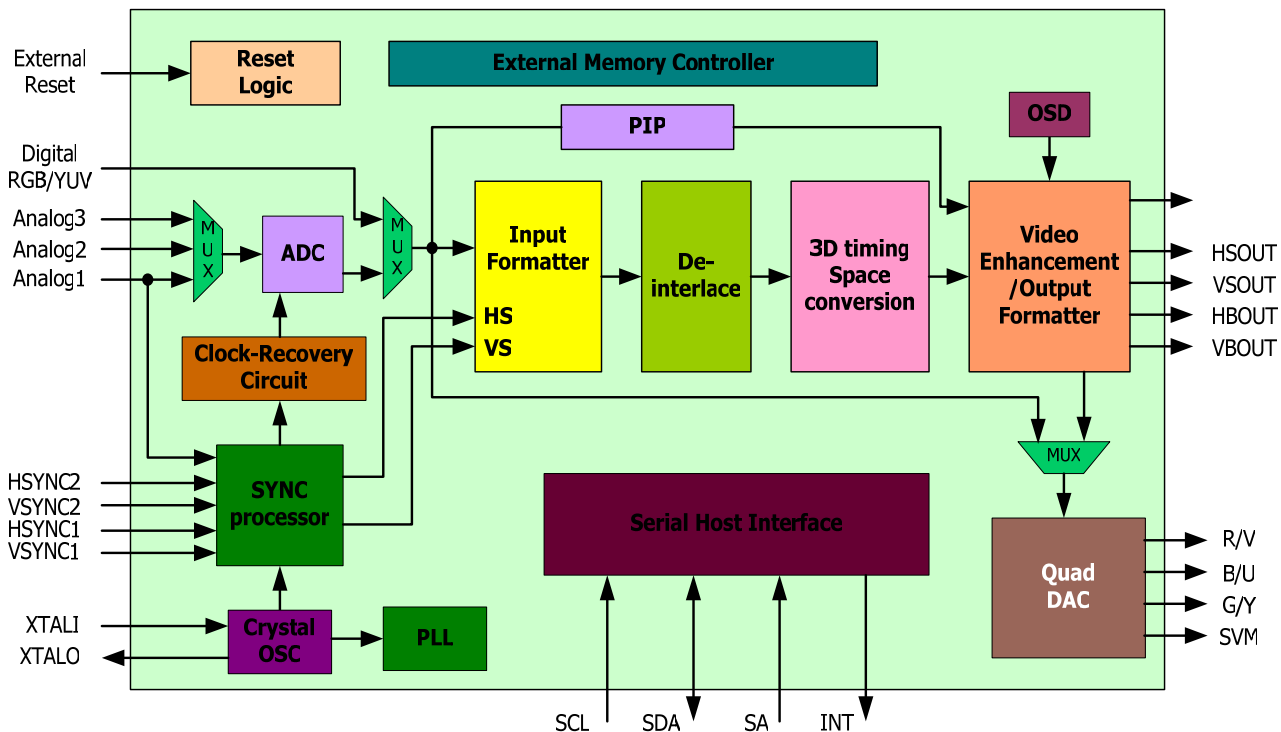
With the high quality video DACs, the video stream is

displayed through its de-interlaced RGB/YPbPr outputs.

The I2C host interface enables OEMs to select from many different CPU's in order to meet their system and technical requirements.

OEMs can easily design a very low cost solution, while minimizing their software development time by leveraging on TV5725's level of integration and software support.

TrueView™5725 provides 3D motion adaptive de-interlacing with diagonal edge detection. It performs high quality line doubling and high-accuracy non-linear motion estimation. It performs pixel based motion detection using two-field buffers. The Video De-interlacing Processor automatically detects noise level and can respond to different noise thresholds. It can also automatically detect input modes such as still images, 3:2 / 2:2 two film and provide adaptive processing.



## TrueView 5725™ FEATURES

### ■ Analog Input Formatter

- Max three channels analog inputs
- RGB/YCbCr/YPbPr input
- Analog input range: 0.5V – 1.0V (p-p)
- Programmable gain/offset controls
- DC or AC coupling inputs
- Internal sync separator to support SOG/SOY
- SXGA (1280x1024 @ 75Hz) at 135MHz
- HDTV up to 1080P
- Supports Macrovision input

### ■ Triple 8-bit ADC

- Maximum analog sampling rate up to 162MSPS

### ■ Clock-recovery Circuit

- Programmable phase adjustment cells
- HSYNC frequency range is from 15KHz to 110KHz

### ■ Digital Input Formatter

- 24bit RGB/YUV input
- 8/16bit YUV input
- 8bit 656/601 input
- NTSC/PAL input
- 480P, 576P input
- VGA/SVGA/XVGA input
- 720P, 1080i, 1080P HD input
- Support DVI interface

### ■ Output formatter

- 480P, 576P, 720P, 1080i, 1080P
- Up to SXGA graphic output formats
- 100/120 interlace double scan
- 75Hz interlace single scan
- 50-75Hz scan rate conversion
- 15~80KHz horizontal frequency
- 16bit YPbPr digital output with syncs
- 24bit YPbPr/RGB digital output with syncs

### ■ De-interlacer

- HD 1080i support
- SD NTSC/PAL
- Direct Edge Correction De-interlace
- Motion Detection
- Edge Detection

- Mode Detection
- Noise Detection
- 3:2/2:2 pull-down detection

### ■ Memory Controller

- 2-8Mbyte memory support
- 16/32bit data access

### ■ Video Enhancement

- Black Level Expansion (BLE)
- White Level Expansion (WLE)
- Color Transition Improvement (DCTI)
- Dynamic Range expansion
- Brightness, Saturation, Contrast, HUE
- Dynamic 2D Peaking
- 2D coring
- 3D noise reduction
- Scan Velocity Modulation (SVM)
- 2D Nonlinear scaling
- Primary Color Enhancement
- Skin Tone Enhancement
- Blue Stretch

### ■ PIP

- Support board-level PIP using an external video decoder/ADC
- Provide timing synchronizing for both Main and PIP channels
- Internal overlay on Main/PIP
- Only 2M external memory needed for PIP channel

### ■ OSD

- Simple OSD generator to support component video inputs

### ■ Host Interface and I/O

- Two-wire I2C interface
- GPIO

### ■ Quadruple 10bit DAC

### ■ Package and Technology

- 160-pin QFP
- 0.18 micron, 3.3V/1.8V technology

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