CMOS 4-BIT D-TYPE REGISTER

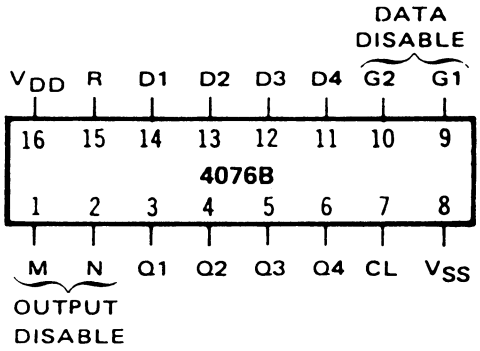
FEATURES

- 3-State Outputs with Gated Control Lines
- Fully Independent Clock
- Asynchronous Reset
- Fully Static Operation - DC to 12MHz @ 10Vdc

DESCRIPTION

The 4076B 4-bit Register consists of four D-Type flip-flops operating synchronously from a common Clock. OR-gated Output Disable inputs force the outputs into a high-impedance state for use in bus-organized systems. OR-gated Data Disable inputs cause the Q outputs to be fed back to the D inputs of the flip-flops. Thus, they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous Master Reset is provided to clear all four flip-flops simultaneously independent of the Clock or Disable inputs.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

C 16-pin Cerdip

E 16-pin Epoxy

TRUTH TABLE

Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⌐	1	X	X	Q	NC
0	⌐	X	1	X	Q	NC
0	⌐	0	0	1	1	
0	⌐	0	0	0	0	
0	1	X	X	X	Q	NC
0	⌙	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

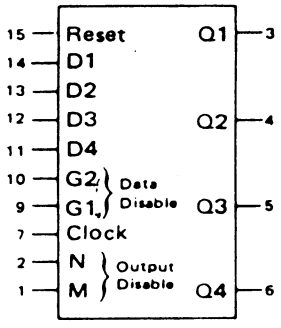
1 ≡ High Level X = Don't Care
0 ≡ Low Level NC = No Change

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

BLOCK DIAGRAM



VDD = Pin 16
VSS = Pin 8

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

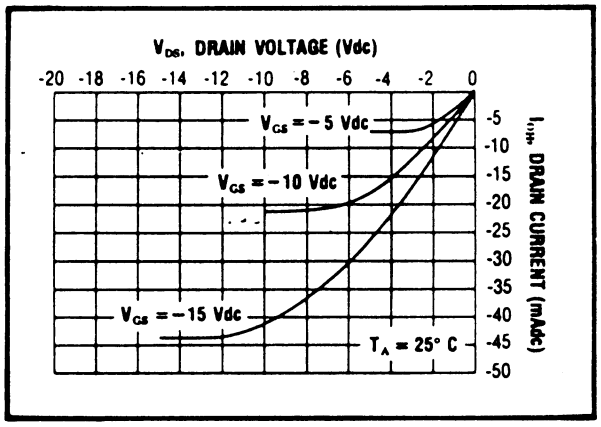
PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid input	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

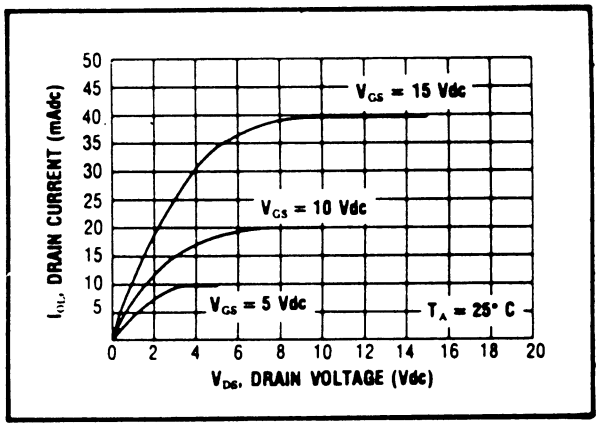
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME						
Clock to Q	t_{PLH}, t_{PHL}	5	–	150	300	ns
		10	–	70	140	
		15	–	45	90	
Output Disable to Q	t_{PHZ}, t_{PLZ}	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
	t_{PZH}, t_{PZL}	5	–	80	160	ns
		10	–	35	70	
		15	–	25	50	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	80	160	ns
		10	–	40	80	
		15	–	30	60	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	3.0	6.0	–	MHz
		10	6.0	12	–	
		15	8.0	16	–	
MAXIMUM CLOCK RISE & FALL TIME[1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM SETUP TIME						
Data Inputs	t_{setup}	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
Data Disable Inputs	t_{setup}	5	–	100	200	ns
		10	–	60	120	
		15	–	45	90	
MINIMUM HOLD TIME						
All Inputs	t_{hold}	5	–	75	150	ns
		10	–	35	70	
		15	–	30	60	
RESET OPERATION						
PROPAGATION DELAY TIME	t_{PHL}	5	–	200	400	ns
		10	–	100	200	
		15	–	75	150	
MINIMUM RESET PULSE WIDTH	PW_R	5	–	75	150	ns
		10	–	40	80	
		15	–	30	60	
RESET REMOVAL TIME	t_{rem}	5	–	100	200	ns
		10	–	60	120	
		15	–	45	90	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

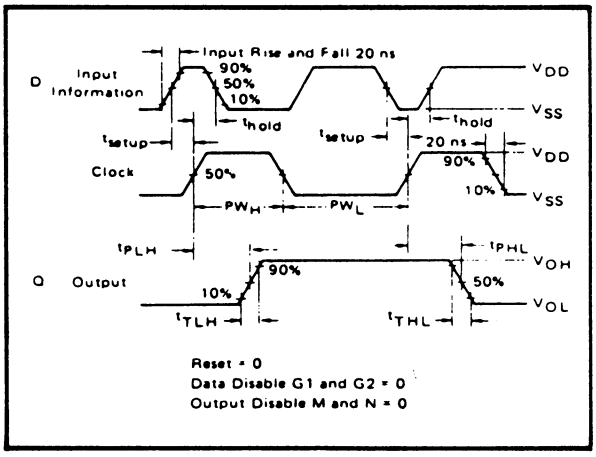


Typical P-Channel
Source Current Characteristics

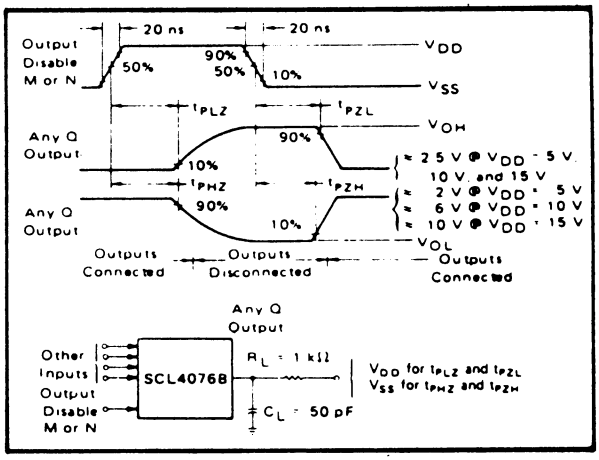


Typical N-Channel
Sink Current Characteristics

TIMING DIAGRAM



THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT



LOGIC DIAGRAM