

CMOS DUAL 2-WIDE, 2-INPUT AND-OR-INVERTER GATE

FEATURES

- Medium-speed operation — $t_{pHL} = 90 \text{ ns}$;
 $t_{pLH} = 125 \text{ ns}$ (typ.) at 10 V
- Individual inhibit controls
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 18 V
- Maximum input current of $1 \mu\text{A}$ at 15 V over full temperature range; 100 nA at 15 V and 25°C
- Noise margin (over full package-temperature range):
 - 1 V at $V_{DD} = 5 \text{ V}$
 - 2 V at $V_{DD} = 10 \text{ V}$
 - 2.5 V at $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

DESCRIPTION

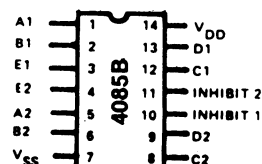
The 4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

RECOMMENDED OPERATING CONDITIONS

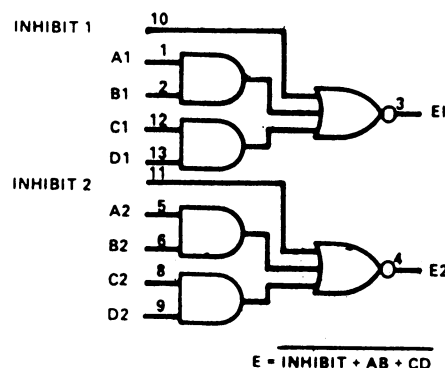
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For $T_A = \text{Full}$ Package Temperature Range)	3	18	V

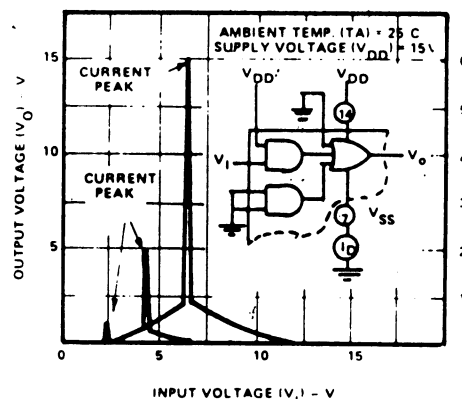
CONNECTION DIAGRAM



TOP VIEW



FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	0.05	—	0.0005	0.05	—	1.5	μA _{dc}
			—	0.10	—	0.001	0.10	—	3.0	
			—	0.20	—	0.002	0.20	—	6.0	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C
 = -40°C for E
 T_{HIGH} = +125°C for C
 = +85°C for E

ABSOLUTE MAXIMUM RATINGS

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) -0.5 to +20V

INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C
 (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C
 (PACKAGE TYPE E) Derate Linearly

at 12 mW/°C to 200 mW

For T_A = -55 to +100°C
 (PACKAGE TYPES D, F, C) 500 mW

For T_A = +100 to +125°C
 (PACKAGE TYPES D, F, C) . Derate Linearly

at 12 mW/°C to 200 mW

DEVICE DISSIPATION

PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100 mW

OPERATING TEMPERATURE RANGE (T_A):

PACKAGE TYPE C -55 to +125°C

PACKAGE TYPE E -40 to +85°C

STORAGE TEMPERATURE

RANGE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
 from case for 10 s max. +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS

(T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50pF, R_L = 200 KΩ)

CHARACTERISTICS		CONDITIONS		LIMITS		UNITS
		V _{DD}		Typ.	Max.	
Propagation Delay Time (Data): High-to-Low Level	t _{PHL}	5		225	450	ns
		10		90	180	
		15		65	130	
Low-to-High Level	t _{PLH}	5		310	620	ns
		10		125	250	
		15		90	180	
Propagation Delay Time (Inhibit): High-to-Low Level	t _{PHL}	5		150	300	ns
		10		60	120	
		15		40	80	
Low-to-High Level	t _{PLH}	5		250	500	ns
		10		100	200	
		15		70	140	
Transition Time t _{THL} , t _{TLH}	t _{THL} , t _{TLH}	5		100	200	ns
		10		50	100	
		15		40	80	
Input Capacitance	C _{IN}	Any Input		5	7.5	pF

