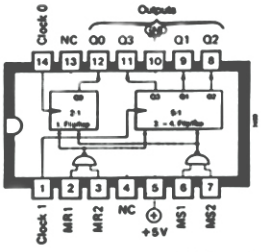

Description:
This package contains a divide-by-two and a divide-by-five counter.

Mode of operation:
The device consists of 4 flip-flops which are connected internally to create one divide-by-2 and one divide-by-5 counters.
All flip-flops have a common reset line controlled by two inputs MR1 and MR2. When both MR1 and MR2 are high the counters are cleared.
Flip-flop 1 is not internally connected to the other stages, thus providing a variety of counter sequences:

a) Counting to 10 (BCD): Output Q0 is connected to the Clock 1 input. The input pulses are applied to the Clock 0 input and the divided signal is extracted at Q3. The device counts in binary code up to 9, with the outputs returning to zero on the 10th clock pulse. Pins 2, 3 and 6, 7 must be grounded.

b) Divide by 2 and divide by 5: Flip-flop 1 is used as a 2:1 divider and flip-flops 2,3 and 4 are used as a 5:1 divider.

c) Symmetrical biquinary divider 10:1: Q3 is connected to Clock 0. Clock 1 is used as the clock input. A symmetrical square-wave with a frequency 1/10 that of the input signal is obtained at output Q0.

The flip-flops are triggered on the falling edge of the clock pulse.
When inputs MS1 and MS2 are both high the counter is preset to 9.

Reset/set inputs				Outputs			
MR1	MR2	MS1	MS2	Q0	Q1	Q2	Q3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Counting			
X	L	X	L	Counting			
L	X	X	L	Counting			
X	L	L	X	Counting			

Application:
Counters and dividers 2:1, 5:1 and 10:1

Data:									
Min. guaranteed clock frequency flip-flop 1	MHz	32					3	32	
Min. guaranteed clock frequency flip-flops 2-4	MHz	16					3	16	
Supply Current	mA	32					3.2	9	
Families:		Std	ALS	AS	F	H	L	LS	S
		●					●	●	

DECADE COUNTER

7490