

# DATA SHEET

## **87C652/87C654**

**80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C**

Product specification

Replaces data sheets 87C652 of 1998 May 01 and 87C654 of 1998 May 01  
IC20 Data Handbook

1999 Jul 23

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### DESCRIPTION

The 87C652/87C654 single-chip 8-Bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 87C652/87C654 has the same instruction set as the 80C51. Three versions of the derivative exist:

80C652—ROMless

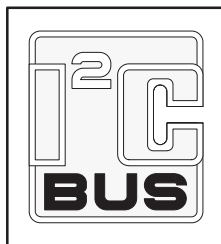
83C652/83C654—8 Kbyte, 16 Kbyte ROM

87C652/87C654—8 Kbyte, 16 Kbyte OTP

The ROMless and ROM are in separate datasheets.

This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 87C654 contains a non-volatile 16k × 8 EPROM and the 87C652 contains an 8k × 8 EPROM. Both have a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I<sup>2</sup>C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 87C652/87C654 can be expanded using standard TTL compatible memories and logic.

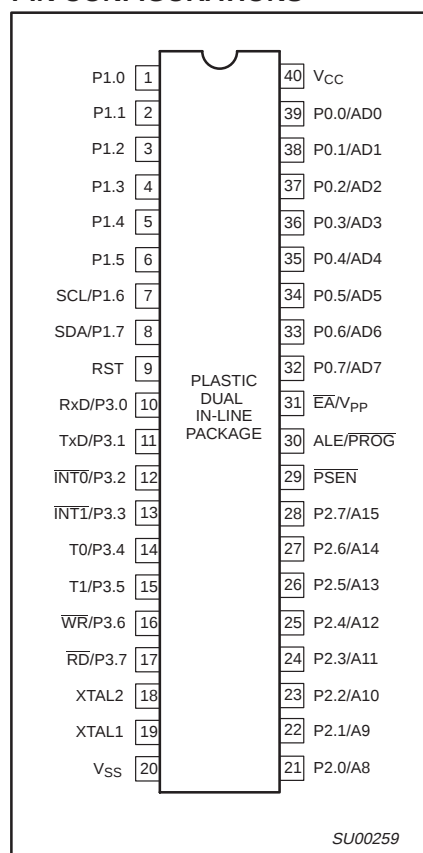
The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16 MHz crystal, 58% of the instructions are executed in 0.75 μs and 40% in 1.5 μs. Multiply and divide instructions require 3 μs.



### FEATURES

- 80C51 central processing unit
- 16k × 8 EPROM or 8k × 8 EPROM expandable externally to 64k bytes
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I<sup>2</sup>C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- Extended temperature range
- OTP package available
- Two speed ranges
  - 16 MHz
  - 20 MHz

### PIN CONFIGURATIONS



### ORDERING INFORMATION

| EPROM        | TEMPERATURE RANGE °C AND PACKAGE         | FREQ MHz | Drawing Number |
|--------------|------------------------------------------|----------|----------------|
| S87C654-4N40 | 0 to +70, Plastic Dual In-line Package   | 16       | SOT129-1       |
| S87C654-4A44 | 0 to +70, Plastic Leaded Chip Carrier    | 16       | SOT187-2       |
| S87C654-4B44 | 0 to +70, Plastic Quad Flat Pack         | 16       | SOT307-2       |
| S87C654-5N40 | –40 to +85, Plastic Dual In-line Package | 16       | SOT129-1       |
| S87C654-5A44 | –40 to +85, Plastic Leaded Chip Carrier  | 16       | SOT187-2       |
| S87C654-5B44 | –40 to +85, Plastic Quad Flat Pack       | 16       | SOT307-2       |
| S87C654-7N40 | 0 to +70, Plastic Dual In-line Package   | 20       | SOT129-1       |
| S87C654-7A44 | 0 to +70, Plastic Leaded Chip Carrier    | 20       | SOT187-2       |
| S87C652-4N40 | 0 to +70, Plastic Dual In-line Package   | 16       | SOT129-1       |
| S87C652-4A44 | 0 to +70, Plastic Leaded Chip Carrier    | 16       | SOT187-2       |
| S87C652-4B44 | 0 to +70, Plastic Quad Flat Pack         | 16       | SOT307-2       |
| S87C652-5A44 | –40 to +85, Plastic Leaded Chip Carrier  | 16       | SOT187-2       |

### NOTES:

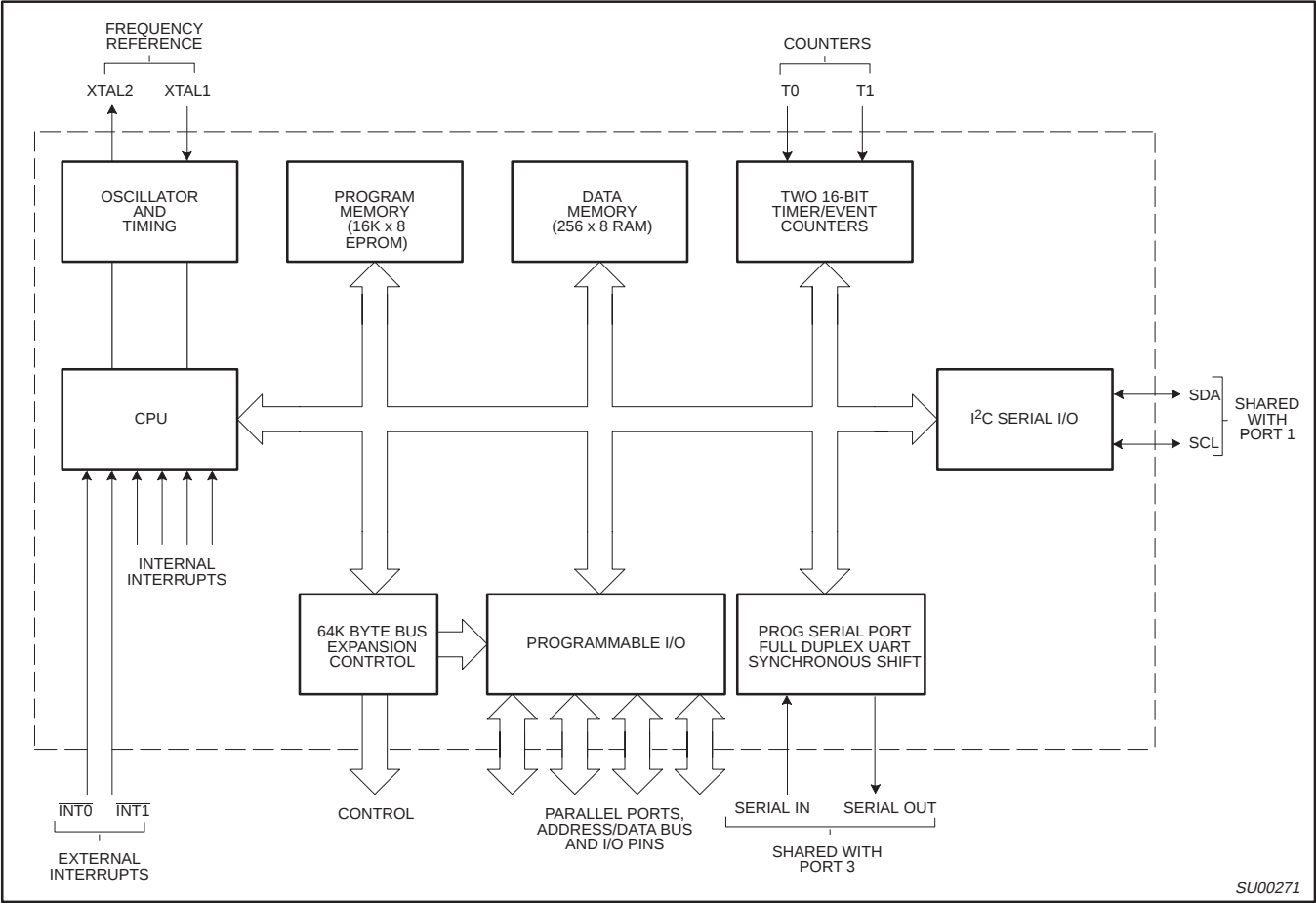
1. For ROM see 83C654 data sheet and 83C652/80C652 data sheet

80C51 8-bit microcontroller

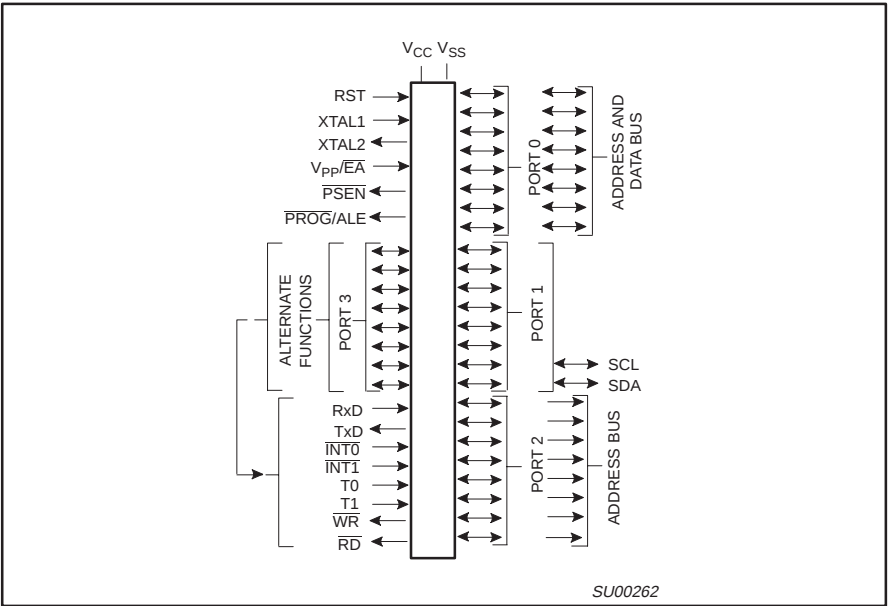
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

BLOCK DIAGRAM



LOGIC SYMBOL



80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

PLASTIC LEADED CHIP  
CARRIER PIN FUNCTIONS

Diagram of the LCC package showing pins 1 through 40. Pin 1 is at the top center, pin 40 is at the top right, pin 39 is at the top left, pin 7 is at the left, pin 17 is at the bottom left, pin 18 is at the bottom, pin 28 is at the bottom right, and pin 29 is at the right.

| Pin | Function                       | Pin | Function                                    |
|-----|--------------------------------|-----|---------------------------------------------|
| 1   | NC*                            | 23  | NC*                                         |
| 2   | P1.0                           | 24  | P2.0/A8                                     |
| 3   | P1.1                           | 25  | P2.1/A9                                     |
| 4   | P1.2                           | 26  | P2.2/A10                                    |
| 5   | P1.3                           | 27  | P2.3/A11                                    |
| 6   | P1.4                           | 28  | P2.4/A12                                    |
| 7   | P1.5                           | 29  | P2.5/A13                                    |
| 8   | P1.6/SCL                       | 30  | P2.6/A14                                    |
| 9   | P1.7/SDA                       | 31  | P2.7/A15                                    |
| 10  | RST                            | 32  | $\overline{\text{PSEN}}$                    |
| 11  | P3.0/RxD                       | 33  | ALE/ $\overline{\text{PROG}}$               |
| 12  | NC*                            | 34  | NC*                                         |
| 13  | P3.1/TxD                       | 35  | $\overline{\text{EA}}/\text{V}_{\text{PP}}$ |
| 14  | P3.2/ $\overline{\text{INT0}}$ | 36  | P0.7/AD7                                    |
| 15  | P3.3/ $\overline{\text{INT1}}$ | 37  | P0.6/AD6                                    |
| 16  | P3.4/T0                        | 38  | P0.5/AD5                                    |
| 17  | P3.5/T1                        | 39  | P0.4/AD4                                    |
| 18  | P3.6/ $\overline{\text{WR}}$   | 40  | P0.3/AD3                                    |
| 19  | P3.7/ $\overline{\text{RD}}$   | 41  | P0.2/AD2                                    |
| 20  | XTAL2                          | 42  | P0.1/AD1                                    |
| 21  | XTAL1                          | 43  | P0.0/AD0                                    |
| 22  | V <sub>SS</sub>                | 44  | V <sub>CC</sub>                             |

\* NO INTERNAL CONNECTION

SU00260

PLASTIC QUAD FLAT PACK  
PIN FUNCTIONS

Diagram of the PQFP package showing pins 1 through 44. Pin 1 is at the top left, pin 33 is at the top right, pin 34 is at the right, pin 23 is at the bottom right, pin 22 is at the bottom, pin 12 is at the bottom left, pin 11 is at the left, and pin 44 is at the top.

| Pin | Function                       | Pin | Function                                    |
|-----|--------------------------------|-----|---------------------------------------------|
| 1   | P1.5                           | 23  | P2.5/A13                                    |
| 2   | P1.6/SCL                       | 24  | P2.6/A14                                    |
| 3   | P1.7/SDA                       | 25  | P2.7/A15                                    |
| 4   | RST                            | 26  | $\overline{\text{PSEN}}$                    |
| 5   | P3.0/RxD                       | 27  | ALE/ $\overline{\text{PROG}}$               |
| 6   | NC*                            | 28  | NC*                                         |
| 7   | P3.1/TxD                       | 29  | $\overline{\text{EA}}/\text{V}_{\text{PP}}$ |
| 8   | P3.2/ $\overline{\text{INT0}}$ | 30  | P0.7/AD7                                    |
| 9   | P3.3/ $\overline{\text{INT1}}$ | 31  | P0.6/AD6                                    |
| 10  | P3.4/T0                        | 32  | P0.5/AD5                                    |
| 11  | P3.5/T1                        | 33  | P0.4/AD4                                    |
| 12  | P3.6/ $\overline{\text{WR}}$   | 34  | P0.3/AD3                                    |
| 13  | P3.7/ $\overline{\text{RD}}$   | 35  | P0.2/AD2                                    |
| 14  | XTAL2                          | 36  | P0.1/AD1                                    |
| 15  | XTAL1                          | 37  | P0.0/AD0                                    |
| 16  | V <sub>SS</sub>                | 38  | V <sub>CC</sub>                             |
| 17  | NC*                            | 39  | NC*                                         |
| 18  | P2.0/A8                        | 40  | P1.0                                        |
| 19  | P2.1/A9                        | 41  | P1.1                                        |
| 20  | P2.2/A10                       | 42  | P1.2                                        |
| 21  | P2.3/A11                       | 43  | P1.3                                        |
| 22  | P2.4/A12                       | 44  | P1.4                                        |

\* NO INTERNAL CONNECTION

SU00261

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### PIN DESCRIPTIONS

| MNEMONIC           | PIN NUMBER |              |               | TYPE | NAME AND FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--------------------|------------|--------------|---------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                    | DIP        | LCC          | QFP           |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| V <sub>SS</sub>    | 20         | 22           | 16            | I    | <b>Ground:</b> 0 V reference.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| V <sub>CC</sub>    | 40         | 44           | 38            | I    | <b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| P0.0–P0.7          | 39–32      | 43–36        | 37–30         | I/O  | <b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C654. External pull-ups are required during program verification.                                                                                                                                                                                                                                                                      |
| P1.0–P1.7          | 1–8        | 2–9          | 40–44,<br>1–3 | I/O  | <b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:                                                                                                                                                                                                                                       |
| P1.6               | 7          | 8            | 2             | I/O  | <b>SCL:</b> I <sup>2</sup> C-bus serial port clock line.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| P1.7               | 8          | 9            | 3             | I/O  | <b>SDA:</b> I <sup>2</sup> C-bus serial port data line.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| P2.0–P2.7          | 21–28      | 24–31        | 18–25         | I/O  | <b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register. |
| P3.0–P3.7          | 10–17      | 11,<br>13–19 | 5,<br>7–13    | I/O  | <b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also serves the special features of the 80C51 family, as listed below:                                                                                                                                                                                                                                                                                                                        |
|                    | 10         | 11           | 5             | I    | <b>RxD (P3.0):</b> Serial input port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|                    | 11         | 13           | 7             | O    | <b>TxD (P3.1):</b> Serial output port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|                    | 12         | 14           | 8             | I    | <b>INT0 (P3.2):</b> External interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                    | 13         | 15           | 9             | I    | <b>INT1 (P3.3):</b> External interrupt                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|                    | 14         | 16           | 10            | I    | <b>T0 (P3.4):</b> Timer 0 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                    | 15         | 17           | 11            | I    | <b>T1 (P3.5):</b> Timer 1 external input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                    | 16         | 18           | 12            | O    | <b>WR (P3.6):</b> External data memory write strobe                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                    | 17         | 19           | 13            | O    | <b>RD (P3.7):</b> External data memory read strobe                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| RST                | 9          | 10           | 4             | I    | <b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| ALE/PROG           | 30         | 33           | 27            | I/O  | <b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.                                                                                                                                                                                                                                                                                                                            |
| PSEN               | 29         | 32           | 26            | O    | <b>Program Store Enable:</b> The read strobe to external program memory. When the 87C654 is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.                                                                                                                                                                                                                                                                                                                                                                                                               |
| EA/V <sub>PP</sub> | 31         | 35           | 29            | I    | <b>External Access Enable/Programming Supply Voltage:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 1FFFH for 87C652 and 3FFFH for 87C654. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH. This pin also receives the 12.75 V programming supply voltage (V <sub>PP</sub> ) during EPROM programming.                                                                                                                                                                                                                                                                                             |
| XTAL1              | 19         | 21           | 15            | I    | <b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| XTAL2              | 18         | 20           | 14            | O    | <b>Crystal 2:</b> Output from the inverting oscillator amplifier.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### NOTE:

To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V<sub>CC</sub> + 0.5 V or V<sub>SS</sub> – 0.5 V, respectively.

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

**Table 1. 8XC652/654 Special Function Registers**

| SYMBOL  | DESCRIPTION            | DIRECT ADDRESS | BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION |      |     |     |      |      |     |     | RESET VALUE |     |
|---------|------------------------|----------------|---------------------------------------------------|------|-----|-----|------|------|-----|-----|-------------|-----|
|         |                        |                | MSB                                               |      |     |     | LSB  |      |     |     |             |     |
| ACC*    | Accumulator            | E0H            | E7                                                | E6   | E5  | E4  | E3   | E2   | E1  | E0  | 00H         |     |
| B*      | B register             | F0H            | F7                                                | F6   | F5  | F4  | F3   | F2   | F1  | F0  | 00H         |     |
| DPTR:   | Data pointer (2 bytes) |                |                                                   |      |     |     |      |      |     |     |             |     |
| DPH     | Data pointer high      | 83H            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| DPL     | Data pointer low       | 82H            |                                                   |      |     |     |      |      |     |     | 00H         |     |
|         |                        |                | AF                                                | AE   | AD  | AC  | AB   | AA   | A9  | A8  |             |     |
| IE*#    | Interrupt enable       | A8H            | EA                                                |      | ES1 | ES0 | ET1  | EX1  | ET0 | EX0 | 0x000000B   |     |
|         |                        |                | BF                                                | BE   | BD  | BC  | BB   | BA   | B9  | B8  |             |     |
| IP*#    | Interrupt priority     | B8H            | –                                                 |      | PS1 | PS0 | PT1  | PX1  | PT0 | PX0 | xx000000B   |     |
|         |                        |                | 87                                                | 86   | 85  | 84  | 83   | 82   | 81  | 80  |             |     |
| P0*     | Port 0                 | 80H            | AD7                                               | AD6  | AD5 | AD4 | AD3  | AD2  | AD1 | AD0 | FFH         |     |
|         |                        |                | 97                                                | 96   | 95  | 94  | 93   | 92   | 91  | 90  |             |     |
| P1*#    | Port 1                 | 90H            | SDA                                               | SCL  |     |     |      |      |     |     | FFH         |     |
|         |                        |                | A7                                                | A6   | A5  | A4  | A3   | A2   | A1  | A0  |             |     |
| P2*     | Port 2                 | A0H            | A15                                               | A14  | A13 | A12 | A11  | A10  | A9  | A8  | FFH         |     |
|         |                        |                | B7                                                | B6   | B5  | B4  | B3   | B2   | B1  | B0  |             |     |
| P3*     | Port 3                 | B0H            | RD                                                | WR   | T1  | T0  | INT1 | INT0 | TXD | RXD | FFH         |     |
| PCON#   | Power control          | 87H            | SMOD                                              | –    | –   | –   | GF1  | GF0  | PD  | IDL | 0xxx0000B   |     |
|         |                        |                | 9F                                                | 9E   | 9D  | 9C  | 9B   | 9A   | 99  | 98  |             |     |
| S0CON*# | Serial 0 port control  | 98H            | SM0                                               | SM1  | SM2 | REN | TB8  | RB8  | TI  | RI  | 00H         |     |
| S0BUF#  | Serial 0 data buffer   | 99H            |                                                   |      |     |     |      |      |     |     | xxxxxxxxB   |     |
|         |                        |                | D7                                                | D6   | D5  | D4  | D3   | D2   | D1  | D0  |             |     |
| PSW*    | Program status word    | D0H            | CY                                                | AC   | F0  | RS1 | RS0  | OV   | F1  | P   | 00H         |     |
| S1DAT#  | Serial 1 data          | DAH            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| SP      | Stack pointer          | 81H            |                                                   |      |     |     |      |      |     |     | 07H         |     |
| S1ADR#  | Serial 1 address       | DBH            | SLAVE ADDRESS                                     |      |     |     |      |      |     |     | GC          | 00H |
|         |                        |                |                                                   |      |     |     |      |      |     |     |             |     |
| S1STA#  | Serial 1 status        | D9H            | SC4                                               | SC3  | SC2 | SC1 | SC0  | 0    | 0   | 0   | F8H         |     |
|         |                        |                | DF                                                | DE   | DD  | DC  | DB   | DA   | D9  | D8  |             |     |
| S1CON*# | Serial 1 control       | D8H            | CR2                                               | ENS1 | STA | STO | SI   | AA   | CR1 | CR0 | 00000000B   |     |
|         |                        |                | 8F                                                | 8E   | 8D  | 8C  | 8B   | 8A   | 89  | 88  |             |     |
| TCON*   | Timer control          | 88H            | TF1                                               | TR1  | TF0 | TR0 | IE1  | IT1  | IE0 | IT0 | 00H         |     |
| TH1     | Timer high 1           | 8DH            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| TH0     | Timer high 0           | 8CH            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| TL1     | Timer low 1            | 8BH            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| TL0     | Timer low 0            | 8AH            |                                                   |      |     |     |      |      |     |     | 00H         |     |
| TMOD    | Timer mode             | 89H            | GATE                                              | C/T  | M1  | M0  | GATE | C/T  | M1  | M0  | 00H         |     |

\* SFRs are bit addressable.

# SFRs are modified from or added to the 80C51 SFRs.

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the Logic Symbol.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

### Reset

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few

milliseconds) plus two machine cycles. At power-on, the voltage on V<sub>CC</sub> and RST must come up at the same time for a proper start-up.

### Idle Mode

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

### Power-Down Mode

In the power-down mode, the oscillator is stopped and the instruction to invoke

power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 2 shows the state of the I/O ports during low current operating modes.

### I<sup>2</sup>C SERIAL COMMUNICATION—SIO1

The I<sup>2</sup>C serial port is identical to the I<sup>2</sup>C serial port on the 8XC552. The operation of this subsystem is described in detail in the 8XC552 section of this manual.

Note that in both the 8XC652/4 and the 8XC552 the I<sup>2</sup>C pins are alternate functions to port pins P1.6 and P1.7. Because of this, P1.6 and P1.7 on these parts do not have a pull-up structure as found on the 80C51. Therefore P1.6 and P1.7 have open drain outputs on the 8XC652/4.

**Table 2. External Pin Status During Idle and Power-Down Mode**

| MODE       | PROGRAM MEMORY | ALE | PSEN | PORT 0 | PORT 1 | PORT 2  | PORT 3 |
|------------|----------------|-----|------|--------|--------|---------|--------|
| Idle       | Internal       | 1   | 1    | Data   | Data   | Data    | Data   |
| Idle       | External       | 1   | 1    | Float  | Data   | Address | Data   |
| Power-down | Internal       | 0   | 0    | Data   | Data   | Data    | Data   |
| Power-down | External       | 0   | 0    | Float  | Data   | Data    | Data   |

### Serial Control Register (S1CON) – See Table 3

#### S1CON (D8H)

|     |      |     |     |    |    |     |     |
|-----|------|-----|-----|----|----|-----|-----|
| CR2 | ENS1 | STA | STO | SI | AA | CR1 | CR0 |
|-----|------|-----|-----|----|----|-----|-----|

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

**Table 3. Serial Clock Rates**

| CR2 | CR1 | CR0 | BIT FREQUENCY (kHz) AT f <sub>OSC</sub> |                        |                         |                         | f <sub>OSC</sub> DIVIDED BY                                                    |
|-----|-----|-----|-----------------------------------------|------------------------|-------------------------|-------------------------|--------------------------------------------------------------------------------|
|     |     |     | 6 MHz                                   | 12 MHz                 | 16 MHz                  | 20 MHz                  |                                                                                |
| 0   | 0   | 0   | 23                                      | 47                     | 62.5                    | 78                      | 256                                                                            |
| 0   | 0   | 1   | 27                                      | 54                     | 71                      | 89 <sup>1</sup>         | 224                                                                            |
| 0   | 1   | 0   | 31.25                                   | 62.5                   | 83.3                    | 104 <sup>1</sup>        | 192                                                                            |
| 0   | 1   | 1   | 37                                      | 75                     | 100                     | 125 <sup>1</sup>        | 160                                                                            |
| 1   | 0   | 0   | 6.25                                    | 12.5                   | 17                      | 21                      | 960                                                                            |
| 1   | 0   | 1   | 50                                      | 100                    | 133 <sup>1</sup>        | 166 <sup>1</sup>        | 120                                                                            |
| 1   | 1   | 0   | 100                                     | 200 <sup>1</sup>       | 267 <sup>1</sup>        | 334 <sup>1</sup>        | 60                                                                             |
| 1   | 1   | 1   | 0.25 < 62.5<br>0 to 255                 | 0.5 < 62.5<br>0 to 254 | 0.65 < 55.6<br>0 to 253 | 0.81 < 69.4<br>0 to 253 | 96 × (256 – (reload value Timer 1))<br>(Reload value range: 0 – 254 in mode 2) |

#### NOTE:

1. These frequencies exceed the upper limit of 100kHz of the I<sup>2</sup>C-bus specification and cannot be used in an I<sup>2</sup>C-bus application.

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

| PARAMETER                                                                                    | RATING        | UNIT |
|----------------------------------------------------------------------------------------------|---------------|------|
| Storage temperature range                                                                    | −65 to +150   | °C   |
| Voltage on $\overline{EA}/V_{PP}$ to $V_{SS}$                                                | −0.5 to + 13  | V    |
| Voltage on any other pin to $V_{SS}$                                                         | −0.5 to + 6.5 | V    |
| Input, output current on any single pin                                                      | ±5            | mA   |
| Power dissipation (based on package heat transfer limitations, not device power consumption) | 1             | W    |

#### NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.

### DEVICE SPECIFICATIONS

| TYPE                    | SUPPLY VOLTAGE (V) |      | FREQUENCY (MHz) |      | TEMPERATURE RANGE (°C) |
|-------------------------|--------------------|------|-----------------|------|------------------------|
|                         | MIN.               | MAX. | MIN.            | MAX. |                        |
| S87C652-4 and S87C654-4 | 4.5                | 5.5  | 3.5             | 16   | 0 to +70               |
| S87C652-5 and S87C654-5 | 4.5                | 5.5  | 3.5             | 16   | −40 to +85             |
| S87C654-7               | 4.5                | 5.5  | 3.5             | 20   | 0 to +70               |

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### DC ELECTRICAL CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ 

| SYMBOL    | PARAMETER                                                                                                                                                                 | PART TYPE                  | TEST CONDITIONS                                                       | LIMITS                             |                                     | UNIT                                                         |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------|------------------------------------|-------------------------------------|--------------------------------------------------------------|
|           |                                                                                                                                                                           |                            |                                                                       | MIN.                               | MAX.                                |                                                              |
| $V_{IL}$  | Input low voltage, except $\overline{EA}$ , P1.6/SCL, P1.7/SDA                                                                                                            | 0 to +70°C<br>-40 to +85°C |                                                                       | -0.5<br>-0.5                       | $0.2V_{CC}-0.1$<br>$0.2V_{CC}-0.15$ | V<br>V                                                       |
| $V_{IL1}$ | Input low voltage to $\overline{EA}$                                                                                                                                      | 0 to +70°C<br>-40 to +85°C |                                                                       | -0.5<br>-0.5                       | $0.2V_{CC}-0.3$<br>$0.2V_{CC}-0.35$ | V<br>V                                                       |
| $V_{IL2}$ | Input low voltage to P1.6/SCL, P1.7/SDA <sup>1</sup>                                                                                                                      |                            |                                                                       | -0.5                               | $0.3V_{CC}$                         | V                                                            |
| $V_{IH}$  | Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA                                                                                                                 | 0 to +70°C<br>-40 to +85°C |                                                                       | $0.2V_{CC}+0.9$<br>$0.2V_{CC}+1.0$ | $V_{CC}+0.5$<br>$V_{CC}+0.5$        | V<br>V                                                       |
| $V_{IH1}$ | Input high voltage, XTAL1, RST                                                                                                                                            | 0 to +70°C<br>-40 to +85°C |                                                                       | $0.7V_{CC}$<br>$0.7V_{CC}+0.1$     | $V_{CC}+0.5$<br>$V_{CC}+0.5$        | V<br>V                                                       |
| $V_{IH2}$ | Input high voltage, P1.6/SCL, P1.7/SDA <sup>1</sup>                                                                                                                       |                            |                                                                       | $0.7V_{CC}$                        | 6.0                                 | V                                                            |
| $V_{OL}$  | Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA                                                                                                              |                            | $I_{OL} = 1.6\text{mA}^{2, 3}$                                        |                                    | 0.45                                | V                                                            |
| $V_{OL1}$ | Output low voltage, port 0, ALE, PSEN                                                                                                                                     |                            | $I_{OL} = 3.2\text{mA}^{2, 3}$                                        |                                    | 0.45                                | V                                                            |
| $V_{OL2}$ | Output low voltage, P1.6/SCL, P1.7/SDA                                                                                                                                    |                            | $I_{OL} = 3.0\text{mA}$                                               |                                    | 0.4                                 | V                                                            |
| $V_{OH}$  | Output high voltage, ports 1, 2, 3                                                                                                                                        | 0 to +70°C<br>-40 to +85°C | $I_{OH} = -60\mu\text{A}$<br>$I_{OH} = -25\mu\text{A}$                | 2.4<br>$0.75V_{CC}$                |                                     | V<br>V                                                       |
| $V_{OH1}$ | Output high voltage; port 0 in external bus mode, ALE, PSEN, RST <sup>4</sup>                                                                                             | 0 to +70°C<br>-40 to +85°C | $I_{OH} = -400\mu\text{A}$<br>$I_{OH} = -150\mu\text{A}$              | 2.4<br>$0.75V_{CC}$                |                                     | V<br>V                                                       |
| $I_{IL}$  | Logical 0 input current, ports 1, 2, 3, 4, except P1.6/SCL, P1.7/SDA                                                                                                      | 0 to +70°C<br>-40 to +85°C | $V_{IN} = 0.45\text{V}$                                               |                                    | -50<br>-75                          | $\mu\text{A}$<br>$\mu\text{A}$                               |
| $I_{TL}$  | Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA                                                                                               | 0 to +70°C<br>-40 to +85°C | See note 5                                                            |                                    | -650<br>-750                        | $\mu\text{A}$<br>$\mu\text{A}$                               |
| $I_{L1}$  | Input leakage current, port 0                                                                                                                                             |                            | $0.45\text{V} < V_I < V_{CC}$                                         |                                    | $\pm 10$                            | $\mu\text{A}$                                                |
| $I_{L2}$  | Input leakage current, P1.6/SCL, P1.7/SDA                                                                                                                                 |                            | $0\text{V} < V_I < 6.0\text{V}$<br>$0\text{V} < V_{CC} < 6.0\text{V}$ |                                    | $\pm 10$                            | $\mu\text{A}$<br>$\mu\text{A}$                               |
| $I_{CC}$  | Power supply current:<br><br>Active mode @ 16 MHz <sup>7</sup><br>Idle mode @ 16 MHz <sup>8</sup><br>Power down mode <sup>9, 10</sup><br>Power down mode <sup>9, 10</sup> | 0 to +70°C<br>-40 to +85°C | See note 6<br>$V_{CC}=6.0\text{V}$                                    |                                    | 25<br>6<br>50<br>135                | $\text{mA}$<br>$\text{mA}$<br>$\mu\text{A}$<br>$\mu\text{A}$ |
| $R_{RST}$ | Internal reset pull-down resistor                                                                                                                                         |                            |                                                                       | 50                                 | 150                                 | k $\Omega$                                                   |
| $C_{IO}$  | Pin capacitance                                                                                                                                                           |                            | Freq.=1 MHz                                                           |                                    | 10                                  | pF                                                           |

#### NOTES:

- The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I<sup>2</sup>C specification, so an input voltage below  $0.3V_{CC}$  will be recognized as a logic 0 while an input voltage above  $0.7V_{CC}$  will be recognized as a logic 1.
- Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the  $V_{OL}$ s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE pin may exceed 0.8 V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.  $I_{OL}$  can exceed these conditions provided that no single output sinks more than 5 mA and no more than two outputs exceed the test conditions.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows: Maximum  $I_{OL} = 10\text{ mA}$  per port pin; Maximum  $I_{OL} = 26\text{ mA}$  total for Port 0; Maximum  $I_{OL} = 15\text{ mA}$  total for Ports 1, 2, and 3; Maximum  $I_{OL} = 71\text{ mA}$  total for all output pins. If  $I_{OL}$  exceeds the test conditions,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- Capacitive loading on ports 0 and 2 may cause the  $V_{OH}$  on ALE and PSEN to momentarily fall below the  $0.9V_{CC}$  specification when the address bits are stabilizing.
- Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when  $V_{IN}$  is approximately 2 V.
- See Figures 9 through 11 for  $I_{CC}$  test conditions.
- The operating supply current is measured with all output pins disconnected; XTAL1 driven with  $t_r = t_f = 10\text{ ns}$ ;  $V_{IL} = V_{SS} + 0.5\text{ V}$ ;  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 not connected;  $\overline{EA} = \text{RST} = \text{Port 0} = \text{P1.6} = \text{P1.7} = V_{CC}$ ;  $f_{CLK} = 16\text{ MHz}$ . See Figure 9.
- The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with  $t_r = t_f = 10\text{ ns}$ ;  $V_{IL} = V_{SS} + 0.5\text{ V}$ ;  $V_{IH} = V_{CC} - 0.5\text{ V}$ ; XTAL2 not connected; Port 0 = P1.6 = P1.7 =  $V_{CC}$ ;  $\overline{EA} = \text{RST} = V_{SS}$ ;  $f_{CLK} = 16\text{ MHz}$ . See Figure 10.
- The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = P1.6 = P1.7 =  $V_{CC}$ ;  $\overline{EA} = \text{RST} = V_{SS}$ . See Figure 11.
- $0.2\text{V} \leq V_{PD} \leq V_{CCmax}$ .

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### AC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

| SYMBOL                | FIGURE | PARAMETER                                                                 | 16 MHz CLOCK |     | VARIABLE CLOCK           |                                       | UNIT |
|-----------------------|--------|---------------------------------------------------------------------------|--------------|-----|--------------------------|---------------------------------------|------|
|                       |        |                                                                           | MIN          | MAX | MIN                      | MAX                                   |      |
| 1/t <sub>CLCL</sub>   | 2      | Oscillator frequency <b>Speed Versions</b><br>87C654<br>-4, -5            |              |     | 3.5                      | 16                                    | MHz  |
| t <sub>LHLL</sub>     | 2      | ALE pulse width                                                           | 85           |     | 2t <sub>CLCL</sub> -40   |                                       | ns   |
| t <sub>AVLL</sub>     | 2      | Address valid to ALE low                                                  | 8            |     | t <sub>CLCL</sub> -55    |                                       | ns   |
| t <sub>LLAX</sub>     | 2      | Address hold after ALE low                                                | 28           |     | t <sub>CLCL</sub> -35    |                                       | ns   |
| t <sub>LLIV</sub>     | 2      | ALE low to valid instruction in                                           |              | 150 |                          | 4t <sub>CLCL</sub> -100               | ns   |
| t <sub>LLPL</sub>     | 2      | ALE low to $\overline{\text{PSEN}}$ low                                   | 23           |     | t <sub>CLCL</sub> -40    |                                       | ns   |
| t <sub>PLPH</sub>     | 2      | $\overline{\text{PSEN}}$ pulse width                                      | 143          |     | 3t <sub>CLCL</sub> -45   |                                       | ns   |
| t <sub>PLIV</sub>     | 2      | $\overline{\text{PSEN}}$ low to valid instruction in                      |              | 83  |                          | 3t <sub>CLCL</sub> -105               | ns   |
| t <sub>PXIX</sub>     | 2      | Input instruction hold after $\overline{\text{PSEN}}$                     | 0            |     | 0                        |                                       | ns   |
| t <sub>PXIZ</sub>     | 2      | Input instruction float after $\overline{\text{PSEN}}$                    |              | 38  |                          | t <sub>CLCL</sub> -25                 | ns   |
| t <sub>AVIV</sub>     | 2      | Address to valid instruction in                                           |              | 208 |                          | 5t <sub>CLCL</sub> -105               | ns   |
| t <sub>PLAZ</sub>     | 2      | $\overline{\text{PSEN}}$ low to address float                             |              | 10  |                          | 10                                    | ns   |
| <b>Data Memory</b>    |        |                                                                           |              |     |                          |                                       |      |
| t <sub>AVLL</sub>     | 3, 4   | Address valid to ALE low                                                  | 28           |     | t <sub>CLCL</sub> -35    |                                       | ns   |
| t <sub>RLRH</sub>     | 3, 4   | $\overline{\text{RD}}$ pulse width                                        | 275          |     | 6t <sub>CLCL</sub> -100  |                                       | ns   |
| t <sub>WLWH</sub>     | 3, 4   | $\overline{\text{WR}}$ pulse width                                        | 275          |     | 6t <sub>CLCL</sub> -100  |                                       | ns   |
| t <sub>RLDV</sub>     | 3, 4   | $\overline{\text{RD}}$ low to valid data in                               |              | 148 |                          | 5t <sub>CLCL</sub> -165               | ns   |
| t <sub>RHDX</sub>     | 3, 4   | Data hold after $\overline{\text{RD}}$                                    | 0            |     | 0                        |                                       | ns   |
| t <sub>RHDZ</sub>     | 3, 4   | Data float after $\overline{\text{RD}}$                                   |              | 55  |                          | 2t <sub>CLCL</sub> -70                | ns   |
| t <sub>LLDV</sub>     | 3, 4   | ALE low to valid data in                                                  |              | 350 |                          | 8t <sub>CLCL</sub> -150               | ns   |
| t <sub>AVDV</sub>     | 3, 4   | Address to valid data in                                                  |              | 398 |                          | 9t <sub>CLCL</sub> -165               | ns   |
| t <sub>LLWL</sub>     | 3, 4   | ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low           | 138          | 238 | 3t <sub>CLCL</sub> -50   | 3t <sub>CLCL</sub> +50                | ns   |
| t <sub>AVWL</sub>     | 3, 4   | Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low | 120          |     | 4t <sub>CLCL</sub> -130  |                                       | ns   |
| t <sub>QVWX</sub>     | 3, 4   | Data valid to $\overline{\text{WR}}$ transition                           | 3            |     | t <sub>CLCL</sub> -60    |                                       | ns   |
| t <sub>DW</sub>       | 3, 4   | Data setup time before $\overline{\text{WR}}$                             | 288          |     | 7t <sub>CLCL</sub> -150  |                                       | ns   |
| t <sub>WHQX</sub>     | 3, 4   | Data hold after $\overline{\text{WR}}$                                    | 13           |     | t <sub>CLCL</sub> -50    |                                       | ns   |
| t <sub>RLAZ</sub>     | 3, 4   | $\overline{\text{RD}}$ low to address float                               |              | 0   |                          | 0                                     | ns   |
| t <sub>WHLH</sub>     | 3, 4   | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high         | 23           | 103 | t <sub>CLCL</sub> -40    | t <sub>CLCL</sub> +40                 | ns   |
| <b>Shift Register</b> |        |                                                                           |              |     |                          |                                       |      |
| t <sub>XLXL</sub>     | 5      | Serial port clock cycle time <sup>3</sup>                                 | 0.75         |     | 12t <sub>CLCL</sub>      |                                       | μs   |
| t <sub>QVXH</sub>     | 5      | Output data setup to clock rising edge <sup>3</sup>                       | 492          |     | 10t <sub>CLCL</sub> -133 |                                       | ns   |
| t <sub>XHQX</sub>     | 5      | Output data hold after clock rising edge <sup>3</sup>                     | 80           |     | 2t <sub>CLCL</sub> -117  |                                       | ns   |
| t <sub>XHDX</sub>     | 5      | Input data hold after clock rising edge <sup>3</sup>                      | 0            |     | 0                        |                                       | ns   |
| t <sub>XHDV</sub>     | 5      | Clock rising edge to input data valid <sup>3</sup>                        |              | 492 |                          | 10t <sub>CLCL</sub> -133              | ns   |
| <b>External Clock</b> |        |                                                                           |              |     |                          |                                       |      |
| t <sub>CHCX</sub>     | 6      | High time <sup>3</sup>                                                    | 20           |     | 20                       | t <sub>CLCL</sub> - t <sub>LOW</sub>  | ns   |
| t <sub>CLCX</sub>     | 6      | Low time <sup>3</sup>                                                     | 20           |     | 20                       | t <sub>CLCL</sub> - t <sub>HIGH</sub> | ns   |
| t <sub>CLCH</sub>     | 6      | Rise time <sup>3</sup>                                                    |              | 20  |                          | 20                                    | ns   |
| t <sub>CHCL</sub>     | 6      | Fall time <sup>3</sup>                                                    |              | 20  |                          | 20                                    | ns   |

#### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and  $\overline{\text{PSEN}}$  = 100 pF, load capacitance for all other outputs = 80 pF.
- These values are characterized but not 100% production tested.

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### AC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

| SYMBOL                | FIGURE | PARAMETER                                                                 | 20 MHz CLOCK |     | VARIABLE CLOCK           |                                       | UNIT |
|-----------------------|--------|---------------------------------------------------------------------------|--------------|-----|--------------------------|---------------------------------------|------|
|                       |        |                                                                           | MIN          | MAX | MIN                      | MAX                                   |      |
| 1/t <sub>CLCL</sub>   | 2      | Oscillator frequency: <b>Speed Versions 87C654</b><br>-7, -8              |              |     | 3.5                      | 20                                    | MHz  |
| t <sub>LHLL</sub>     | 2      | ALE pulse width                                                           | 60           |     | 2t <sub>CLCL</sub> -40   |                                       | ns   |
| t <sub>AVLL</sub>     | 2      | Address valid to ALE low                                                  | 25           |     | t <sub>CLCL</sub> -25    |                                       | ns   |
| t <sub>LLAX</sub>     | 2      | Address hold after ALE low                                                | 25           |     | t <sub>CLCL</sub> -25    |                                       | ns   |
| t <sub>LLIV</sub>     | 2      | ALE low to valid instruction in                                           |              | 135 |                          | 4t <sub>CLCL</sub> -65                | ns   |
| t <sub>LLPL</sub>     | 2      | ALE low to $\overline{\text{PSEN}}$ low                                   | 25           |     | t <sub>CLCL</sub> -25    |                                       | ns   |
| t <sub>PLPH</sub>     | 2      | $\overline{\text{PSEN}}$ pulse width                                      | 105          |     | 3t <sub>CLCL</sub> -45   |                                       | ns   |
| t <sub>PLIV</sub>     | 2      | $\overline{\text{PSEN}}$ low to valid instruction in                      |              | 90  |                          | 3t <sub>CLCL</sub> -60                | ns   |
| t <sub>PIX</sub>      | 2      | Input instruction hold after $\overline{\text{PSEN}}$                     | 0            |     | 0                        |                                       | ns   |
| t <sub>PIXZ</sub>     | 2      | Input instruction float after $\overline{\text{PSEN}}$                    |              | 25  |                          | t <sub>CLCL</sub> -25                 | ns   |
| t <sub>AVIV</sub>     | 2      | Address to valid instruction in                                           |              | 170 |                          | 5t <sub>CLCL</sub> -80                | ns   |
| t <sub>PLAZ</sub>     | 2      | $\overline{\text{PSEN}}$ low to address float                             |              | 10  |                          | 10                                    | ns   |
| <b>Data Memory</b>    |        |                                                                           |              |     |                          |                                       |      |
| t <sub>AVLL</sub>     | 3, 4   | Address valid to ALE low                                                  | 25           |     | t <sub>CLCL</sub> -25    |                                       | ns   |
| t <sub>RLRH</sub>     | 3, 4   | $\overline{\text{RD}}$ pulse width                                        | 200          |     | 6t <sub>CLCL</sub> -100  |                                       | ns   |
| t <sub>WLWH</sub>     | 3, 4   | $\overline{\text{WR}}$ pulse width                                        | 200          |     | 6t <sub>CLCL</sub> -100  |                                       | ns   |
| t <sub>RLDV</sub>     | 3, 4   | $\overline{\text{RD}}$ low to valid data in                               |              | 160 |                          | 5t <sub>CLCL</sub> -90                | ns   |
| t <sub>RHDX</sub>     | 3, 4   | Data hold after $\overline{\text{RD}}$                                    | 0            |     | 0                        |                                       | ns   |
| t <sub>RHDZ</sub>     | 3, 4   | Data float after $\overline{\text{RD}}$                                   |              | 72  |                          | 2t <sub>CLCL</sub> -28                | ns   |
| t <sub>LLDV</sub>     | 3, 4   | ALE low to valid data in                                                  |              | 250 |                          | 8t <sub>CLCL</sub> -150               | ns   |
| t <sub>AVDV</sub>     | 3, 4   | Address to valid data in                                                  |              | 285 |                          | 9t <sub>CLCL</sub> -165               | ns   |
| t <sub>LLWL</sub>     | 3, 4   | ALE low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low           | 100          | 200 | 3t <sub>CLCL</sub> -50   | 3t <sub>CLCL</sub> +50                | ns   |
| t <sub>AVWL</sub>     | 3, 4   | Address valid to $\overline{\text{WR}}$ low or $\overline{\text{RD}}$ low | 125          |     | 4t <sub>CLCL</sub> -75   |                                       | ns   |
| t <sub>QVWX</sub>     | 3, 4   | Data valid to $\overline{\text{WR}}$ transition                           | 20           |     | t <sub>CLCL</sub> -30    |                                       | ns   |
| t <sub>DW</sub>       | 3, 4   | Data setup time before $\overline{\text{WR}}$                             | 220          |     | 7t <sub>CLCL</sub> -130  |                                       | ns   |
| t <sub>WHQX</sub>     | 3, 4   | Data hold after $\overline{\text{WR}}$                                    | 25           |     | t <sub>CLCL</sub> -25    |                                       | ns   |
| t <sub>RLAZ</sub>     | 3, 4   | $\overline{\text{RD}}$ low to address float                               |              | 0   |                          | 0                                     | ns   |
| t <sub>WHLH</sub>     | 3, 4   | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to ALE high         | 25           | 75  | t <sub>CLCL</sub> -25    | t <sub>CLCL</sub> +25                 | ns   |
| <b>Shift Register</b> |        |                                                                           |              |     |                          |                                       |      |
| t <sub>XLXL</sub>     | 5      | Serial port clock cycle time <sup>3</sup>                                 | 0.6          |     | 12t <sub>CLCL</sub>      |                                       | μs   |
| t <sub>QVXH</sub>     | 5      | Output data setup to clock rising edge <sup>3</sup>                       | 367          |     | 10t <sub>CLCL</sub> -133 |                                       | ns   |
| t <sub>XHQX</sub>     | 5      | Output data hold after clock rising edge <sup>3</sup>                     | 40           |     | 2t <sub>CLCL</sub> -60   |                                       | ns   |
| t <sub>XHDX</sub>     | 5      | Input data hold after clock rising edge <sup>3</sup>                      | 0            |     | 0                        |                                       | ns   |
| t <sub>XHDV</sub>     | 5      | Clock rising edge to input data valid <sup>3</sup>                        |              | 367 |                          | 10t <sub>CLCL</sub> -133              | ns   |
| <b>External Clock</b> |        |                                                                           |              |     |                          |                                       |      |
| t <sub>CHCX</sub>     | 6      | High time <sup>3</sup>                                                    | 17           |     | 17                       | t <sub>CLCL</sub> - t <sub>LOW</sub>  | ns   |
| t <sub>CLCX</sub>     | 6      | Low time <sup>3</sup>                                                     | 17           |     | 17                       | t <sub>CLCL</sub> - t <sub>HIGH</sub> | ns   |
| t <sub>CLCH</sub>     | 6      | Rise time <sup>3</sup>                                                    |              | 20  |                          | 20                                    | ns   |
| t <sub>CHCL</sub>     | 6      | Fall time <sup>3</sup>                                                    |              | 20  |                          | 20                                    | ns   |

#### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and  $\overline{\text{PSEN}}$  = 100 pF, load capacitance for all other outputs = 80 pF.
- These values are characterized but not 100% production tested.

# 80C51 8-bit microcontroller 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

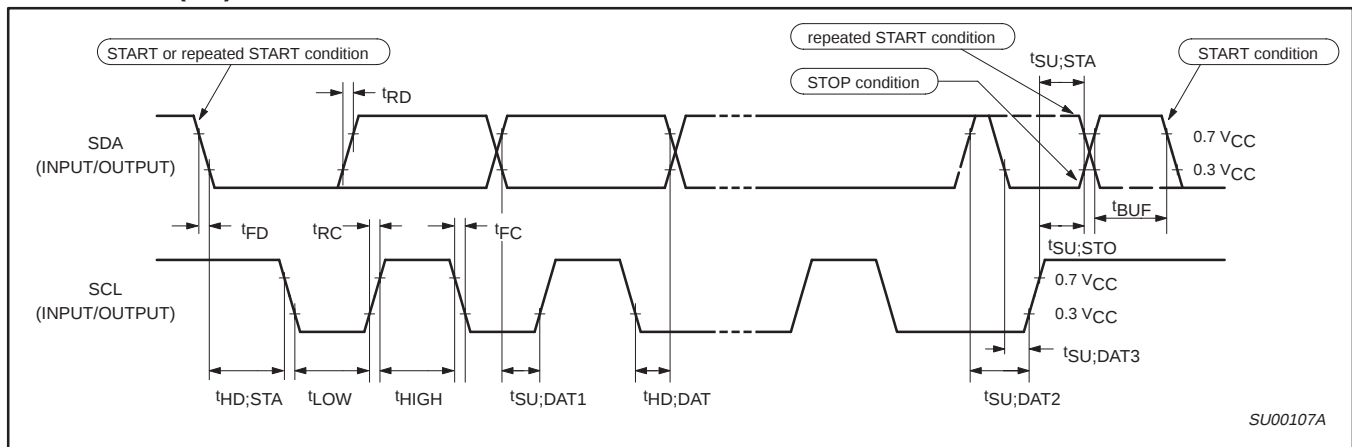
## AC ELECTRICAL CHARACTERISTICS – I<sup>2</sup>C INTERFACE

| SYMBOL                            | PARAMETER                                 | INPUT              | OUTPUT                   |
|-----------------------------------|-------------------------------------------|--------------------|--------------------------|
| <b>SCL TIMING CHARACTERISTICS</b> |                                           |                    |                          |
| $t_{HD; STA}$                     | START condition hold time                 | $\geq 14 t_{CLCL}$ | $> 4.0 \mu s^1$          |
| $t_{LOW}$                         | SCL LOW time                              | $\geq 16 t_{CLCL}$ | $> 4.7 \mu s^1$          |
| $t_{HIGH}$                        | SCL HIGH time                             | $\geq 14 t_{CLCL}$ | $> 4.0 \mu s^1$          |
| $t_{RC}$                          | SCL rise time                             | $\leq 1 \mu s$     | – <sup>2</sup>           |
| $t_{FC}$                          | SCL fall time                             | $\leq 0.3 \mu s$   | $< 0.3 \mu s^3$          |
| <b>SDA TIMING CHARACTERISTICS</b> |                                           |                    |                          |
| $t_{SU; DAT1}$                    | Data set-up time                          | $\geq 250 ns$      | $> 20 t_{CLCL} - t_{RD}$ |
| $t_{SU; DAT2}$                    | SDA set-up time (before rep. START cond.) | $\geq 250 ns$      | $> 1 \mu s^1$            |
| $t_{SU; DAT3}$                    | SDA set-up time (before STOP cond.)       | $\geq 250 ns$      | $> 8 t_{CLCL}$           |
| $t_{HD; DAT}$                     | Data hold time                            | $\geq 0 ns$        | $> 8 t_{CLCL} - t_{FC}$  |
| $t_{SU; STA}$                     | Repeated START set-up time                | $\geq 14 t_{CLCL}$ | $> 4.7 \mu s^1$          |
| $t_{SU; STO}$                     | STOP condition set-up time                | $\geq 14 t_{CLCL}$ | $> 4.0 \mu s^1$          |
| $t_{BUF}$                         | Bus free time                             | $\geq 14 t_{CLCL}$ | $> 4.7 \mu s^1$          |
| $t_{RD}$                          | SDA rise time                             | $\leq 1 \mu s$     | – <sup>2</sup>           |
| $t_{FD}$                          | SDA fall time                             | $\leq 0.3 \mu s$   | $< 0.3 \mu s^3$          |

### NOTES:

- At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
- Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be  $< 1 \mu s$ .
- Spikes on the SDA and SCL lines with a duration of less than  $3 t_{CLCL}$  will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
- $t_{CLCL} = 1/f_{OSC}$  = one oscillator clock period at pin XTAL1. For  $62 ns < t_{CLCL} < 285 ns$  (16 MHz)  $> f_{OSC} > 3.5 MHz$  the SI01 interface meets the I<sup>2</sup>C-bus specification for bit-rates up to 100 kbit/s.

## TIMING SIO1 (I<sup>2</sup>C) INTERFACE



# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address

C – Clock

D – Input data

H – Logic level high

I – Instruction (program memory contents)

L – Logic level low, or ALE

P –  $\overline{\text{PSEN}}$ 

Q – Output data

R –  $\overline{\text{RD}}$  signal

t – Time

V – Valid

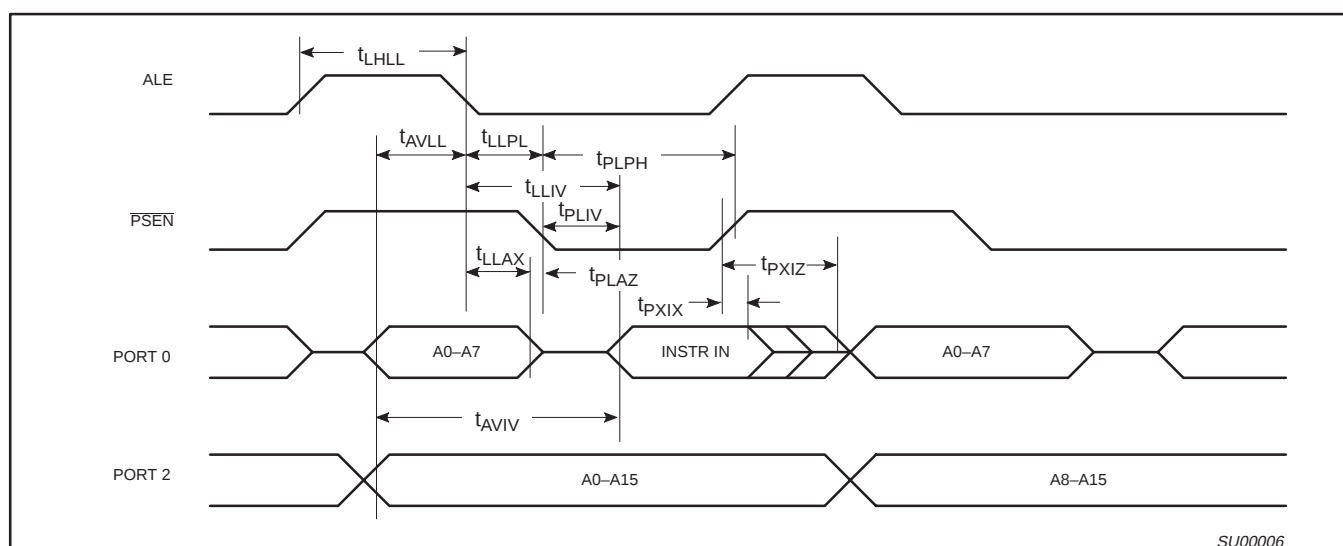
W –  $\overline{\text{WR}}$  signal

X – No longer a valid logic level

Z – Float

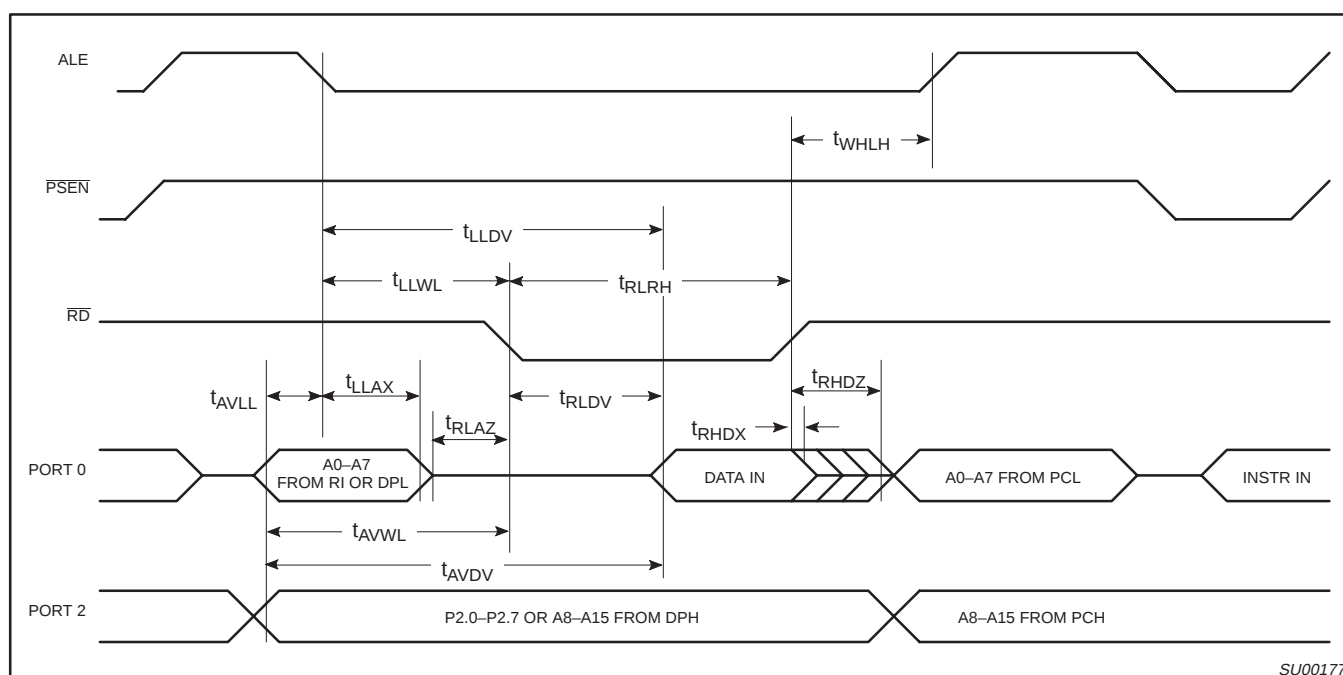
**Examples:**  $t_{\text{AVLL}}$  = Time for address valid to ALE low.

$t_{\text{LLPL}}$  = Time for ALE low to  $\overline{\text{PSEN}}$  low.



SU00006

Figure 1. External Program Memory Read Cycle



SU00177

Figure 2. External Data Memory Read Cycle

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8K/16K, 256 OTP, I<sup>2</sup>C

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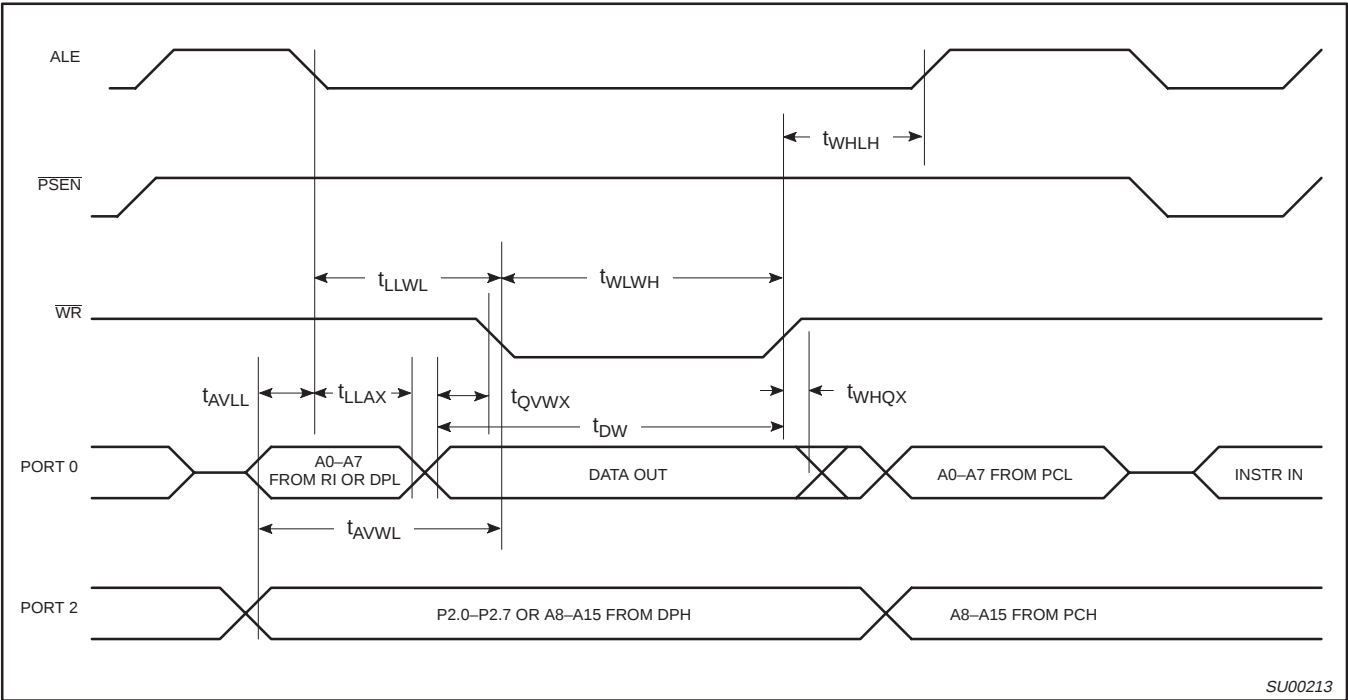


Figure 3. External Data Memory Write Cycle

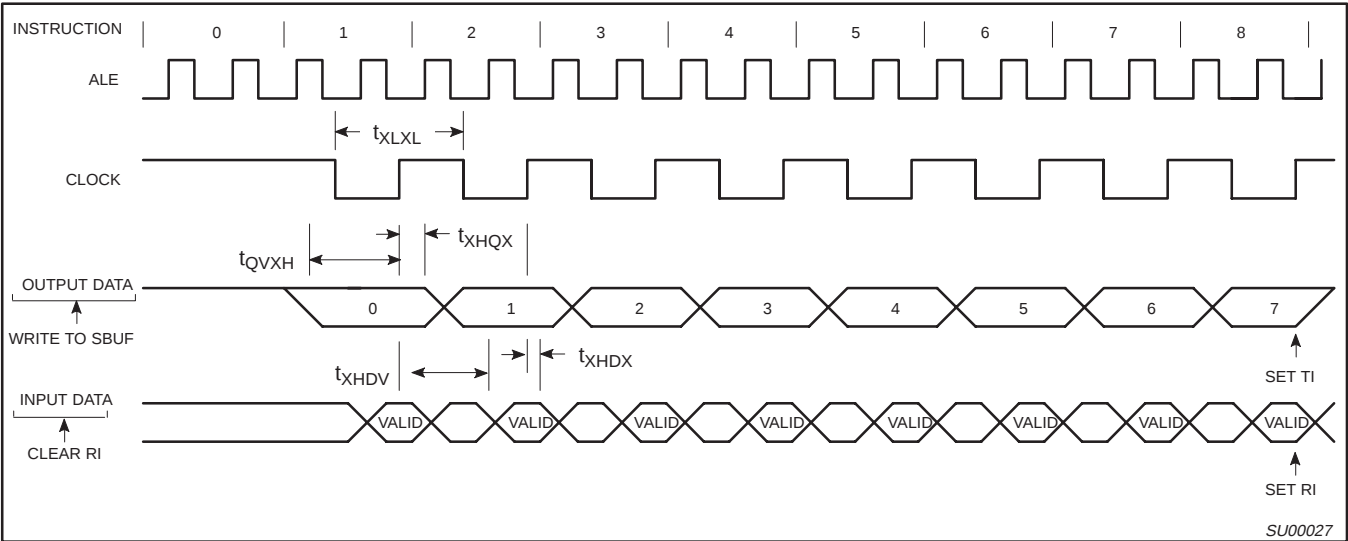


Figure 4. Shift Register Mode Timing

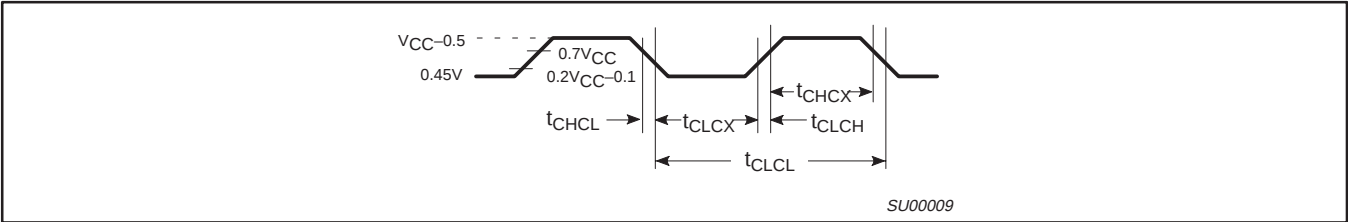


Figure 5. External Clock Drive

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8K/16K, 256 OTP, I<sup>2</sup>C

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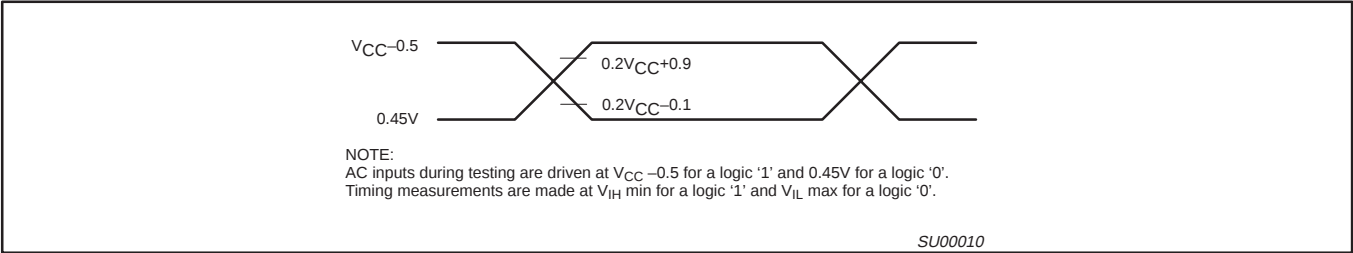


Figure 6. AC Testing Input/Output

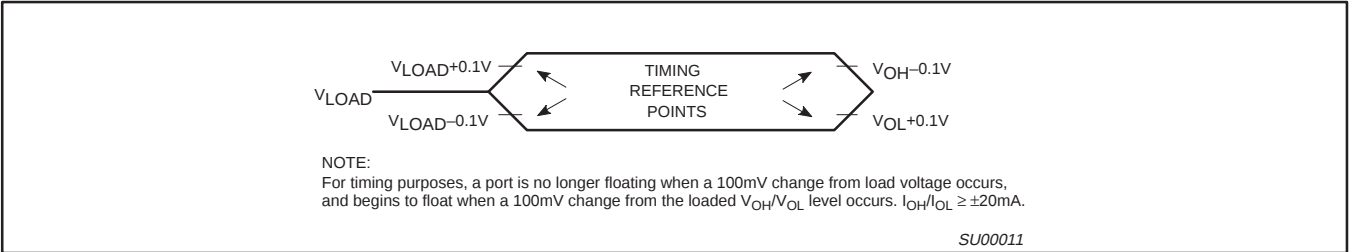


Figure 7. Float Waveform

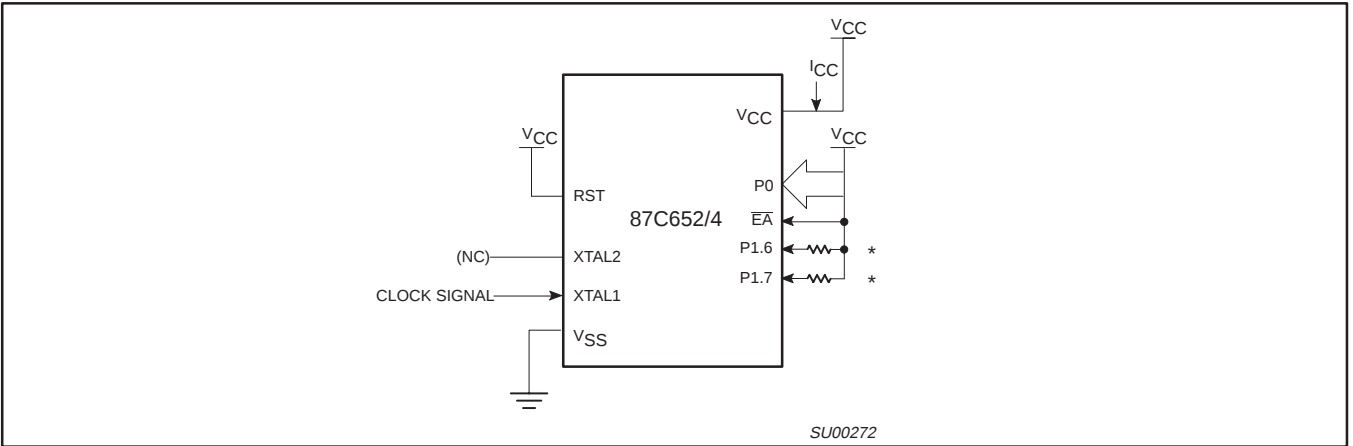


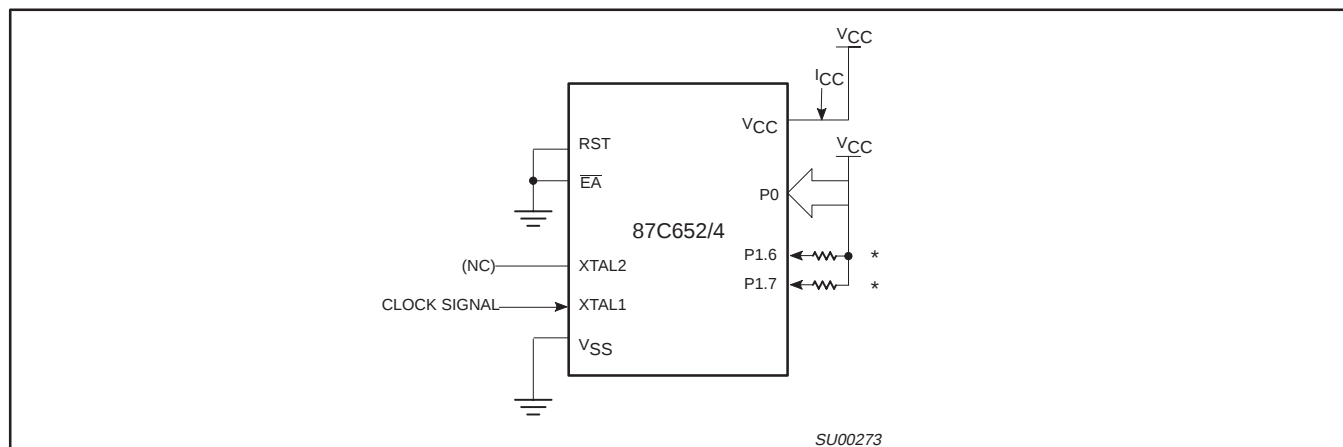
Figure 8. I<sub>CC</sub> Test Condition, Active Mode  
All other pins are disconnected

**NOTE:**  
\* Ports 1.6 and 1.7 should be connected to  $V_{CC}$  through resistors of sufficiently high value such that the sink current into these pins does not exceed the  $I_{OL1}$  specification.

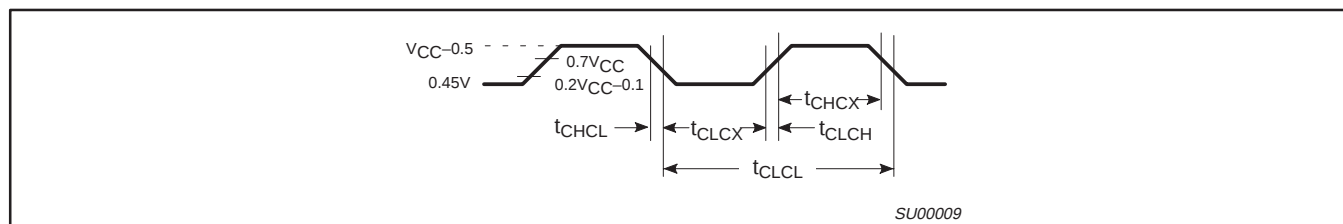
# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

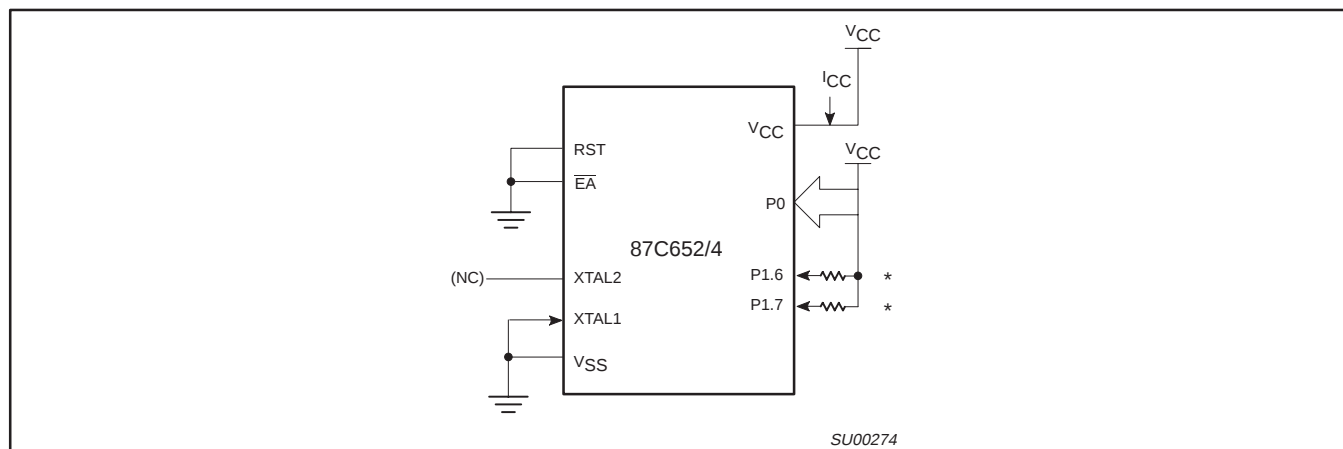
87C652/87C654



**Figure 9.  $I_{CC}$  Test Condition, Idle Mode**  
All other pins are disconnected



**Figure 10. Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes**  
 $t_{CLCH} = t_{CHCL} = 10 \text{ ns}$



**Figure 11.  $I_{CC}$  Test Condition, Power Down Mode**  
All other pins are disconnected.  $V_{CC} = 2 \text{ V to } 5.5 \text{ V}$

### NOTE:

- \* Ports 1.6 and 1.7 should be connected to  $V_{CC}$  through resistors of sufficiently high value such that the sink current into these pins does not exceed the  $I_{OL1}$  specification.

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### EPROM CHARACTERISTICS

The 87C652/87C654 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V<sub>PP</sub> (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C652/87C654 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C652/87C654 manufactured by Philips Components.

Table 4 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

### Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 12. Note that the 87C652/87C654 is running with a 4 to 6 MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as

shown in Figure 12. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 4 are held at the 'Program Code Data' levels indicated in Table 4. The ALE/PROG is pulsed low 25 times as shown in Figure 13.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the EA/V<sub>PP</sub> pin must not be allowed to go above the maximum specified V<sub>PP</sub> level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V<sub>PP</sub> source should be well regulated and free of glitches and overshoot.

### Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for

program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 14. The other pins are held at the 'Verify Code Data' levels indicated in Table 4. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

### Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 15H indicates manufactured by Philips

(031H) = 99H

### Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 4, and which satisfies the timing specifications, is suitable.

**Table 4. EPROM Programming Modes**

| MODE                 | RST | PSEN | ALE/PROG | EA/V <sub>PP</sub> | P2.7 | P2.6 | P3.7 | P3.6 |
|----------------------|-----|------|----------|--------------------|------|------|------|------|
| Read signature       | 1   | 0    | 1        | 1                  | 0    | 0    | 0    | 0    |
| Program code data    | 1   | 0    | 0*       | V <sub>PP</sub>    | 1    | 0    | 1    | 1    |
| Verify code data     | 1   | 0    | 1        | 1                  | 0    | 0    | 1    | 1    |
| Pgm encryption table | 1   | 0    | 0*       | V <sub>PP</sub>    | 1    | 0    | 1    | 0    |
| Pgm lock bit 1       | 1   | 0    | 0*       | V <sub>PP</sub>    | 1    | 1    | 1    | 1    |
| Pgm lock bit 2       | 1   | 0    | 0*       | V <sub>PP</sub>    | 1    | 1    | 0    | 0    |

### NOTES:

1. '0' = Valid low for that pin, '1' = valid high for that pin.

2. V<sub>PP</sub> = 12.75 V ±0.25 V.

3. V<sub>CC</sub> = 5 V ±10% during programming and verification.

\* ALE/PROG receives 25 programming pulses while V<sub>PP</sub> is held at 12.75 V. Each programming pulse is low for 100 μs (±10 μs) and high for a minimum of 10 μs.

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80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

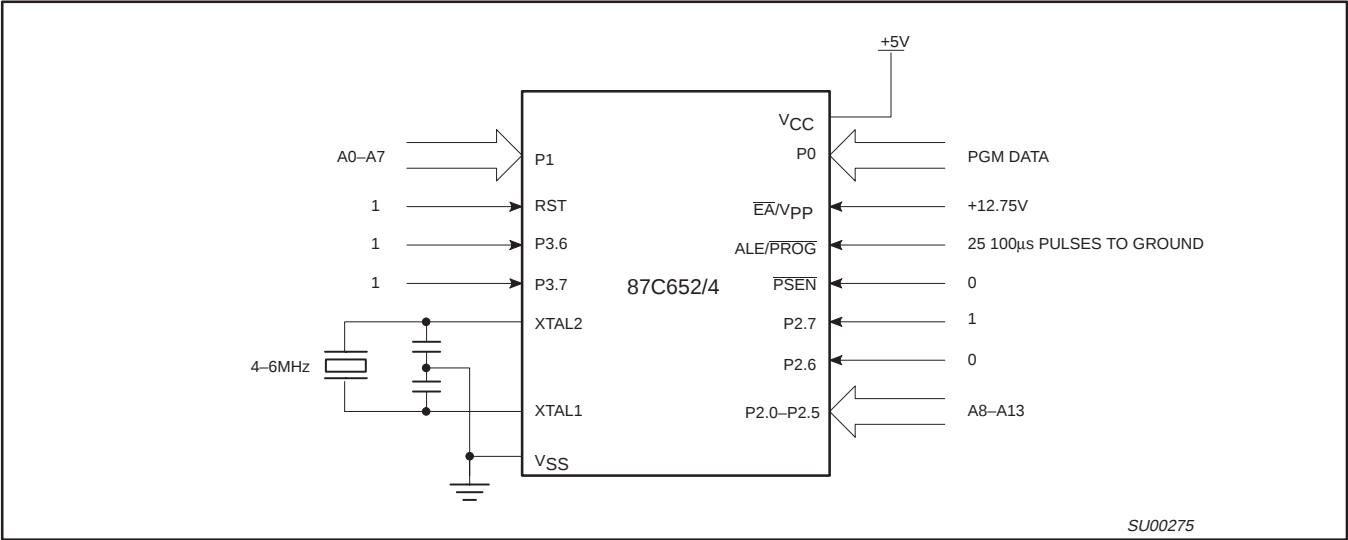


Figure 12. Programming Configuration

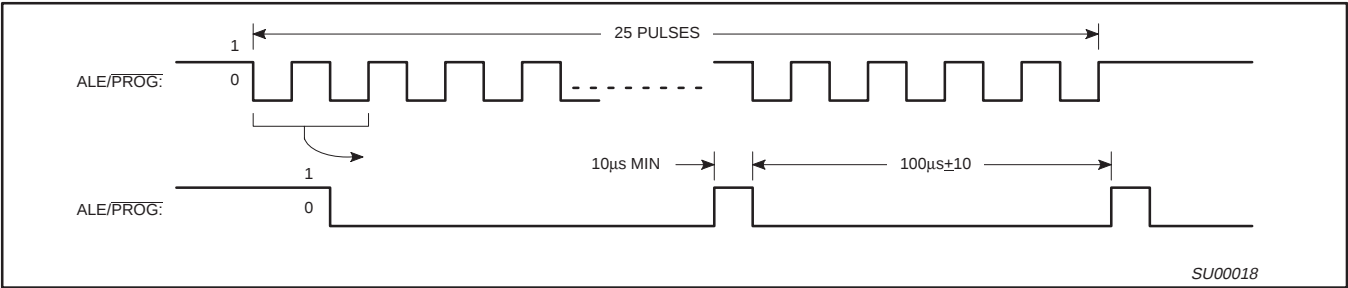


Figure 13. PROG Waveform

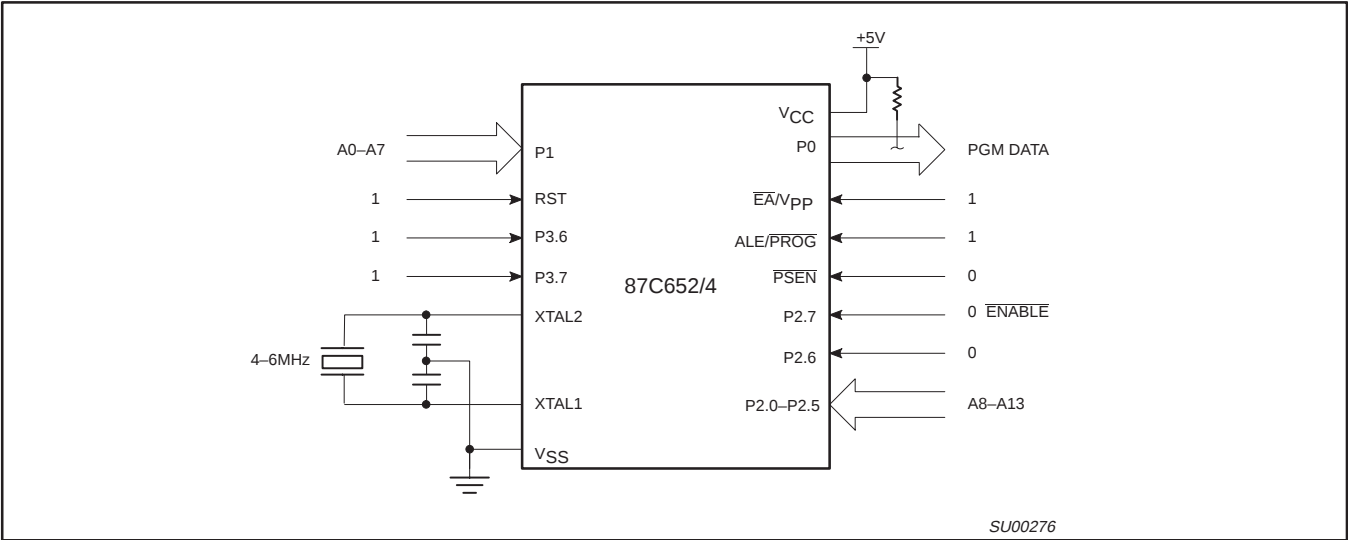


Figure 14. Program Verification

# 80C51 8-bit microcontroller

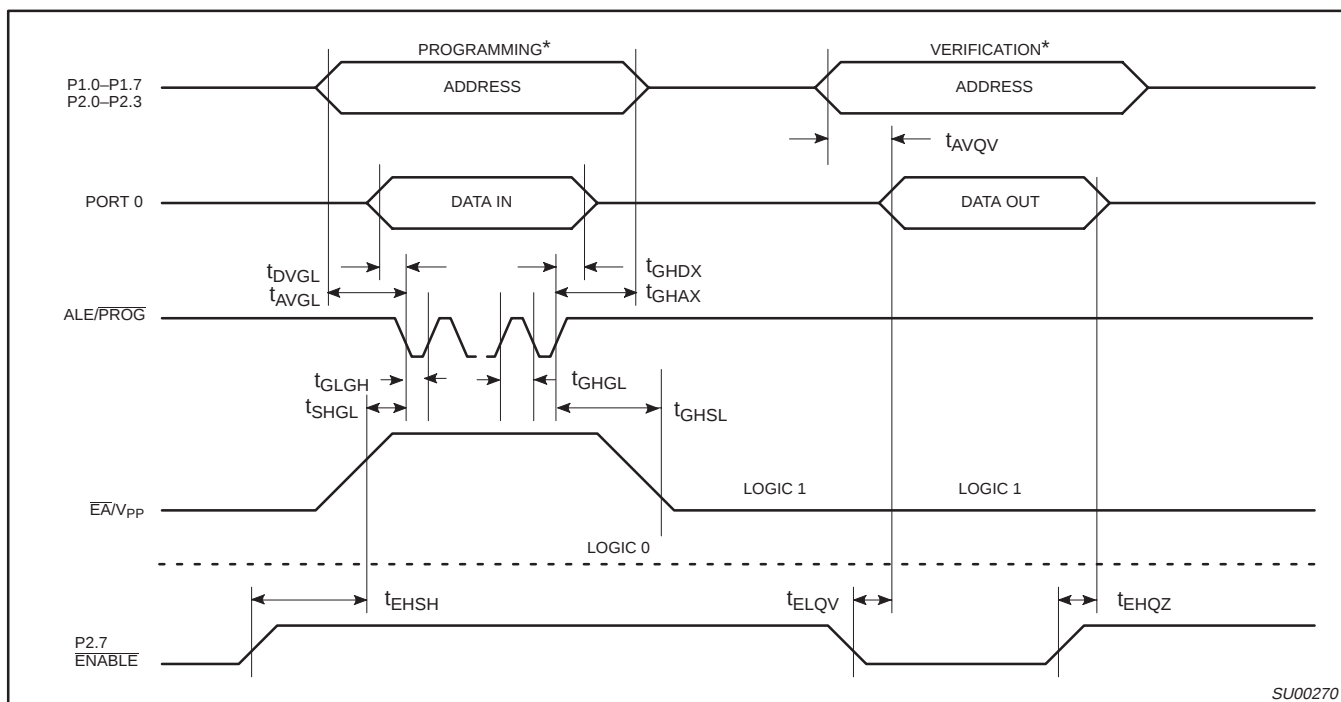
## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

$T_{amb} = 21^{\circ}\text{C}$  to  $+27^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{SS} = 0\text{V}$  (See Figure 15)

| SYMBOL       | PARAMETER                                                     | MIN          | MAX          | UNIT          |
|--------------|---------------------------------------------------------------|--------------|--------------|---------------|
| $V_{PP}$     | Programming supply voltage                                    | 12.5         | 13.0         | V             |
| $I_{PP}$     | Programming supply current                                    |              | 50           | mA            |
| $1/t_{CLCL}$ | Oscillator frequency                                          | 4            | 6            | MHz           |
| $t_{AVGL}$   | Address setup to $\overline{\text{PROG}}$ low                 | $48t_{CLCL}$ |              |               |
| $t_{GHAX}$   | Address hold after $\overline{\text{PROG}}$                   | $48t_{CLCL}$ |              |               |
| $t_{DVGL}$   | Data setup to $\overline{\text{PROG}}$ low                    | $48t_{CLCL}$ |              |               |
| $t_{GHDX}$   | Data hold after $\overline{\text{PROG}}$                      | $48t_{CLCL}$ |              |               |
| $t_{EHS}$    | P2.7 (ENABLE) high to $V_{PP}$                                | $48t_{CLCL}$ |              |               |
| $t_{SHGL}$   | $V_{PP}$ setup to $\overline{\text{PROG}}$ low                | 10           |              | $\mu\text{s}$ |
| $t_{GHS}$    | $V_{PP}$ hold after $\overline{\text{PROG}}$                  | 10           |              | $\mu\text{s}$ |
| $t_{GLGH}$   | $\overline{\text{PROG}}$ width                                | 90           | 110          | $\mu\text{s}$ |
| $t_{AVQV}$   | Address to data valid                                         |              | $48t_{CLCL}$ |               |
| $t_{ELQZ}$   | ENABLE low to data valid                                      |              | $48t_{CLCL}$ |               |
| $t_{EHQZ}$   | Data float after ENABLE                                       | 0            | $48t_{CLCL}$ |               |
| $t_{GHGL}$   | $\overline{\text{PROG}}$ high to $\overline{\text{PROG}}$ low | 10           |              | $\mu\text{s}$ |



SU00270

\* FOR PROGRAMMING VERIFICATION SEE FIGURE 12.  
FOR VERIFICATION CONDITIONS SEE FIGURE 14.

Figure 15. EPROM Programming and Verification



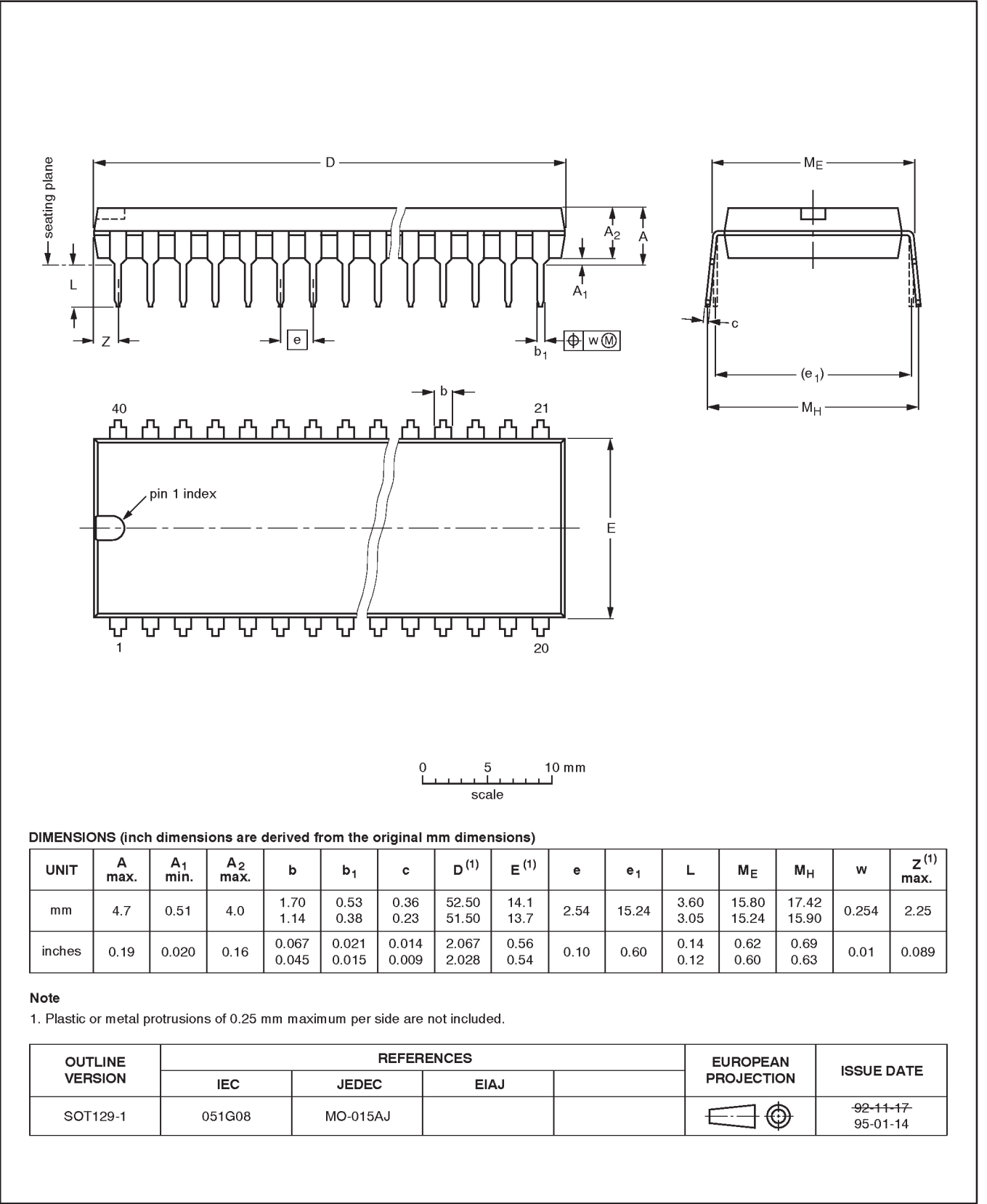
Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

DIP40: plastic dual in-line package; 40 leads (600 mil)

SOT129-1

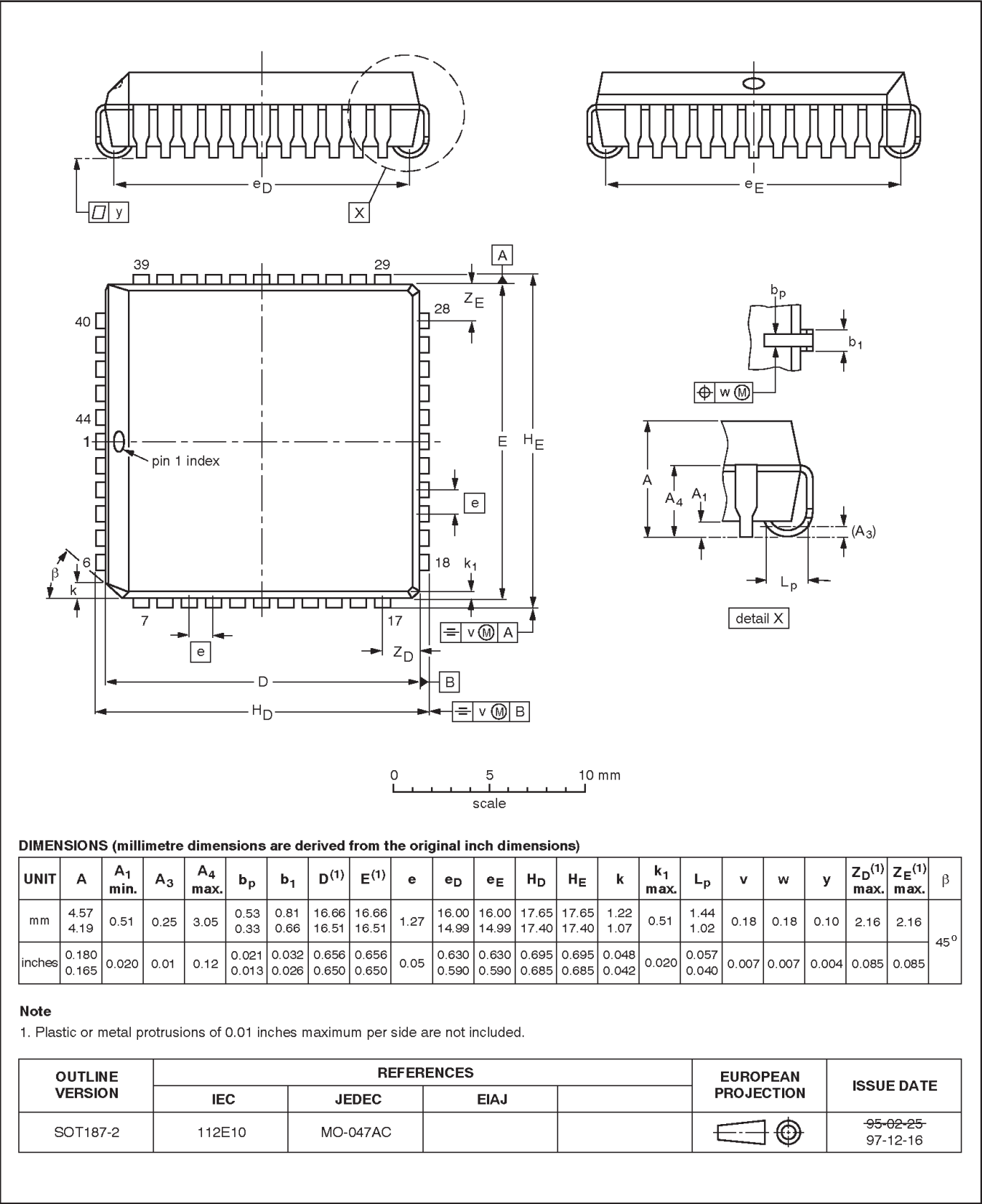


80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

PLCC44: plastic leaded chip carrier; 44 leads

SOT187-2

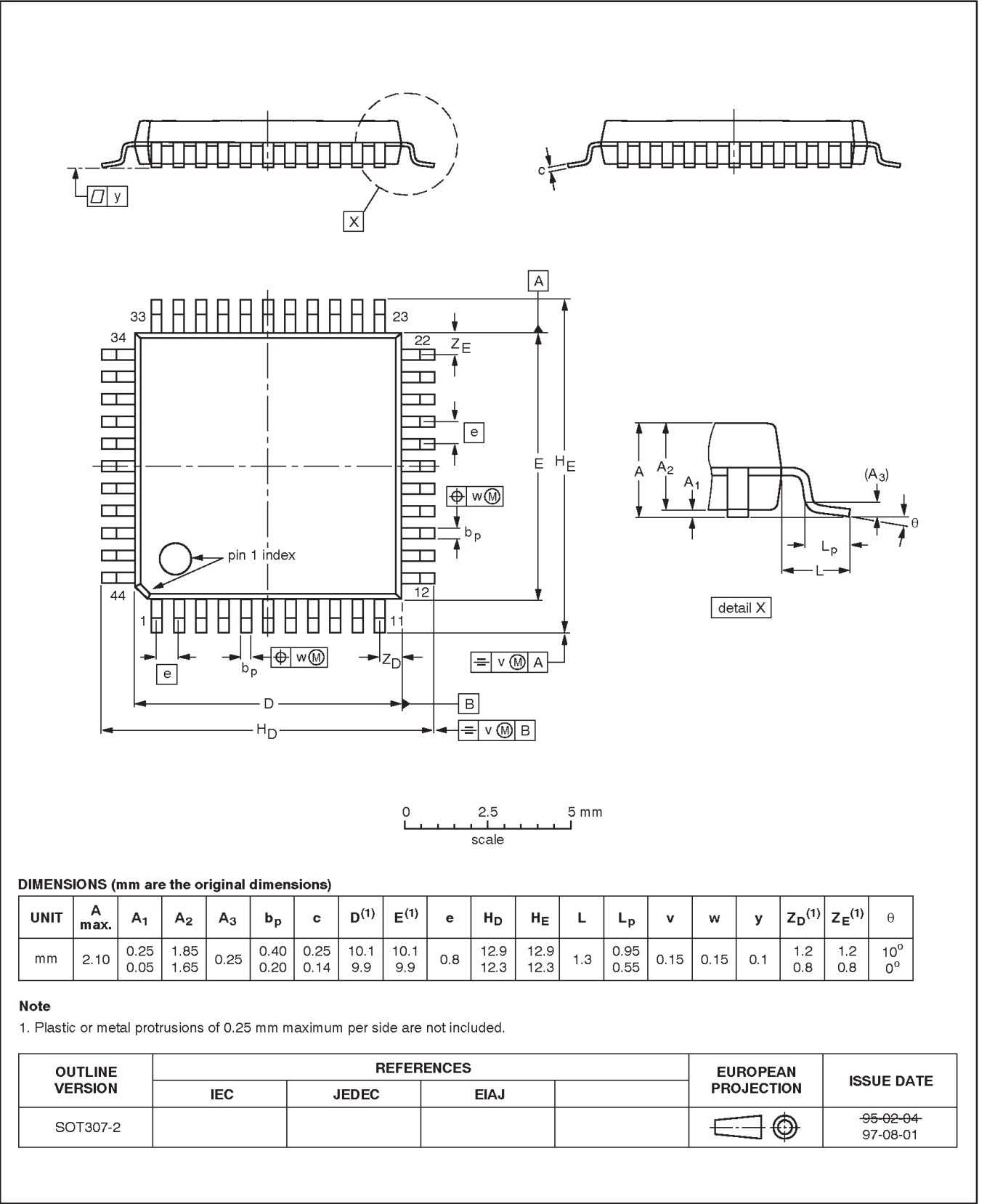


80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



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80C51 8-bit microcontroller  
8K/16K, 256 OTP, I<sup>2</sup>C

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87C652/87C654

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## NOTES

# 80C51 8-bit microcontroller

## 8K/16K, 256 OTP, I<sup>2</sup>C

87C652/87C654

### Data sheet status

| Data sheet status         | Product status | Definition [1]                                                                                                                                                                                                                                             |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 07-99

Document order number:

9397-750-06607

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