



**AO4821**

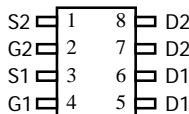
**Dual P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

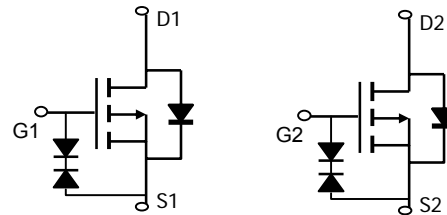
The AO4821 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected. *Standard Product AO4821 is Pb-free (meets ROHS & Sony 259 specifications). AO4821L is a Green Product ordering option. AO4821 and AO4821L are electrically*

**Features**

- $V_{DS}$  (V) = -12V
- $I_D$  = -8 A ( $V_{GS}$  = -4.5V)
- $R_{DS(ON)} < 18m\Omega$  ( $V_{GS}$  = -4.5V)
- $R_{DS(ON)} < 22m\Omega$  ( $V_{GS}$  = -2.5V)
- $R_{DS(ON)} < 29m\Omega$  ( $V_{GS}$  = -1.8V)
- ESD Rating: 4KV HBM



**SOIC-8**



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current <sup>A</sup>	$T_A=25^\circ\text{C}$	-8	A
	$T_A=70^\circ\text{C}$	-6.7	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	-20	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	2	W
	$T_A=70^\circ\text{C}$	1.28	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>		Steady-State	74	
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JL}$	35	40	$^\circ\text{C/W}$

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-12			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-9.6\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 4.5\text{V}$ $V_{DS}=0\text{V}$ , $V_{GS}=\pm 8\text{V}$			$\pm 1$ $\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-0.3	-0.55	-1	
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-4.5\text{V}$ , $I_D=-8\text{A}$ $T_J=125^\circ\text{C}$ $V_{GS}=-2.5\text{V}$ , $I_D=-8\text{A}$ $V_{GS}=-1.8\text{V}$ , $I_D=-5\text{A}$		14.8 19 18.3 22.4	18 23 22 29	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-8\text{A}$		34		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.74	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-2.5	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance			3960		pF
$C_{oss}$	Output Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-6\text{V}$ , $f=1\text{MHz}$		910		pF
$C_{rss}$	Reverse Transfer Capacitance			757		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		6.9		$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g$	Total Gate Charge			37		nC
$Q_{gs}$	Gate Source Charge	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-6\text{V}$ , $I_D=-8\text{A}$		4.4		nC
$Q_{gd}$	Gate Drain Charge			11		nC
$t_{D(on)}$	Turn-On Delay Time			15		ns
$t_r$	Turn-On Rise Time	$V_{GS}=-4.5\text{V}$ , $V_{DS}=-6\text{V}$ , $R_L=0.75\Omega$ , $R_{GEN}=3\Omega$		43		ns
$t_{D(off)}$	Turn-Off Delay Time			158		ns
$t_f$	Turn-Off Fall Time			95		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-8\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		63		ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-8\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		56		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80 $\mu\text{s}$  pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

Rev2: August 2005

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

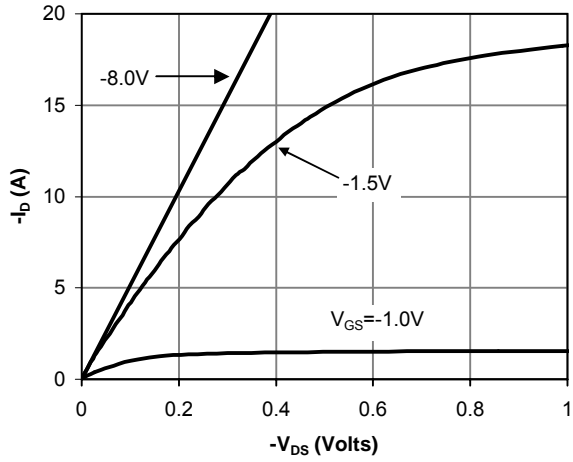


Fig 1: On-Region Characteristics

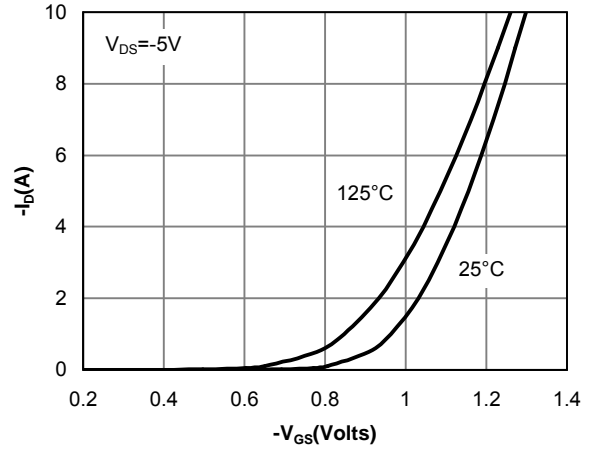


Figure 2: Transfer Characteristics

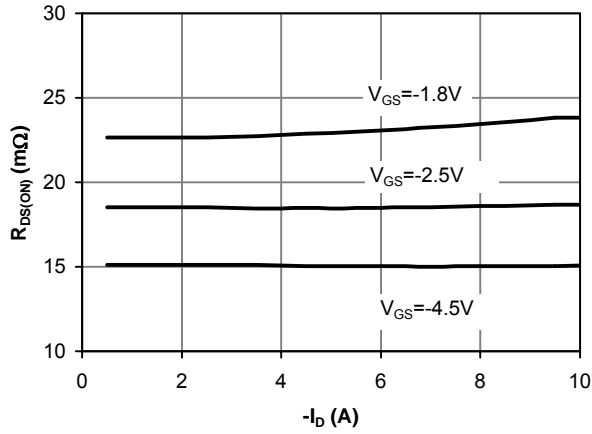


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

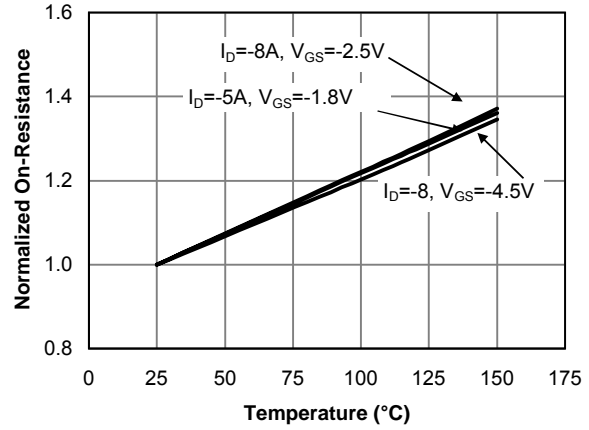


Figure 4: On-Resistance vs. Junction Temperature

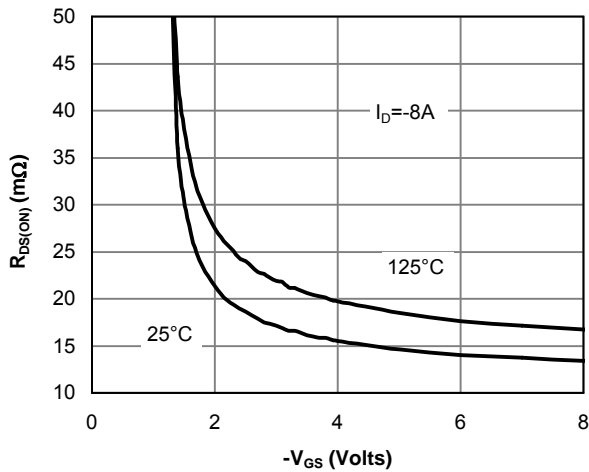


Figure 5: On-Resistance vs. Gate-Source Voltage

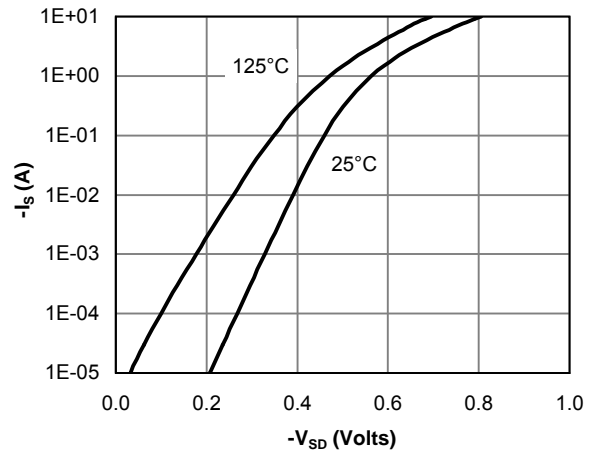


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

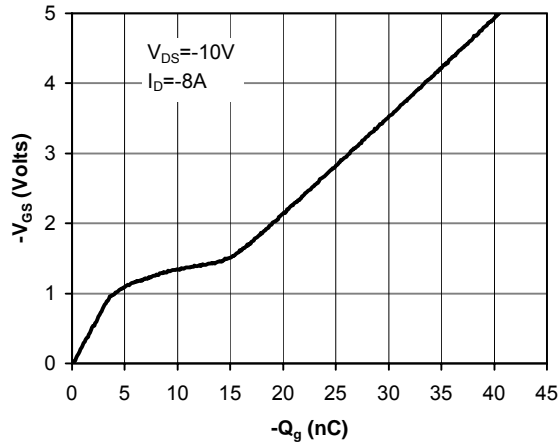


Figure 7: Gate-Charge Characteristics

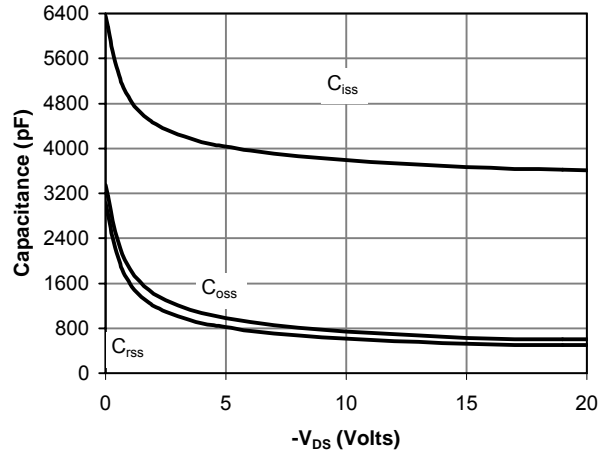


Figure 8: Capacitance Characteristics

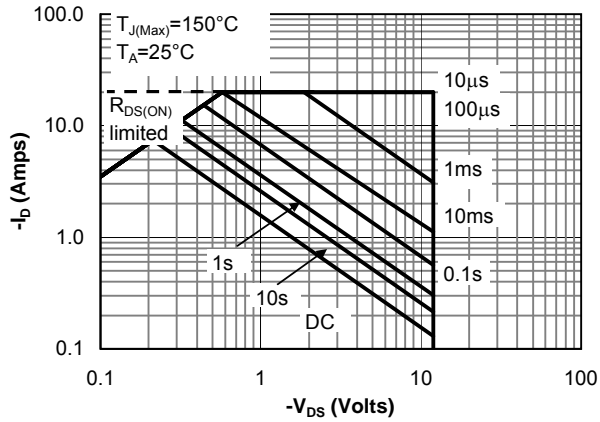


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

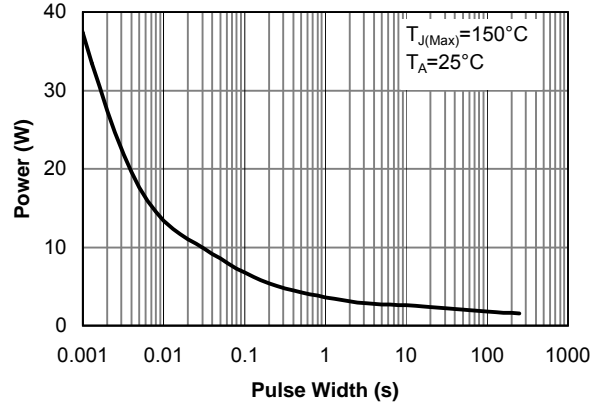


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

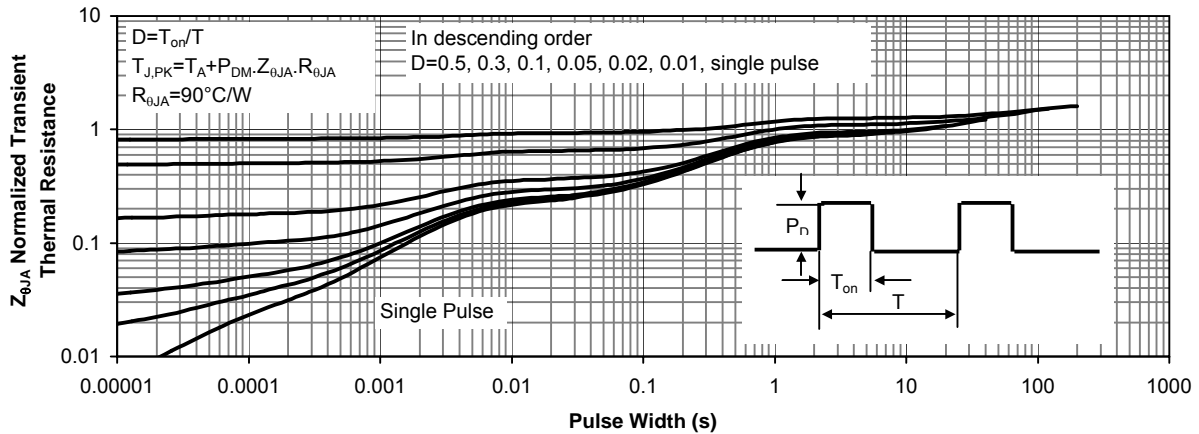


Figure 11: Normalized Maximum Transient Thermal Impedance