Audio sound controller

BD3861FS

The BD3861FS is an audio sound controller IC for micro-component stereo systems. Tone and volume can be controlled easily by two-line serial control from micro-controller.

●Applications

Micro-component stereo systems, radio cassette players and mini-component stereo systems

●Features

1) Built-in volume, tone (bass, middle and treble), input gain amplifier and input selector.
2) The volume control of resistance ladder type allows the low distortion and low noise in Bi-CMOS process.
3) Two-line serial interface.
4) The built-in input gain amplifier reduces the needs of external input, and this IC is suitable for space-saving design.
5) Residual noise can be reduced by separating the front stage volume control from the rear stage volume control.

●Absolute maximum ratings (Ta=25°C)

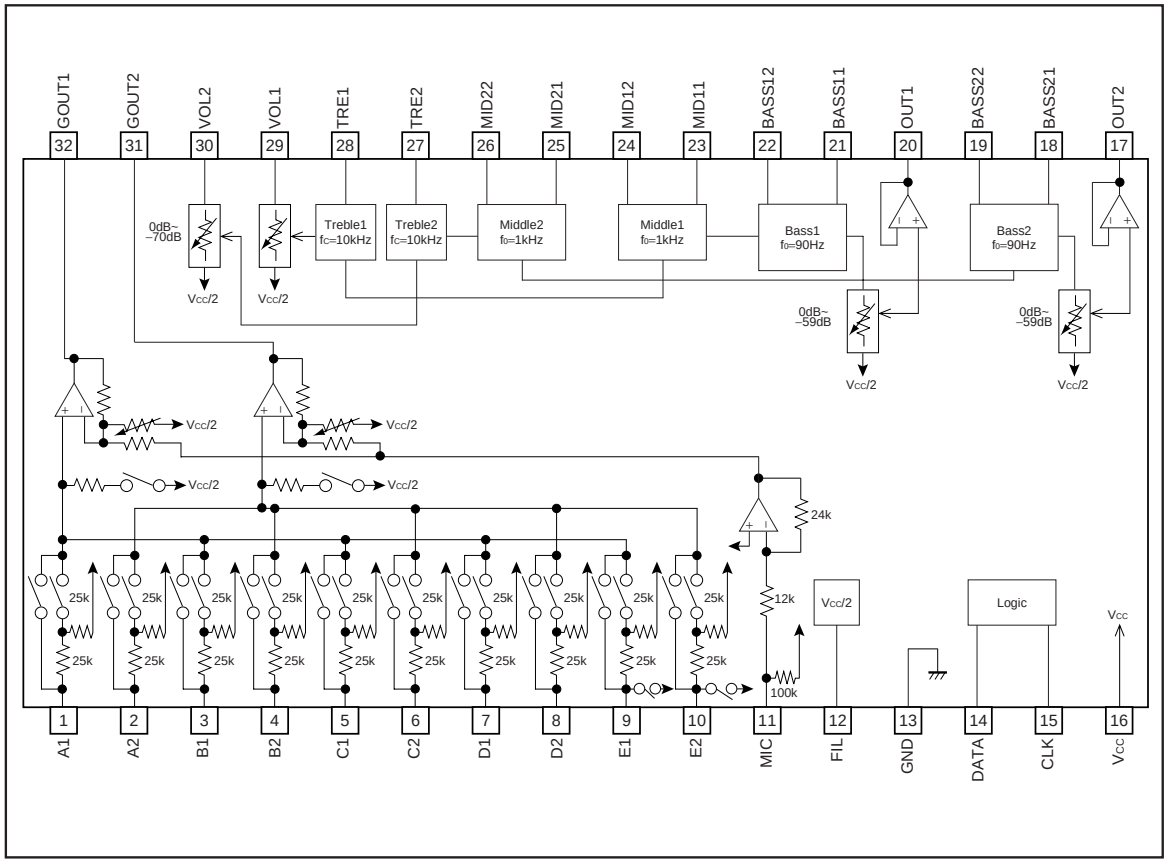
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	10	V
Power dissipation	Pd	800*	mW
Operating temperature	Topr	−25 to +75	°C
Storage temperature	Tstg	−55 to +150	°C

*Reduced by 6.4mW for each increase in Ta of 1°C over 25°C.

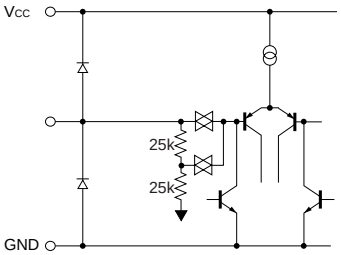
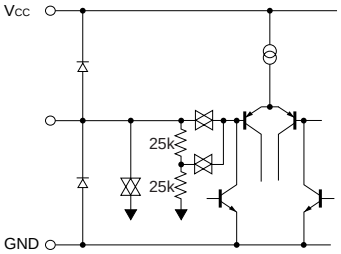
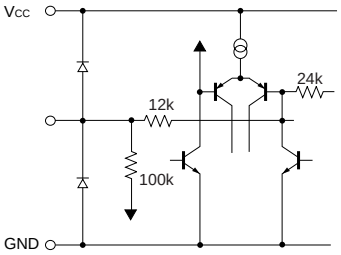
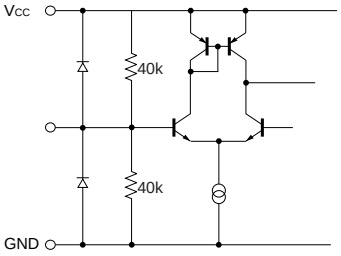
●Recommended operating conditions (Ta=25°C)

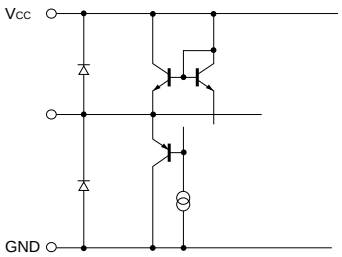
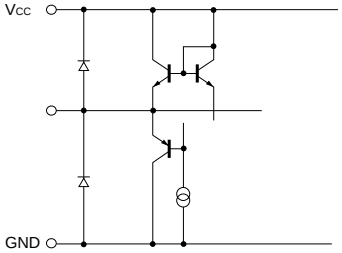
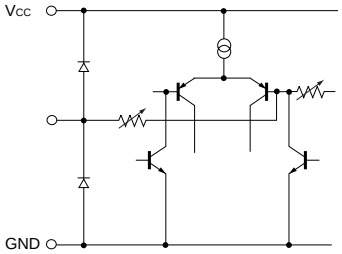
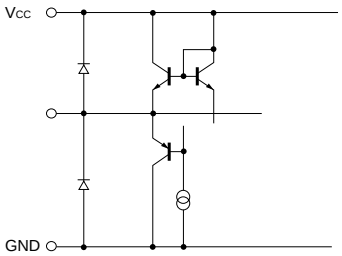
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	6.5	−	9.5	V

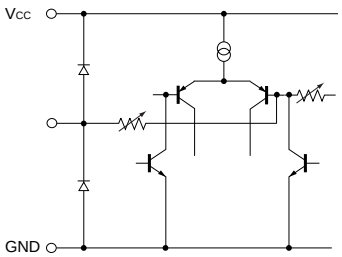
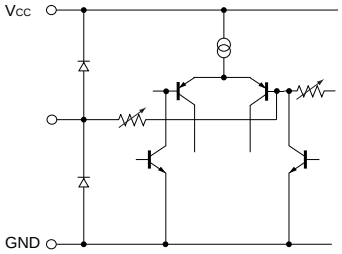
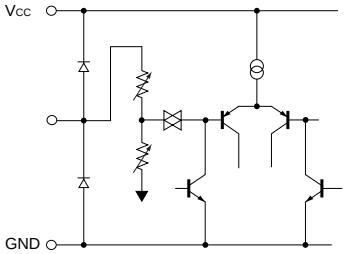
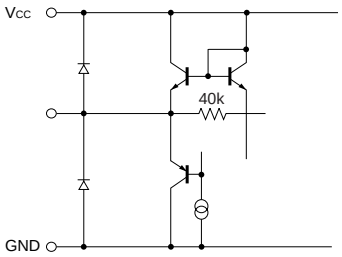
●**Block diagram**

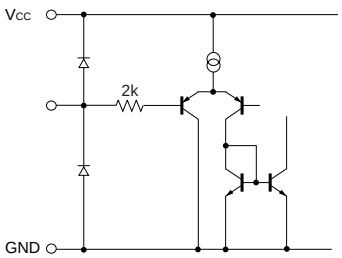


●Pin equivalent circuit and description

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
1 2 3 4 5 6 7 8	A1 A2 B1 B2 C1 C2 D1 D2	Vcc/2		A pin for inputting a sound signal. It is suitable for input of CD, MD, tuner and tape. Connect this pin to a front stage circuit through a coupling capacitor.
9 10	E1 E2	Vcc/2		A pin for inputting a sound signal. It is suitable for input from outside of the pin.
11	MIC	Vcc/2		A pin for microphone input.
12	FIL	Vcc/2		Vcc/2 Voltage for power supply of signal system.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
17 20	OUT2 OUT1	Vcc/2		A pin for outputting a sound signal. Connect this pin to a rear stage circuit through a coupling capacitor.
18 21	BASS21 BASS11	Vcc/2		A pin for setting central frequency (fo) of bass and for setting gain.
19 22	BASS22 BASS12	Vcc/2		A pin for setting central frequency (fo) of bass and for setting gain.
23 25	MID11 MID21	Vcc/2		A pin for setting central frequency (fo) of middle and for setting gain.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
24 26	MID12 MID22	Vcc/2		A pin for setting central frequency (fo) of middle and for setting gain.
27 28	TRE2 TRE1	Vcc/2		A pin for setting cut-off frequency (fc) of treble and for setting gain.
29 30	VOL1 VOL2	Vcc/2		A pin for inputting sound signal into input volume control. The input impedance is 36kΩ (upon Typ.).
31 32	GOUT2 GOUT1	Vcc/2		A pin for outputting input gain.

Pin No.	Pin name	Pin voltage	Equivalent circuit	Pin description
14 15	DATA CLK	–		A pin for inputting a serial control data.
16	Vcc	Vcc	–	Power supply pin.
13	GND	0V	–	A ground pin.

●**Electrical characteristics** (Unless specified particularly, V_{CC}=9V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, RL=10kΩ, Ta=25°C, INPUT Gain=0dB, VOL=0dB, Bass, Middle, Treble=0dB) Measurement circuit is Fig.1.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	SW No. 1/4	2/5	3/8	7	8	9/10	11/12	Select address/Serial data (HEX notation) 1	2	3	4-1	4-2	5-1	5-2	Measurement point
<TOTAL>																					
Circuit current	IQ	–	13.0	26.0	mA	Without signal	1	1	–	2	1	1	2	00	02	01	05	0D	03	0B	I
Output voltage gain	GV	–1.5	0.0	1.5	dB	G_V=20log(O1/V_{IN})	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B	O1
						G_V=20log(O2/V_{IN})															O2
Total harmonic distortion	THD	–	0.02	0.08	%	V_{IN}=2Vrms 400~30kHz BPF	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B	O1
																					O2
Maximum output voltage	V_{OM}	2.0	2.5	–	Vrms	THD=1%	1	2	2	2	2	1	2	00	02	01	05	0D	03	0B	O1
																					O2
Maximum noise voltage	V_{NO}	–	8.0	15.0	μVrms	Rg=0kΩ, IHF–A	1	1	–	2	2	1	2	00	02	01	05	0D	03	0B	O1
																					O2
Cross-talk between channels	CT	–	–80	–70	dB	Rg=0kΩ, IHF–A CT=20log(O2/O1)	1	2/1	2/–	2	2	1	2	00	02	01	05	0D	03	0B	O2
						CT=20log(O1/O2)		1/2	–/2												O1
<INPUT>																					
6dBSW gain	G_{V6}	5	6	7	dB	V_{IN}=200mVrms G_{V6}=20log(G1/V_{IN})	1	2	2	2	2	1	1	00	02	11	05	0D	03	0B	G1
						G_{V6}=20log(G2/V_{IN})															G2
Input voltage gain1 *	Gvmaxl1	–1	*1	+1	dB	V_{IN}=200mVrms From 0 to 10dB Gvmaxl1=20log(G1/V_{IN})	1	2	2	2	2	1	1	00	02	01	*3 A5	0D	03	0B	G1
						Gvmaxl1=20log(G2/V_{IN})															G2
Input voltage gain2 *	Gvmaxl2	–1.5	*2	+1.5	dB	V_{IN}=200mVrms From 12 to 20dB Gvmaxl1=20log(G1/V_{IN})	1	2	2	2	2	1	1	00	02	01	*4 F5	0D	03	0B	G1
						Gvmaxl1=20log(G2/V_{IN})															G2
Input gain switch step	Gvmaxlst	–	2	–	dB	From 0 to 20dB	1	2	2	2	2	1	1	00	02	01	–	0D	03	0B	G1
																					G2
INPUT total harmonic distortion	THD_I	–	0.02	0.08	%	V_{IN}=2Vrms 400~30kHz BPF	1	2	2	2	2	1	1	00	02	01	05	0D	03	0B	G1
																					G2
INPUT maximum output voltage	V_{OMI}	2.0	2.5	–	dB	THD=1%	1	2	2	2	2	1	1	00	02	01	05	0D	03	0B	G1
																					G2
Cross-talk between selectors	CS	–	–80.0	–70.0	dB	Rg=0kΩ, IHF–A CS=20log(G1/V_{IN})	1	2	2	2	2	1	1	00	02	81	05	0D	03	0B	G1
						CS=20log(G2/V_{IN})															G2
Input resistance	R_I	35.0	50.0	65.0	kΩ	R_I=51k×V_{R1}/ (V_{IN}-V_{R1})	1	2	1	2	2	1	1	00	02	01	05	0D	03	0B	V_{R1}
						R_I=51k×V_{R2}/ (V_{IN}-V_{R2})															V_{R2}
"E" input SW attenuation	G_{RE}	–	–20.0	–15.0	dB	G_{RE}=20log(G1/V_{IN})	5	2	2	2	2	1	1	00	02	29	05	0D	03	0B	G1
						G_{RE}=20log(G2/V_{IN})															G2
<INPUT Volume>																					
Input Volume Gain1 *	G_{IV1}	–2	*5	+2	dB	From 0 to –50dB G_{IV1}=20log(O1/V_{IN})	1	1	–	2	2	2	1	00	*7 1A	01	05	0D	03	0B	O1
						G_{IV1}=20log(O2/V_{IN})															O2
Input Volume Gain2 *	G_{IV2}	–3	*6	+3	dB	From –54 to –70dB G_{IV2}=20log(O1/V_{IN})	1	1	–	2	2	2	1	00	*8 7A	01	05	0D	03	0B	O1
						G_{IV2}=20log(O2/V_{IN})															O2
Volume switch step1	G_{IVst1}	–	2	–	dB	From 0 to –50dB	1	1	–	2	2	2	1	00	–	01	05	0D	03	0B	O1
																					O2
Volume switch step2	G_{IVst2}	–	4	–	dB	From –54 to –70dB	1	1	–	2	2	2	1	00	–	01	05	0D	03	0B	O1
																					O2
MUTE level	GminI	–	–	–90.0	dB	IHF–A G_{minI}=20log(O1/V_{IN})	1	1	–	2	2	2	1	00	FA	01	05	0D	03	0B	O1
						G_{minI}=20log(O2/V_{IN})															O2
<OUTPUT Volume>																					
Output Volume Gain *	G_{OV}	–1	*9	+1	dB	From 0 to –59dB G_{OV}=20log(O1/V_{IN})	1	1	–	2	2	2	1	*10 DC	02	01	05	0D	03	0B	O1
						G_{OV}=20log(O2/V_{IN})															O2
OUTPUT switch step	G_{OVst}	–	1	–	dB	From 0 to –59dB	1	1	–	2	2	2	1	–	02	01	05	0D	03	0B	O1
																					O2
MUTE level	GminO	–	–	–90.0	dB	IHF–A G_{minO}=20log(O1/V_{IN})	1	1	–	2	2	2	1	FC	02	01	05	0D	03	0B	O1
						G_{minO}=20log(O2/V_{IN})															O2

* It shows a specified value at the deviation from the setting value.
*1 0.2.4.6.8.10dB
*2 12.14.16.18.20dB
*3 Setting 10dB
*4 Setting 20dB
*5 From 0 to –50dB –2dB/STEP
*6 From –54 to –70dB –4dB/STEP
*7 Setting –50dB
*8 Setting –70dB
*9 From 0 to –59dB –1dB/STEP
*10 Setting –59dB

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		SW No. 1/4	2/5	3/8	7	8	9/10	11/12	Select address/Serial data (HEX notation) 1	2	3	4-1	4-2	5-1	5-2	Measurement point
<BASS>																						
Maximum Bass boost gain	G_{BB}	12	14	16	dB	V_{IN}=200mVrms, f=90Hz	$G_{BB}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	ED	03	0B	O1
							$G_{BB}=20\log(O2/V_{IN})$																O2
Maximum Bass cut gain	G_{BC}	–16	–14	–12	dB	V_{IN}=200mVrms, f=90Hz	$G_{BC}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	FD	03	0B	O1
							$G_{BC}=20\log(O2/V_{IN})$																O2
Bass switch step	G_{BST}	–	2	–	dB	V_{IN}=200mVrms, f=90Hz		1	2	2	2	2	1	2	00	02	01	05	–	03	0B	O1
																						O2
<MIDDLE>																						
Maximum Middle boost gain	G_{MB}	10	12	14	dB	V_{IN}=200mVrms	$G_{MB}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	0D	E3	0B	O1
							$G_{MB}=20\log(O2/V_{IN})$																O2
Maximum Middle cut gain	G_{MC}	–14	–12	–10	dB	V_{IN}=200mVrms	$G_{MC}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	0D	F3	0B	O1
							$G_{MC}=20\log(O2/V_{IN})$																O2
Middle switch step	G_{MST}	–	2	–	dB	V_{IN}=200mVrms		1	2	2	2	2	1	2	00	02	01	05	0D	–	0B	O1
																						O2
<TREBLE>																						
Maximum Treble boost gain	G_{TB}	10	12	14	dB	V_{IN}=200mVrms, f=10kHz	$G_{TB}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	0D	03	EB	O1
							$G_{TB}=20\log(O2/V_{IN})$																O2
Maximum Treble cut gain	G_{TC}	–14	–12	–10	dB	V_{IN}=200mVrms, f=10kHz	$G_{TC}=20\log(O1/V_{IN})$	1	2	2	2	2	1	2	00	02	01	05	0D	03	FB	O1
							$G_{TC}=20\log(O2/V_{IN})$																O2
Treble switch step	G_{TST}	–	2	–	dB	V_{IN}=200mVrms, f=10kHz		1	2	2	2	2	1	2	00	02	01	05	0D	03	–	O1
																						O2
<Microphone amplifier>																						
Microphone voltage gain	G_{MIC}	4.5	6.0	7.5	dB	V_{IN}=200mVrms	$G_{MIC}=20\log(O1/V_{IN})$	1	1	–	1	2	1	2	00	02	01	05	0D	03	0B	O1
							$G_{MIC}=20\log(O2/V_{IN})$																O2

∗ It shows a specified value at the deviation from the setting value.

●**Measurement circuit**

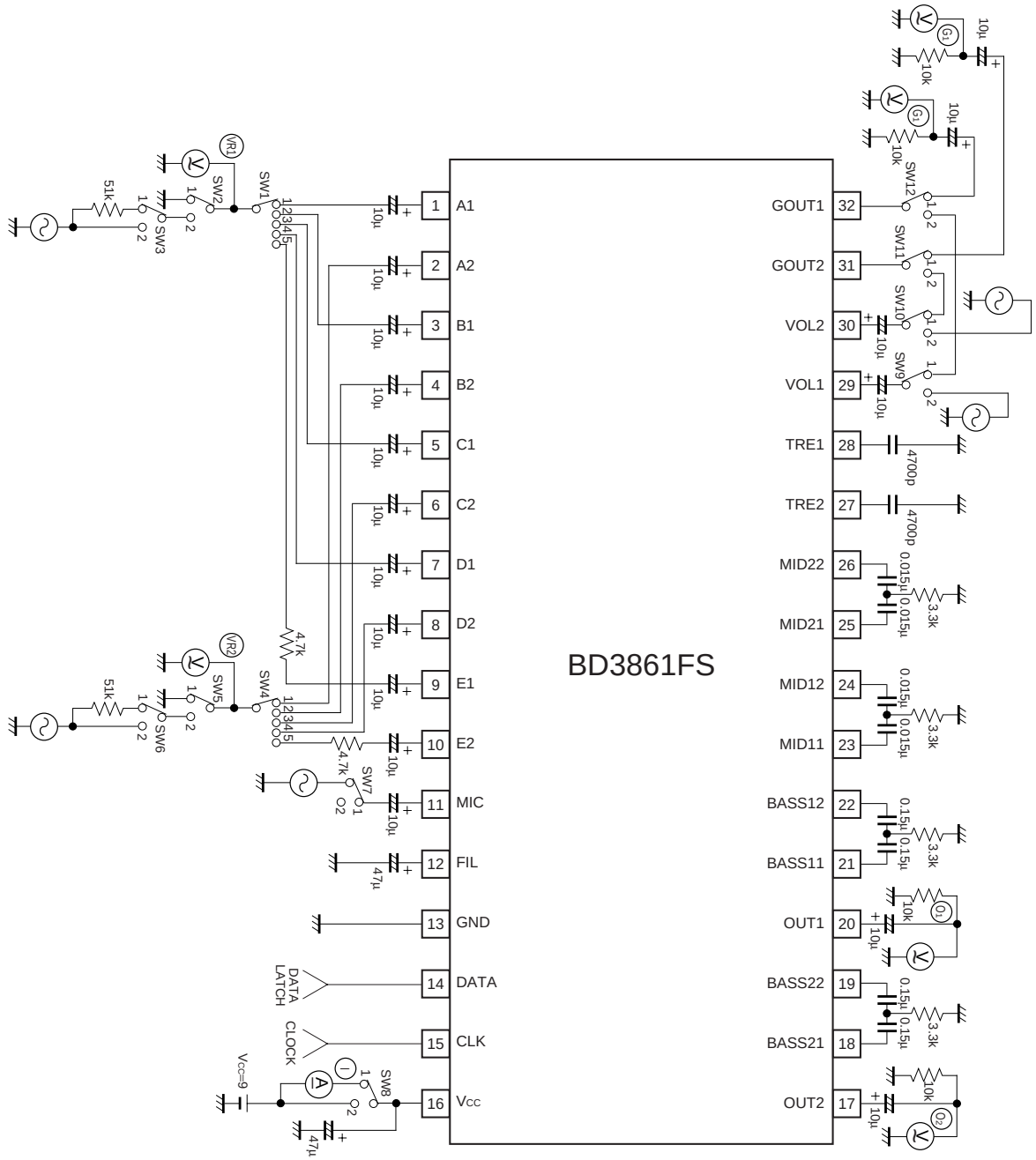


Fig.1

●Attached components

External Parts of measurement circuit.

(1) Element marked with ∗
- Carbon-film resistor: ±1%
- Film capacitor: ±1%
- Ceramic capacitor: ±1%

(2) Unless specified particularly, use the following external parts:
- Carbon-film resistor: ±5%
- Film capacitor: ±20%
- Electrolytic capacitor: ±20%

Notes on wiring

(1) GND shall be wired solidly.

(2) Wiring pattern of CLK and DATA shall be away from that of analog unit and cross talk shall not be acceptable.

(3) Wiring pattern of CLK and DATA of shall not be parallel if possible. They shall be shielded, if they are adjacent to each other.

●Circuit operations

Specifications for control signal

(1) Timing of control signal
- Data is read at a leading edge of clock.
- Latch is read at a trailing edge of clock.
- Be sure to set DATA to LOW after latching.

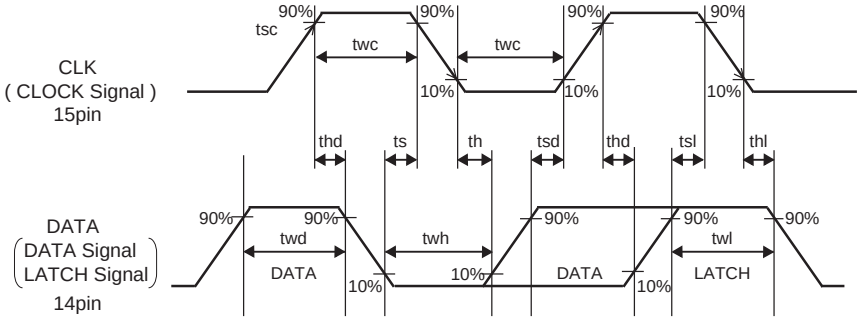


Fig.2

Constant of timing chart (Ta=25°C, V_{CC}=9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
"High" input voltage	V_{IH}	2.6	–	5.5	V
"Low" input voltage	V_{IL}	0	–	1.1	V
Clock width	twc	2.0	–	–	µs
Data width	twd	2.0	–	–	µs
Latch width	twl	2.0	–	–	µs
"Low" hold width	twh	2.0	–	–	µs
Setup time (DATA→CLK)	tsd	1.0	–	–	µs
Hold time (CLK→DATA)	thd	1.0	–	–	µs
Setup time (CLK→LATCH)	tsl	1.0	–	–	µs
Hold time (DATA→LATCH)	thl	1.0	–	–	µs
"Low" setup time	ts	1.0	–	–	µs
"Low" hold time	th	1.0	–	–	µs

●**Application example**

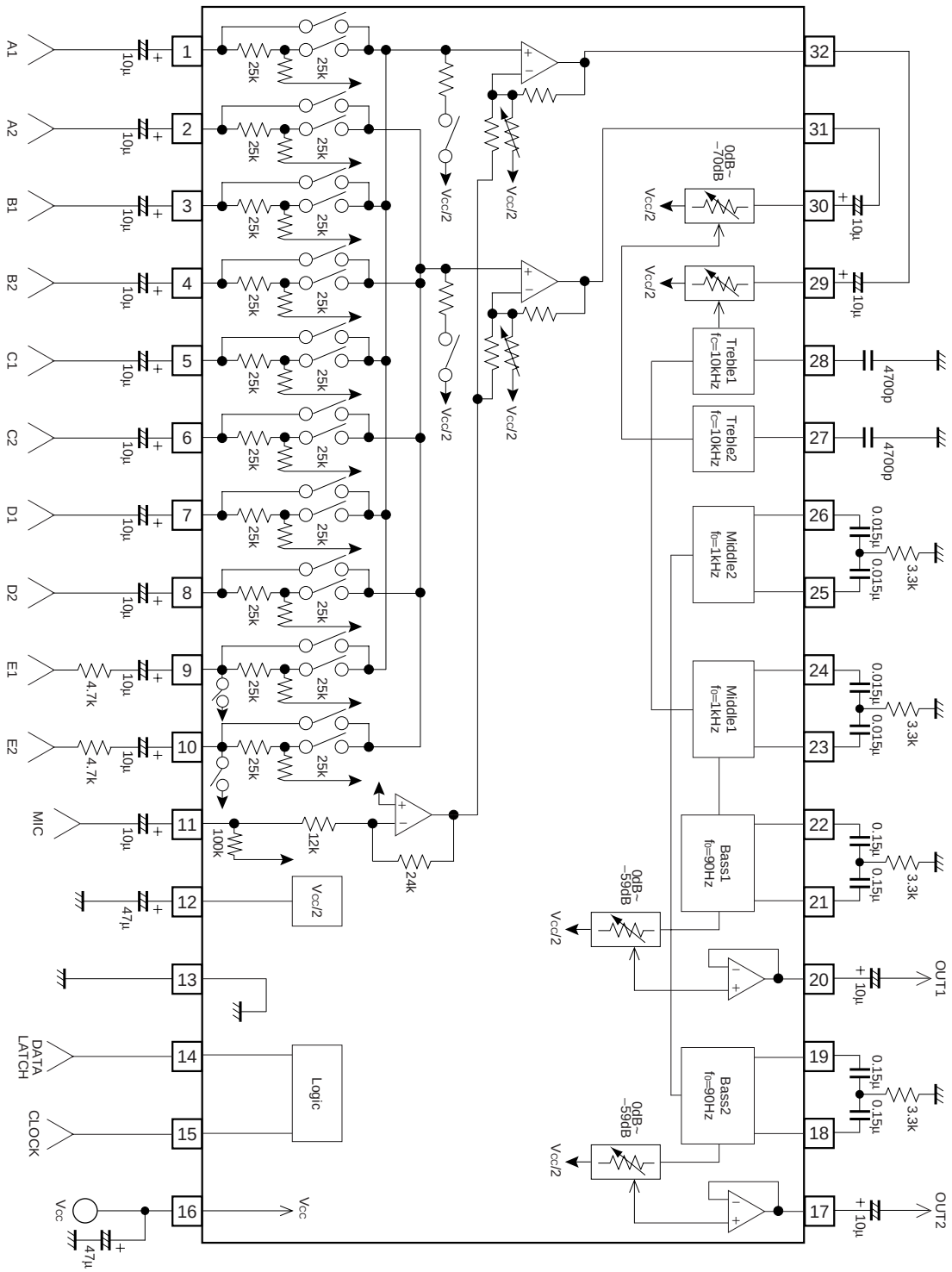


Fig.3

●Operation notes

1. About operation voltage supply range
   Within operation voltage supply range, basic circuit function operation is guaranteed within operation ambient temperature. But please confirm set up of constant and element, voltage set up and temperature set up on use.

2. About operation temperature range
   If it within recommended operation voltage range, circuit function operation is guaranteed within operation temperature. It corralled to conditions of power dissipation to temperature.
   Please watch out except condition stipulated by electrical characteristics within the range, It cannot guarantee standard value of electrical characteristics. But it retains original function.

3. About Application circuit
   Example of application circuit drawing is convinced as recommendable, but please confirm characteristic including above-mentioned notes. At use with modification of external constant, please decide with enough margin considering distribution of this IC, external parts including quiescence characteristics and excessive characteristics. Please note that we have not yet confirmed any concerned patent rights completely.

4. Power-on reset
   Any circuit to perform initialization in the IC upon power on is not contained. Therefore, be sure to send initial data to all the addresses upon power on. Moreover, be sure to mute the set side until the initial data has been sent. For data setting at the second time or later, necessary address only can be modified.

5. Schmidt circuit
   This IC has the Schmidt circuit as preventive measures against logic signal input into the DATA (14pin) and CLK (15pin) terminals. Therefore, this IC is not affected so much by noise to a logic signal line. For the “High” voltage for logic control, voltage in a range from 2.6 to 5.5V is available.

6. Setting of input gain
   Because of the S/N characteristics, it is recommendable to turn ON 6dBSW in input gain in a range between 6 and 20dB (in 2dB increment).

7. Input pin E1 (9pin) and E2 (10pin)
   Input pin E1 (9pin) and E2 (10pin) has a built-in mute circuit. It is the optimal for the auxiliary input.

8. Microphone terminal
   If the microphone terminal (11pin) is not used, use this IC in “open” because of the S/N characteristics.

9. Serial control
   Wire the CLK terminal and DATA terminal taking care not to interfere with an analog signal line.

●**Electrical characteristic curves**

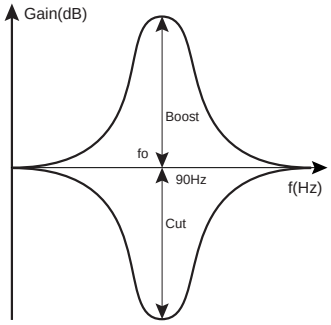


Fig.4 Tone control (Bass)

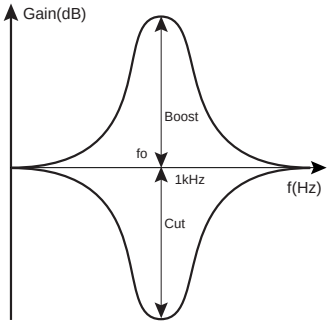


Fig.5 Tone control (Middle)

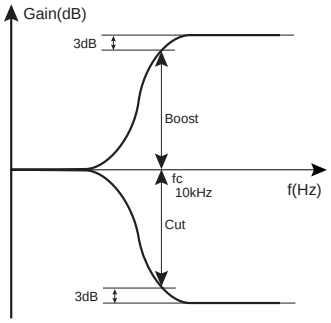
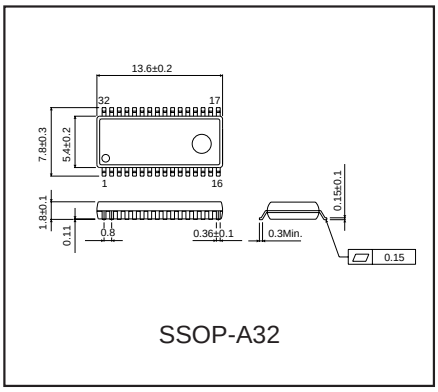


Fig.6 Tone control (Treble)

●**External dimensions** (Unit : mm)



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