

DM54LS461/DM74LS461 Octal Counter

General Description

The LS461 is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (I_0, I_1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0) . The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCRE-MENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CI} = LOW$), otherwise the operation is a HOLD. The carry-out (\overline{CO}) is TRUE ($\overline{CO} = LOW$) when the output register (Q_7-Q_0) is all HIGHs, otherwise FALSE ($\overline{CO} = HIGH$).

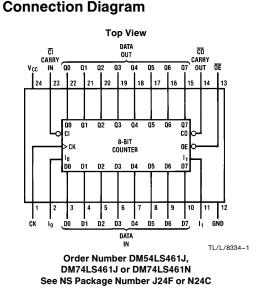
The output register (Q_7-Q_0) is enabled when \overline{OE} is LOW, and disabled (HI-Z) when \overline{OE} is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

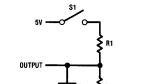
Two or more LS461 octal counters may be cascaded to provide larger counters. The operation codes were chosen such that when I_1 is HIGH, I_0 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

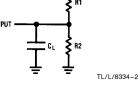
Features/Benefits

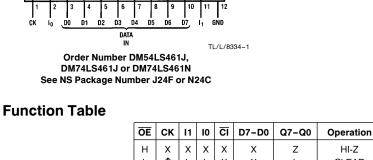
- Octal counter for microprogram-counter, DMA controller and general purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin Skinny Dip saves space
- TRI-STATE® outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Standard Test Load









Н	х	х	х	х	х	Z	HI-Z
L	↑	L	L	X	Х	L	CLEAR
L	↑	L	н	X	Х	Q	HOLD
L	↑	н	L	X	D	D	LOAD
L	↑	н	н	н	Х	Q	HOLD
L	1	Н	Н	L	Х	Q plus 1	INCREMENT

TRI-STATE® is a registered trademark of National Semiconductor Corp.

© 1995 National Semiconductor Corporation TL/L/8334

RRD-B30M115/Printed in U. S. A.

July 1989

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage V_{CC} 7V

Off-State Output Voltage Storage Temperature 5.5V -65°C to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Units	
Symbol	Falameter	Min	Тур	Max	Min	Тур	Max	Units	
V _{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T _A	Operating Free-Air Temperature		-55		125*	0		75	°C
tw	Width of Clock		40			35			ns
۲W	Width of Olock	High	30			25			115
t _{SU}	Set Up Time		60			50			ns
t _h	Hold Time		0	-15		0	-15		113

5.5V

*Case Temperature

Input Voltage

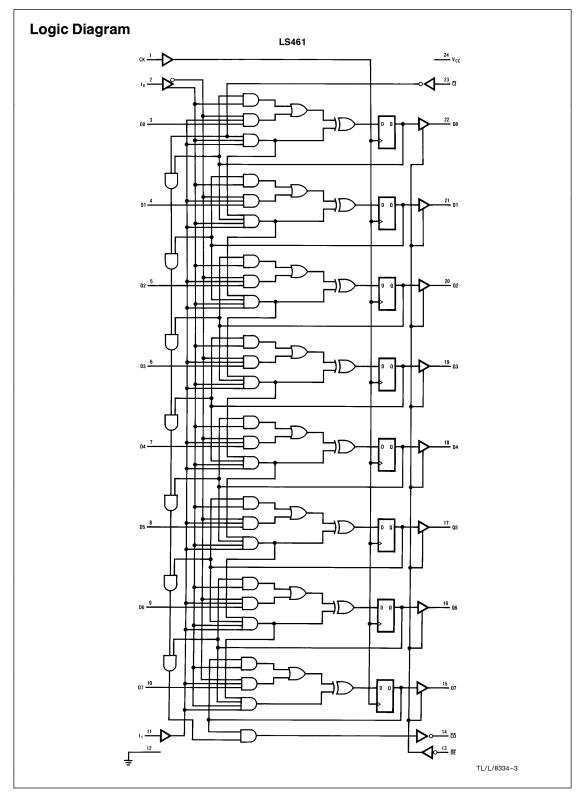
Electrical Characteristics Over Operating Conditions

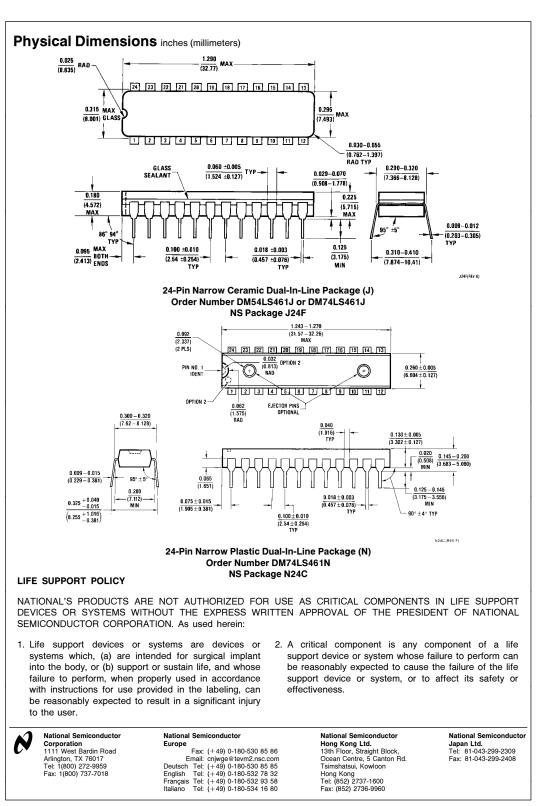
Symbol	Parameter		Test Conditio	ns	Min	Тур†	Max	Units
VIL	Low-Level Input Voltage						0.8	V
VIH	High-Level Input Voltage				2			V
VIC	Input Clamp Voltage	$V_{CC} = MIN$	$I_{I} = -18 \text{ mA}$				-1.5	V
Ι _{ΙL}	Low-Level Input Current	$V_{CC} = MAX$	$V_l = 0.4V$				-0.25	mA
I _{IH}	High-Level Input Current	V _{CC} =MAX	$V_1 = 2.4V$				25	μA
lj –	Maximum Input Current	V _{CC} =MAX	V _I =5.5V				1	mA
V _{OL}	Low-Level Output Voltage	$V_{CC} = MIN$ $V_{IL} = 0.8V$	MIL	I _{OL} =12 mA			0.5	v
		V _{IH} =2V	СОМ	I _{OL} =24 mA				
V _{OH}	High-Level Output Voltage	$V_{CC} = MIN$ $V_{IL} = 0.8V$	MIL	$I_{OH} = -2 \text{ mA}$	2.4			v
		V _{IH} =2V	СОМ	$I_{OH} = -3.2 \text{ mA}$				
I _{OZL}	Off-State Output Current	$V_{CC} = MAX$ $V_{IL} = 0.8V$		V _O =0.4V			- 100	μΑ
I _{OZH}		$V_{IH} = 2V$		V _O =2.4V			100	μΑ
I _{OS}	Output Short-Circuit Current*	V _{CC} =5.0V		$V_{CC} = 0V$	-30		- 130	mA
ICC	Supply Current	V _{CC} =MAX				120	180	mA

*No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second $\dot{\uparrow}$ All typical values are at V_{CC}=5V, T_A=25°C.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Military			Commercial			Units
Symbol	Farameter	(See Test Load)	Min	Тур	Мах	Min	Тур	Max	Units
f _{MAX}	Maximum Clock Frequency		10.5			12.5			MHz
t _{PD}	CBI to CBO Delay	$C_L = 50 \text{ pF}$ R ₁ = 200 Ω R ₂ = 390 Ω		35	60		35	50	ns
t _{PD}	Clock to Q			20	35		20	30	ns
t _{PD}	Clock to CO			55	95		55	80	ns
t _{PZX}	Output Enable Delay	112-000 12		35	55		35	45	ns
t _{PXZ}	Output Disable Delay			35	55		35	45	ns





National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.