National Semiconductor

May 2007

DS16EV5110
Video Equalizer for DVI, HDMI, and CAT5 Cables

General Description

The DS16EV5110 is a 2.25 Gbps multi-channel equalizer optimized for video cable extension applications. It contains three transition-minimized differential signaling (TMDS) data channels and one clock channel as commonly found in DVI and HDMI cables. It provides compensation for skin-effect and dielectric losses, a common phenomenon when transmitting video on commercially available high definition video cables.

The inputs and outputs fully support DVI and HDMI requirements and features programmable levels of input equalization. This provides optimal signal boost and reduces intersymbol interference. The device supports DC-coupled data paths providing a wider input common-mode voltage range. This eliminates the need for external coupling capacitors, thereby reducing solution size and cost.

The clock channel is optimized for clock rates of up to 225 MHz and features a signal detect circuit. To maximize noise immunity, the DS16EV5110 features a programmable loss of signal threshold. The threshold is adjustable through a Serial Management Bus (SMBus) interface.

The DS16EV5110 also provides support for system power management via output enable controls. Additional controls are provided via the SMBus enabling customization and optimization for specific applications requirements. These include programmable features such as output amplitude and boost control as well as system level diagnostics.

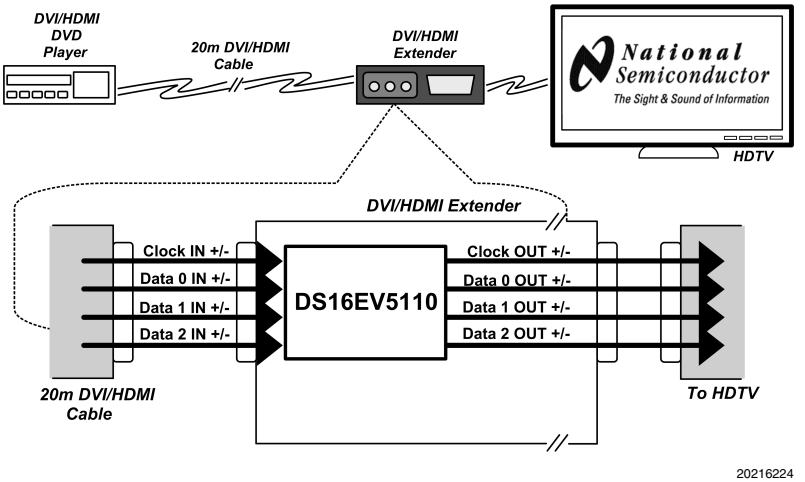
Features

- 8 levels of equalization settable by 3 pins or through the SMBus interface
- DC-Coupled inputs and outputs
- Optimized for operation from 250 Mbps to 2.25 Gbps in support of UXGA, 480 I/P, 720 I/P, 1080 I, and 1080 P with 8, 10, and 12–bit Color Depth Resolutions
- Two DS16EV5110 devices support DVI/HDMI Dual Link
- DVI 1.0, HDMI 1.2a, and HDMI 1.3 Compatible TMDS Interface
- Clock channel signal detect (LOS)
- Enable for power savings standby mode
- Serial Management Bus (SMBus) provides control of boost, output amplitude, enable, and clock channel signal detect threshold
- Low power consumption: 475mW (Typical)
- 0.13 UI total jitter at 1.65 Gbps including cable
- Single 3.3V power supply
- Small 7mm x 7mm, 48-pin leadless LLP package
- -40°C to +85°C operating temperature range
- Extends TMDS cable reach over:
  1. > 40 meters 24 AWG DVI Cable
  2. > 20 meters 28 AWG DVI Cable
  3. > 20 meters Cat5/Cat5e/Cat6 cables
  4. > 20 meters at 2.25 Gbps over 28 AWG HDMI cables

Applications

- DVI/HDMI Cable Extenders / Switchers
- Digital Routers and Switches
- Projectors
- High Definition Displays

Typical Application



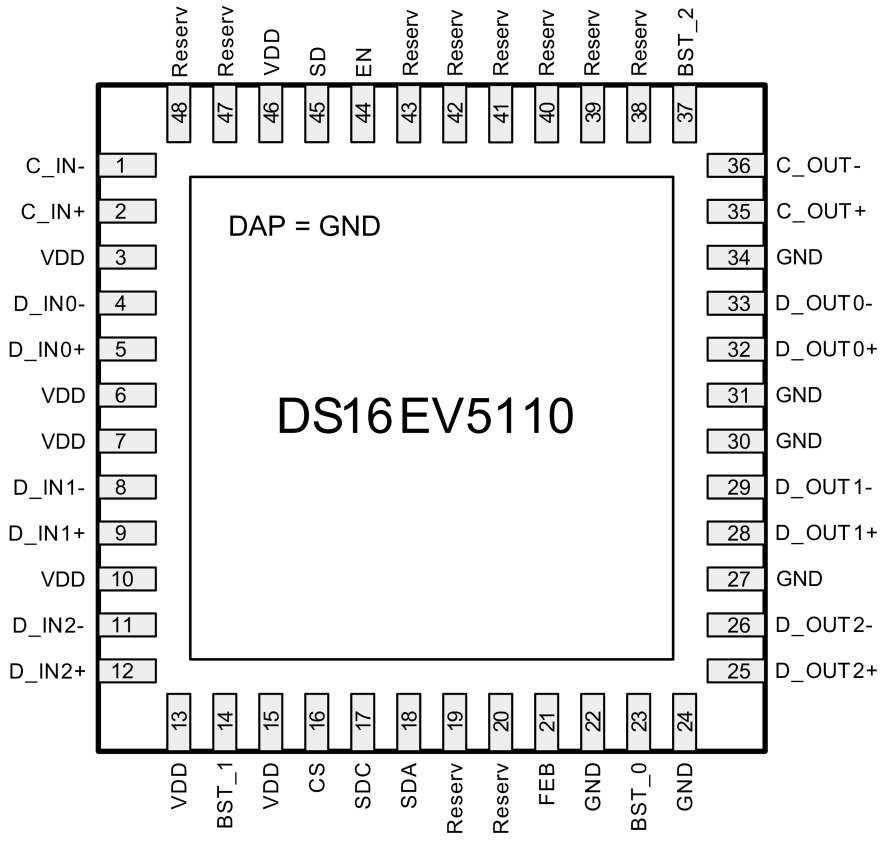
20216224

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
C_IN– C_IN+	1 2	I, CML	Inverting and non-inverting TMDS Clock inputs to the equalizer. An on-chip 50Ω terminating resistor connects C_IN+ to VDD and C_IN- to VDD.
D_IN0– D_IN0+	4 5	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN0+ to VDD and D_IN0- to VDD.
D_IN1– D_IN1+	8 9	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN1+ to VDD and D_IN1- to VDD.
D_IN2– D_IN2+	11 12	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN2+ to VDD and D_IN2- to VDD.
C_OUT- C_OUT+	36 35	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT0– D_OUT0+	33 32	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT1– D_OUT1+	29 28	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT2– D_OUT2+	26 25	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
Equalization Control			
BST_0 BST_1 BST_2	23 14 37	I, CMOS	BST_0, BST_1, and BST_2 select the equalizer boost level for EQ channels. BST_0, BST_1, and BST_2 are internally pulled low.
Device Control			
EN	44	I, CMOS	Enable Equalizer inputs. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled high.
FEB	21	I, CMOS	Force External Boost. When held high, the equalizer boost setting is controlled by the BST_[0:2] pins. When held low, the equalizer boost level is controlled through the SMBus (see *Table 1*) control pins. FEB is internally pulled high.
SD	45	O, CMOS	Equalizer Clock Channel Signal Detect Output. Produces a high when signal is detected.
POWER			
V_{DD}	3, 6, 7, 10, 13, 15, 46	I, Power	V_{DD} pins should be tied to the V_{DD} plane through a low inductance path. A 0.01µF bypass capacitor should be connected between each V_{DD} pin to the GND planes.
GND	22, 24, 27, 30, 31, 34	I, Power	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	PAD	I, Power	The exposed pad at the center of the package must be connected to the ground plane.
Serial Management Bus (SMBus) Interface Control Pins			
SDA SDC CS	18 17 16	I, CMOS I, CMOS I, CMOS	Data Input. Internally pulled high. Clock Input. Internally pulled high. Chip select. When held high, the equalizer SMBus register is enabled. When held low, the equalizer SMBus register is disabled. CS is internally pulled low. CS is internally gated with SDC.
Other			
Reserv	19, 20, 38, 39, 40,41, 42, 43, 47, 48		Reserved. Do not connect.

Note: I = Input O = Output

Connection Diagram



20216226

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +4.2V
CMOS Input Voltage	−0.5V to (V_{DD} + 0.5V)
CMOS Output Voltage	−0.5V to (V_{DD} + 0.5V)
CML Input/Output Voltage	-0.3V to (V_{DD} + 0.3V)
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temp. (Soldering, 5 sec.)	+260°C
ESD Rating	
HBM, 1.5 kΩ, 100 pF	>8 kV
CML Inputs	>10 kV
Thermal Resistance	
θ_{JA}, No Airflow	30°C/W

Recommended Operating Conditions (Notes 2, 3)

	Min	Typ	Max	Units
Supply Voltage (V_{DD} to GND)	3.0	3.3	3.6	V
Ambient Temperature	−40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
I_{IH-PU}	High Level Input Leakage Current	CMOS pins with internal pull-up resistors	—10		+10	µA
I_{IH-PD}	High Level Input Leakage Current	CMOS pins with internal pull-down resistors	80		105	µA
I_{IL-PU}	Low Level Input Leakage Current	CMOS pins with internal pull-up resistors	—20		—10	µA
I_{IL-PD}	Low Level Input Leakage Current	CMOS pins with internal pull-down resistors	—10		+10	µA
V_{IH}	High Level Input Voltage		2.0		VDD	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{OH}	High Level Output Voltage	SD Pin	2.4			V
V_{OL}	Low Level Output Voltage	SD Pin			0.4	V
POWER						
P	Power Supply Consumption	EN = High, Device Enabled		475	700	mW
		EN = Low, Power Down Mode			70	mW
N	Supply Noise Tolerance (Note 4)	50 Hz – 100 Hz 100 Hz – 10 MHz 10 MHz – 825 MHz		100 40 10		mV_{P-P} mV_{P-P} mV_{P-P}
CML INPUTS						
V_{IN}	Input Voltage Swing	Measured differentially at TPA (*Figure 1*)	800		1200	mV_{P-P}
V_{ICMDC}	Input Common-Mode Voltage	DC-Coupled Requirement Measured at TPB (*Figure 1*)	V_{DD}-0.3		V_{DD}-0.2	V
R_{LI}	Differential Input Return Loss	100 MHz– 825 MHz, with fixture's effect de-embedded		10		dB
R_{IN}	Input Resistance	IN+ to VDD and IN– to VDD	45	50	55	Ω
CML OUTPUTS						
V_O	Output Voltage Swing	Measured differentially with OUT+ and OUT– terminated by 50Ω to VDD	800		1200	mV_{P-P}
V_{OCM}	Output common-mode Voltage	Measured Single-ended	V_{DD}-0.3		V_{DD}-0.2	V
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins.	75		240	ps
t_{CCSK}	Inter Pair Channel-to-Channel Skew (all 4 Channels)	Difference in 50% crossing between shortest and longest channels		25		ps

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_D	Latency			350		ps
OUTPUT JITTER						
TJ1	Total Jitter at 1.65 Gbps	20m 28 AWG STP DVI Cable Data Paths EQ Setting 0x04 PRBS7 (Notes 5, 6, 7)		0.13	0.17	UI_{P-P}
TJ2	Total Jitter at 2.25 Gbps	20m 28 AWG STP DVI Cable Data Paths EQ Setting 0x04 PRBS7 (Notes 5, 6, 7)		0.2		UI_{P-P}
TJ3	Total Jitter at 165 MHz	Clock Paths Clock Pattern (Notes 5, 6, 7)			0.165	UI_{P-P}
TJ4	Total Jitter at 225 MHz	Clock Paths Clock Pattern (Notes 5, 6, 7)		0.165		UI_{P-P}
RJ	Random Jitter	(Notes 7, 8)		3		psrms
BIT RATE						
F_{CLK}	Clock Frequency	Clock Path (Note 5)	25		225	MHz
BR	Bit Rate	Data Path (Note 5)	0.25		2.25	Gbps

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: Typical values represent most likely parametric norms at V_{DD} = 3.3V, T_A = 25°C., and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

Note 3: The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 4: Allowed supply noise (mV_{P-P} sine wave) under typical conditions.

Note 5: Specification is guaranteed by characterization and is not tested in production.

Note 6: Deterministic jitter is measured at the differential outputs (TPC of *Figure 1*), minus the deterministic jitter before the test channel (TPA of *Figure 1*). Random jitter is removed through the use of averaging or similar means.

Note 7: Total Jitter is defined as peak-to-peak deterministic jitter from (Note 8) + 14.2 times random jitter.

Note 8: Random jitter contributed by the equalizer is defined as sq rt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see TPC of *Figure 1*; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see TPA of *Figure 1*.

Electrical Characteristics — Serial Management Bus Interface (Notes 2, 3)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Serial Bus Interface — DC Specifications						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.8		V_{DD}	V
I_{PULLUP}	Current through pull-up resistor or current source	VOL = 0.4V		10		mA
V_{DD}	Nominal Bus Voltage		3.0		3.6	V
$I_{LEAK-Bus}$	Input Leakage per bus segment	(Note 9)	—200		+200	µA
$I_{LEAK-Pin}$	Input Leakage per device pin			—15		µA
C_I	Capacitance for SDA and SDC	(Notes 9, 10)			10	pF
R_{TERM}	Termination Resistance	$V_{DD3.3}$ (Notes 9, 10, 11)		2000		Ω
		$V_{DD2.5}$ (Notes 9, 10, 11)		1000		Ω
Serial Bus Interface Timing Specification						
FSMB	Bus Operating Frequency	(Note 12)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold Time After (Repeated) Start Condition. First CLK generated after this period.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	(Note 12)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	(Note 12)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	(Note 12)			2	ms
t_F	Clock/Data Fall Time	(Note 12)			300	ns
t_R	Clock/Data Rise Time	(Note 12)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	(Note 12)			500	ms

Note 9: Recommended value. Parameter not tested in production.

Note 10: Recommended maximum capacitance load per bus segment is 400pF.

Note 11: Maximum termination voltage should be identical to the device supply voltage.

Note 12: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Serial Management Bus (SMBus) Configuration Registers

The Serial Management Bus interface is compatible to SMBus 2.0 physical layer specification, except for bus termination voltages. Holding the CS pin high enables the SMBus port allowing access to the SMBus registers. The configuration registers can be read and written using SMBus through the SDA and SDC pins. In the STANDBY state, the Serial Management Bus remains active. Please see *Table 1* for more information.

TABLE 1. SMBus Register Address

Name	Address	Default	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	0x00	0x00	RO	ID Revision				Reserved	Reserved	Reserved	SD
Status	0x01	0x00	RO	Reserved	Boost 1			EN	Reserved		
Status	0x02	0x00	RO	Reserved	Boost 3			Reserved	Boost 2		
Internal Enable/ Individual Channel Boost Control for C_IN±, D_IN0±	0x03	0x77	RW	EN (Int.) 0:Enable 1:Disable (D_IN0±)	Boost Control (BC for CH0) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)			EN (Int.) 0:Enable 1:Disable (C_IN±)	Reserved		
Individual Channel Boost Control for D_IN1±, D_IN2±	0x04	0x77	RW	EN (Int.) 0:Enable 1:Disable (D_IN2±)	Boost Control (BC for CH2) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)			EN (Int.) 0:Enable 1:Disable (D_IN1±)	Boost Control (BC for CH1) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)		
Signal Detect ON (SD_ON)	0x05	0x00	RW	Reserved						Threshold (mV) 00: 70 (Default) 01: 55 10: 90 11: 75	
Signal Detect OFF (SD_OFF)	0x06	0x00	RW	Reserved						Threshold (mV) 00: 40 (Default) 01: 30 10: 55 11: 45	
SMBus or CMOS Control for EN	0x07	0x00	RW	Reserved							SMBus Enable 0: Disable 1: Enable
Output Level	0x08	0x78	RW	Reserved				Output Level: 00: 540 mVp-p 01: 770 mVp-p 10: 1000 mVp-p 11: 1200 mVp-p		Reserved	

Note: RO = Read Only, RW = Read/Write

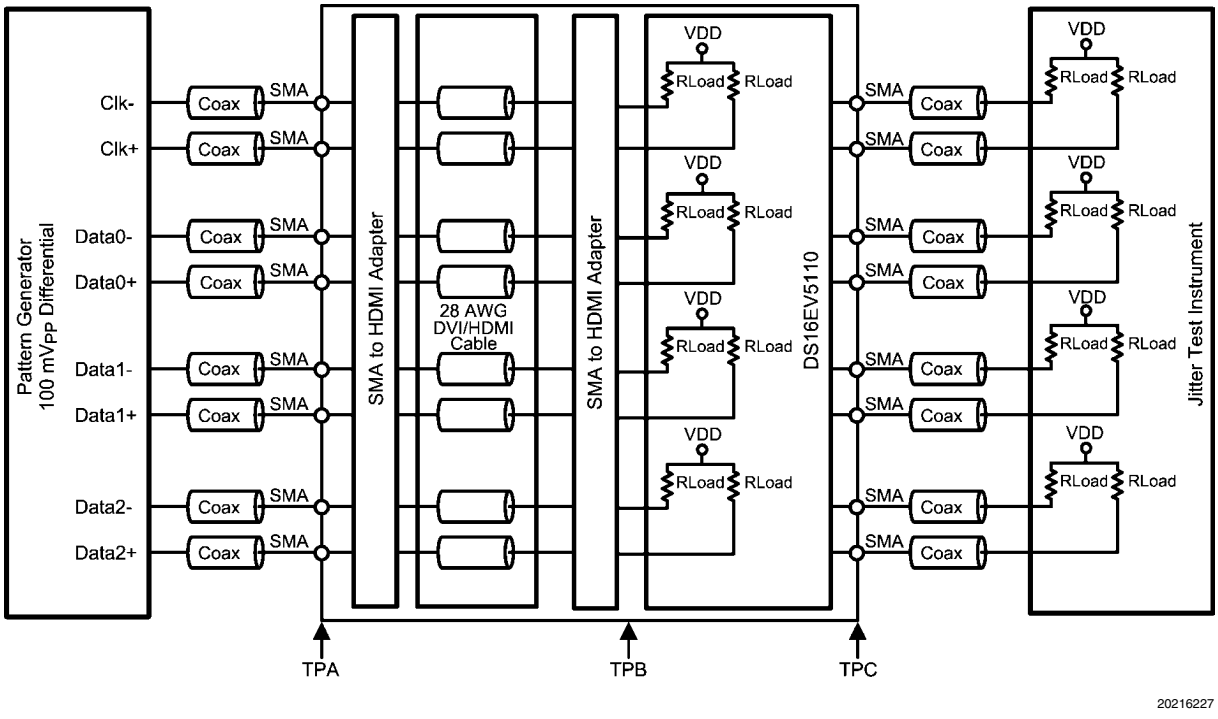


FIGURE 1. Test Setup Diagram

DS16EV5110 Device Description

The DS16EV5110 video equalizer comprises three data channels, a clock channel, and a control interface including a Serial Management Bus (SMBus) port.

DATA CHANNELS

The DS16EV5110 provides three data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a TMDS driver as shown in *Figure 2*.

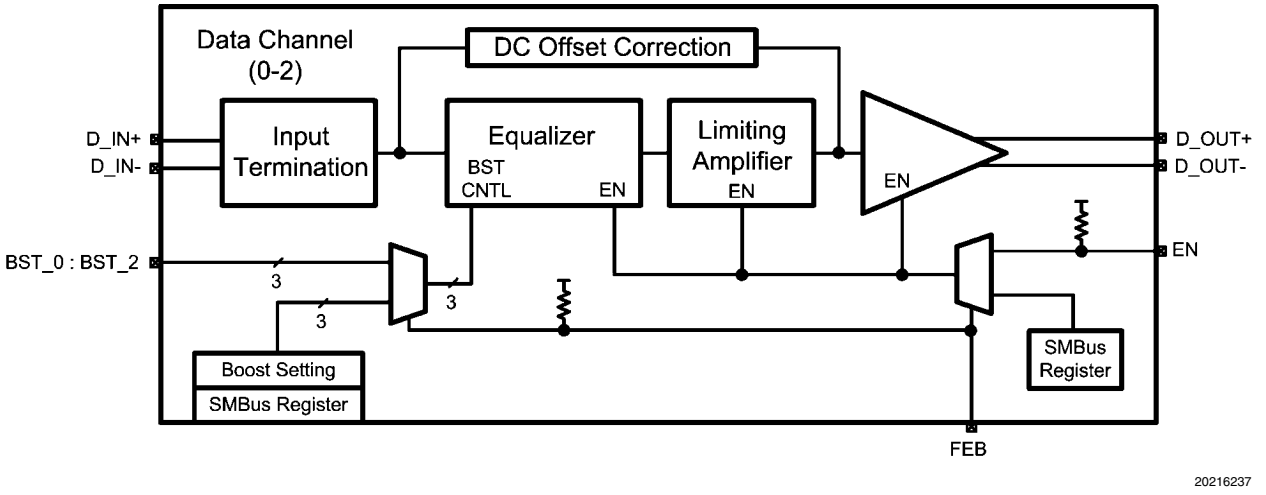


FIGURE 2. DS16EV5110 Data Channel

EQUALIZER BOOST CONTROL

The data channel equalizers support eight programmable levels of equalization boost. The state of the FEB pin determines how the boost settings are controlled. If the FEB pin is held high, then the equalizer boost setting is controlled by the Boost Set pins (BST_[0:2]) in accordance with *Table 2*. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all three data channels. When the FEB pin is held low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see *Table 1*). Using this approach, equalizer boost settings can be programmed for each channel individually. FEB is internally pulled high (default setting); therefore if left unconnected, the boost settings are controlled by the Boost Set pins (BST_[0:2]). The range of boost settings provided enables the DS16EV5110 to address a wide range of transmission line path loss scenarios, enabling support for a variety of data rates and formats.

TABLE 2. EQ Boost Control Table

Control Via SMBus BC_2, BC_1, BC_0 (FEB = 0)	**Control Via Pins** BST_2, BST_1, BST_0 (FEB = 1)	**EQ Boost Setting at 825 MHz (dB)**
000	000	9
001	001	14
010	010	18
011	011	21
100	100	24
101	101	26
110	110	28
111	111	30

DEVICE STATE AND ENABLE CONTROL

The DS16EV5110 has an Enable feature which provides the ability to control device power consumption. This feature can be controlled either via the Enable Pin (EN Pin) or via the Enable Control Bit which is accessed through the SMBus port (see *Table 1* and *Table 3*). If Enable is activated, the data channels and clock channel are placed in the ACTIVE state and all device blocks function as described. The DS16EV5110 can also be placed in STANDBY mode to save power. In this mode only the control interface including the SMBus port as well as the clock channel signal detection circuit remain active.

TABLE 3. Enable and Device State Control

Register 07[0] (SMBus)	EN Pin (CMOS)	Register 03[3] (EN Control) (SMBus)	Device State
0 : Disable	1	X	ACTIVE
0 : Disable	0	X	STANDBY
1 : Enable	X	0	ACTIVE
1 : Enable	X	1	STANDBY

CLOCK CHANNEL

The clock channel incorporates a limiting amplifier, a DC offset correction, and a TMDS driver (*Figure 3*).

CLOCK CHANNEL SIGNAL DETECT

The DS16EV5110 features a signal detect circuit on the clock channel. The status of the clock signal can be determined by either reading the Signal Detect bit (SD) in the SMBus registers (see *Table 1*) or by the state of the SD pin. A logical high indicates the presence of a signal that has exceeded a specified maximum threshold value (called SD_ON). A logical low means that the clock signal has fallen below a minimum threshold value (called SD_OFF). These values are programmed via the SMBus (*Table 1*). If not programmed via the SMBus, the minimum and maximum thresholds take on the default values for the minimum and maximum values as indicated in *Table 4*. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

TABLE 4. Clock Channel Signal Detect Threshold Values

Bit 1	Bit 0	Minimum Threshold Register 06 (mV)	Maximum Threshold Register 05 (mV)
0	0	40 (Default)	70 (Default)
0	1	30	55
1	0	55	90
1	1	45	75

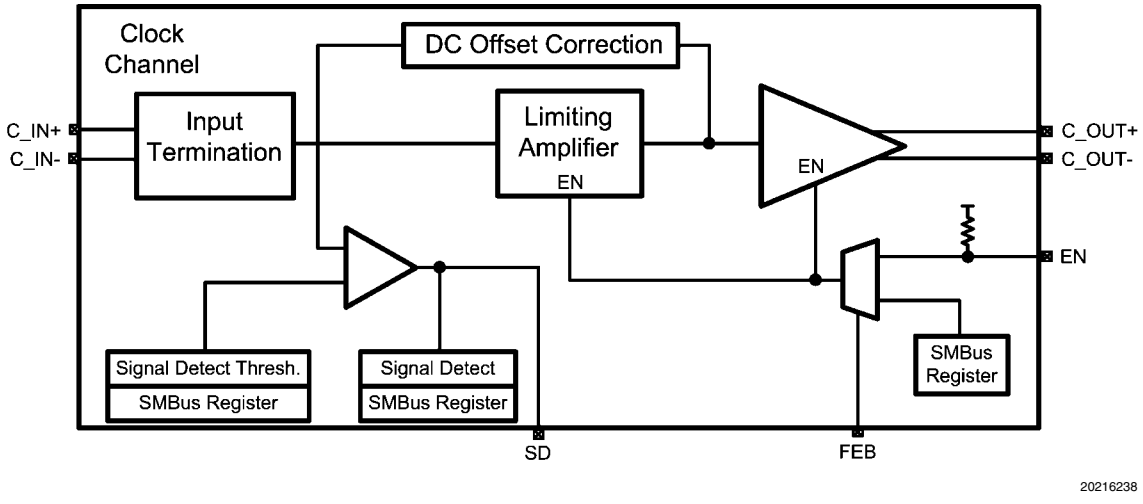


FIGURE 3. DS16EV5110 Clock Channel

OUTPUT LEVEL CONTROL

The output amplitude of the TMDS drivers for both the data channels and the clock channel can be controlled via the SMBus (see *Table 1*). The default output level is 1000mV p-p. The following Table presents the output level values supported:

TABLE 5. Output Level Control Settings

Bit 3	Bit 2	Output Level (mV)
0	0	540
0	1	770
1	0	1000 (default)
1	1	1200

AUTOMATIC ENABLE FEATURE

It may be desired for the DS16EV5110 to be configured to automatically enter STANDBY mode if no clock signal is present. This is implemented by connecting the Signal Detect (SD) pin to the external (CMOS) Enable (EN) pin. In order for this option to function properly, the FEB pin must be either tied high or not connected (the FEB pin is internally pulled high by default). If the clock signal applied to the clock channel input swings above the maximum level specified in the threshold register via the SMBus, then the SD pin is asserted high. If the SD pin is connected to the EN pin, this will enable the equalizer, limiting amplifier, and output buffer on the data channels as well as the limiting amplifier and output buffer on the clock channel (provided that the FEB pin is high); thus the DS16EV5110 will automatically enter the ACTIVE state. If the clock signal present falls below the minimum level specified in the threshold register, then the SD pin will be asserted low, causing the aforementioned blocks to be placed in the STANDBY state.

Application Information

The DS16EV5110 is used to recondition DVI/HDMI video signals or differential signals with similar characteristics after signal loss and degradation due to transmission through a length of shielded or unshielded cable.

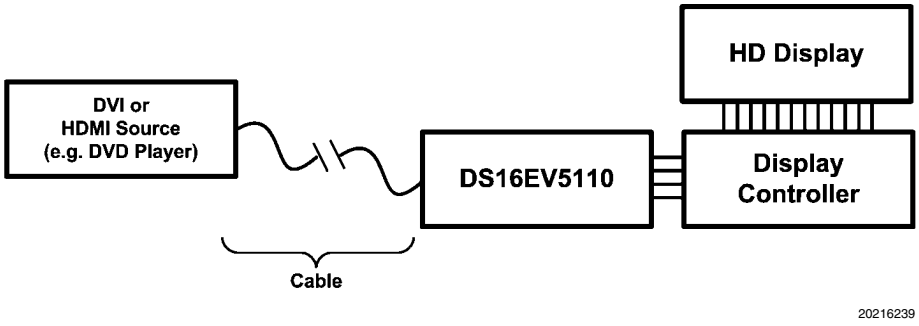


FIGURE 4. DS16EV5110 Typical Use

DVI 1.0 AND HDMI V1.2a APPLICATIONS

A single DS16EV5110 can be used to implement cable extension solutions with various resolutions and screen refresh rates. The range of digital serial rates supported is between 250 Mbps and 1.65 Gbps. For applications requiring ultra-high resolution for DVI applications (e.g., QXGA and WQXGA), a "dual link" TMDS interface is required. This is easily configured by using two DS16EV5110 devices as shown in *Figure 5*.

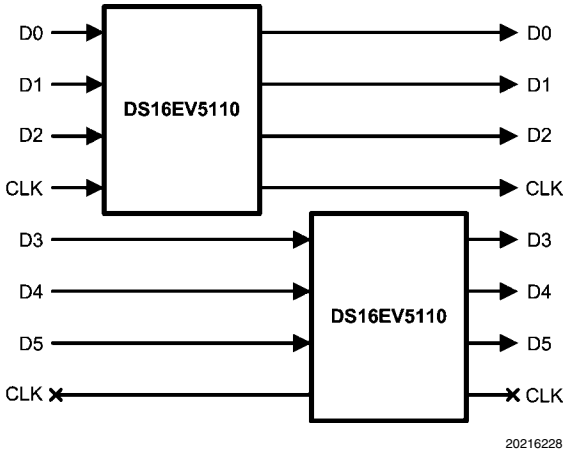


FIGURE 5. Connection in Dual Link Application

HDMI V1.3 APPLICATION

The DS16EV5110 can reliably extend operation to distances greater than 20 meters of 28 AWG HDMI cable at 2.25 Gbps, thereby supporting HDMI v1.3 for 1080p HDTV resolution with 12-bit color depth. Please note that the Electrical Characteristics specified in this document have not been tested for and are not guaranteed for 2.25 Gbps operation.

DC COUPLED DATA PATHS AND DVI/HDMI COMPLIANCE

The DS16EV5110 is designed to support TMDS differential pairs with DC coupled transmission lines. It contains integrated termination resistors (50Ω), pulled up to VCC at the input stage, and open collector outputs for DVI / HDMI compliance.

28 AWG STP DVI / HDMI CABLES RECOMMENDED BOOST SETTINGS

The following table presents the recommended boost control settings for various data rates and cable lengths for 28 AWG DVI/HDMI compliant configurations:

TABLE 6. Boost Control Setting for STP Cables

Setting	Data Rate	28 AWG DVI / HDMI
0x04	750 Mbps	0–25m
0x04	1.65 Gbps	0–20m
0x06	750 Mbps	25m to greater than 30m
0x06	1.65 Gbps	20m to greater than 25m
0x03	2.25 Gbps	0–15m
0x06	2.25 Gbps	15m to greater than 20m

UTP (UNSHIELDED TWIST PAIRS) CABLES

The DS16EV5110 can be used to extend the length of UTP cables, such as CAT5, CAT5e and CAT6 to distances greater than 20 meters at 1.65 Gbps with < 0.13 UI of jitter. Please note that for non-standard DVI/HDMI cables, the user must ensure the clock-to-data channel skew requirements are met. Table 7 presents the recommended boost control settings for various data rates and cable lengths for UTP configurations:

TABLE 7. Boost Control Setting for UTP Cables

Setting	Data Rate	CAT5 Cable
0x03	750 Mbps	0–25m
0x06	750 Mbps	25–45m
0x03	1.65 Gbps	Greater than 20m

CABLE SELECTION

At higher frequencies, longer cable lengths produce greater losses due to the skin effect. The quality of the cable with respect to conductor wire gauge and shielding heavily influences performance. Thicker conductors have lower signal degradation per unit length. In nearly all applications, the DS16EV5110 equalization can be set to 0x04, and equalize up to 22 dB skin effect loss for all input cable configurations at all data rates, without degrading signal integrity.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The TMDS differential inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route TMDS lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the TMDS signals away from other signals and noise sources on the printed circuit board. All traces of TMDS differential inputs and outputs must be equal in length to minimize intra-pair skew.

See AN-1187 for additional information on LLP packages.

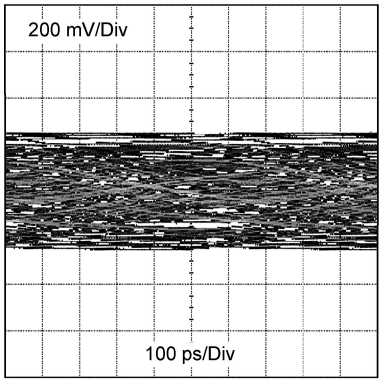
General Recommendations

The DS16EV5110 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips as well as many other available resources available addressing signal integrity design issues.

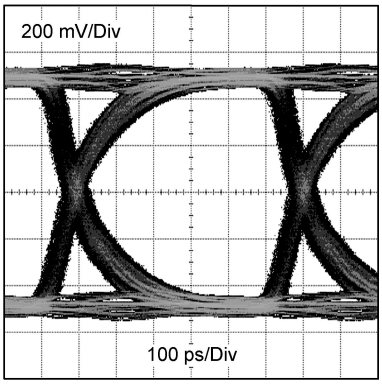
POWER SUPPLY BYPASSING

Two approaches are recommended to insure that the DS16EV5110 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS16EV5110. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2µF to 10µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS16EV5110.

Typical Performance Characteristics

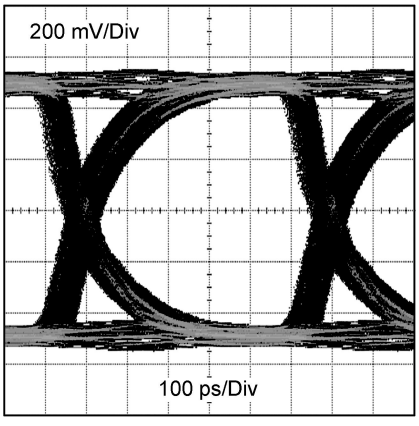


20216229



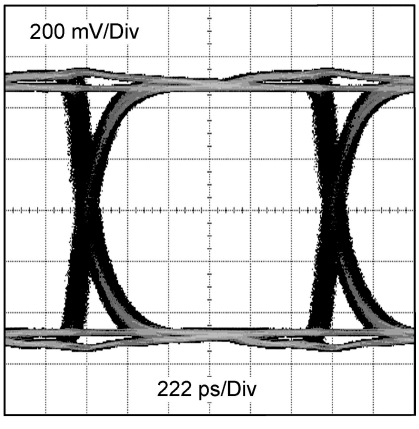
20216230

FIGURE 6. Un-equalized vs. Equalized Signal after 25m of 28 AWG DVI Cable at 1.65 Gbps (0x06 Setting)



20216231

FIGURE 7. Output Signal after 20m of CAT5 Cable at 1.65 Gbps (0x06 Setting)



20216232

FIGURE 8. Output Signal after 30m of 28 AWG DVI Cable at 750 Mbps (0x06 Setting)

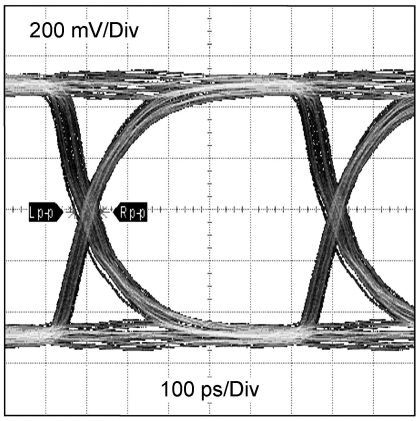


FIGURE 9. Output Signal after 0.3m of 28 AWG DVI Cable at 1.65 Gbps (0x04 Setting)

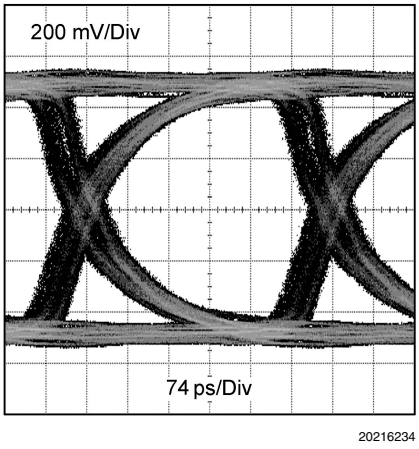


FIGURE 10. Output Signal after 20m of 28 AWG HDMI Cable at 2.25 Gbps (0x06 Setting)

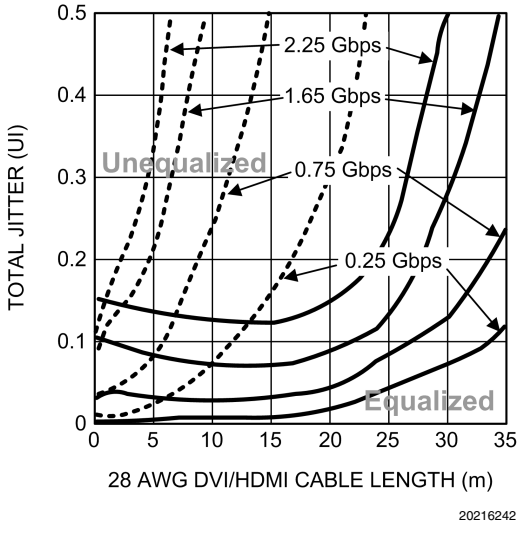


FIGURE 11. Equalized vs. Unequalized Jitter Performance Over 28 AWG DVI/HDMI Cable

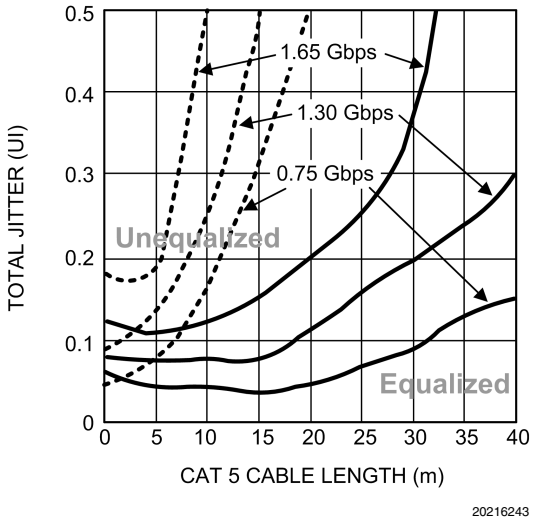


FIGURE 12. Equalized vs. Unequalized Jitter Performance Over CAT5 Cable

Equivalent I/O Structures

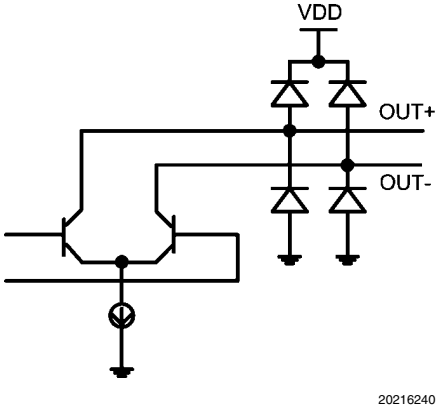


FIGURE 13. Equivalent Output Structure

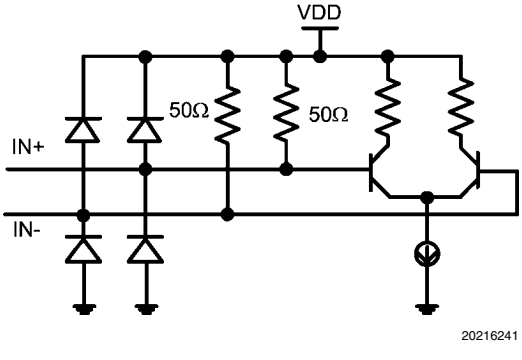
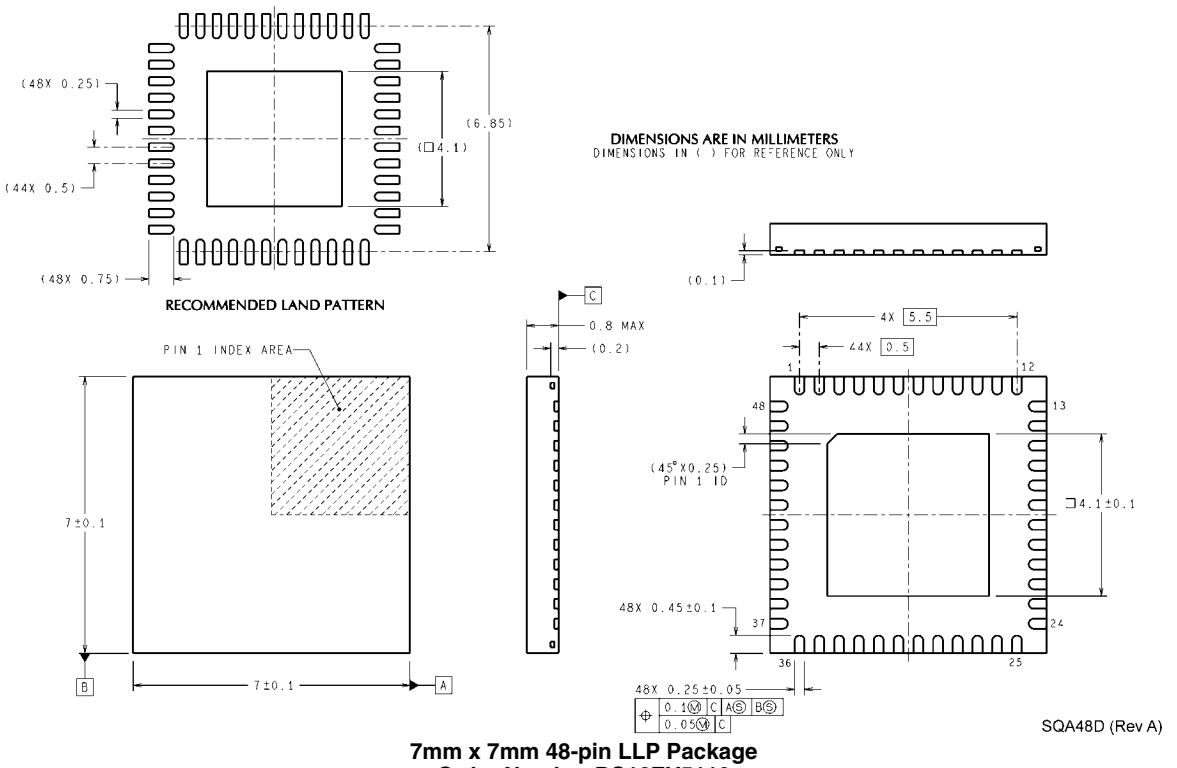


FIGURE 14. Equivalent Input Structure

Physical Dimensions inches (millimeters) unless otherwise noted



7mm x 7mm 48-pin LLP Package
Order Number DS16EV5110
Package Number SQA48D

To order lead-free products, call your National Semiconductor distributors. They can order products for you with an "NOPB" specification. For more information on our Lead-free program, please check out our Lead-Free Status page.

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560