FAIRCHILD SEMICONDUCTOR TM

April 1999

FDN335N

N-Channel 2.5V Specified PowerTrench™ MOSFET

General Description

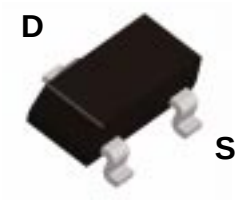
This N-Channel 2.5V specified MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

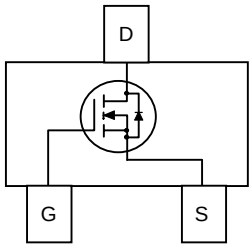
- DC/DC converter
- Load switch

Features

- 1.7 A, 20 V. $R_{DS(ON)}$ = 0.07 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.100 Ω @ V_{GS} = 2.5 V.
- Low gate charge (3.5nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



SuperSOT™-3



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1a)	1.7	A
	- Pulsed		8	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
335	FDN335N	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.4	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		-3		mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 1.7 A V_{GS} = 4.5 V, I_D = 1.7 A,T_J = 125°C V_{GS} = 2.5 V, I_D = 1.5 A		0.055 0.079 0.078	0.070 0.120 0.100	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	8			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.5 A		7		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		310		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		5	15	ns
t_r	Turn-On Rise Time			8.5	17	ns
$t_{d(off)}$	Turn-Off Delay Time			11	20	ns
t_f	Turn-Off Fall Time			3	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.7 A, V_{GS} = 4.5 V,		3.5	5	nC
Q_{gs}	Gate-Source Charge			0.55		nC
Q_{gd}	Gate-Drain Charge			0.95		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)		0.7	1.2	V

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 in² Pad of 2 oz. Cu.

b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2: Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

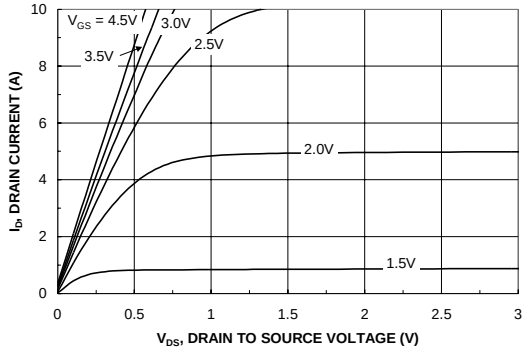


Figure 1. On-Region Characteristics.

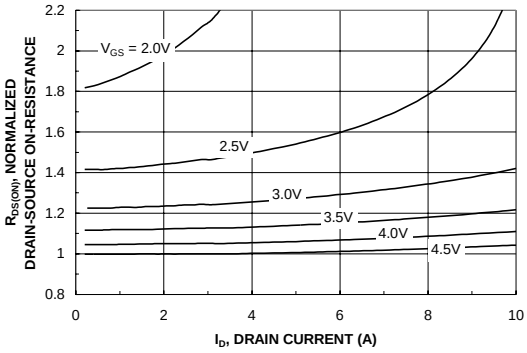


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

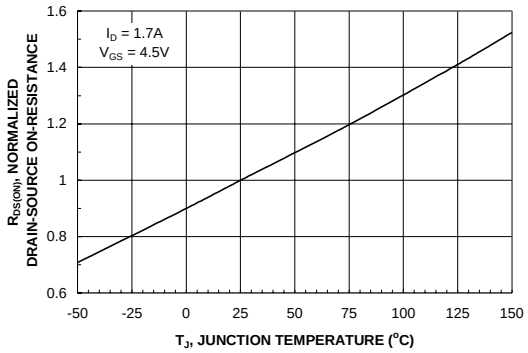


Figure 3. On-Resistance Variation with Temperature.

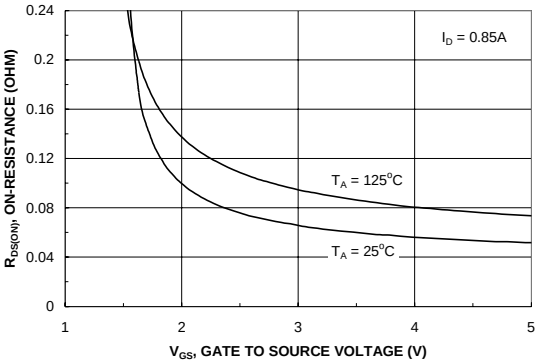


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

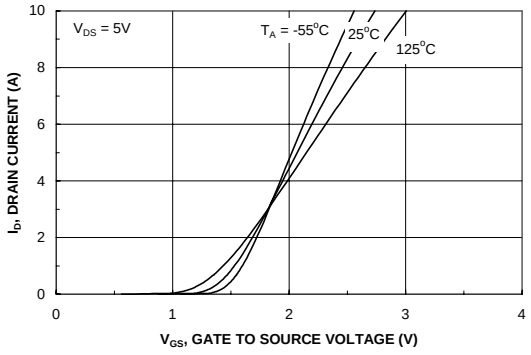


Figure 5. Transfer Characteristics.

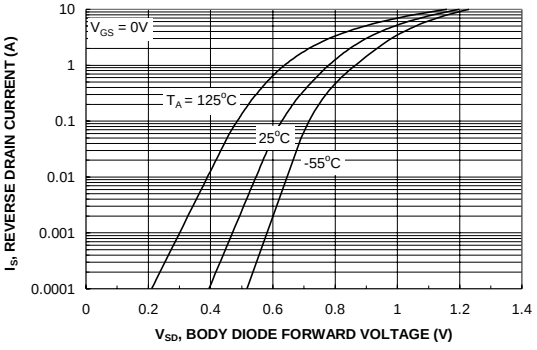


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

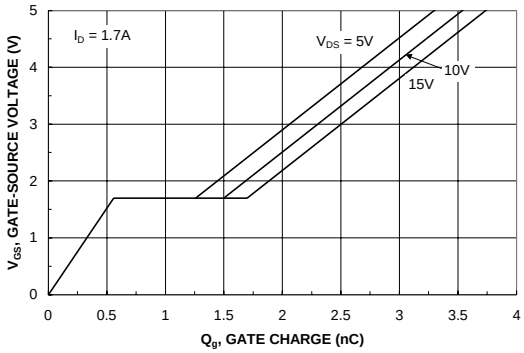


Figure 7. Gate Charge Characteristics.

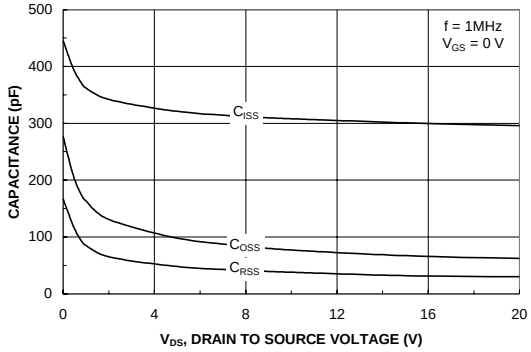


Figure 8. Capacitance Characteristics.

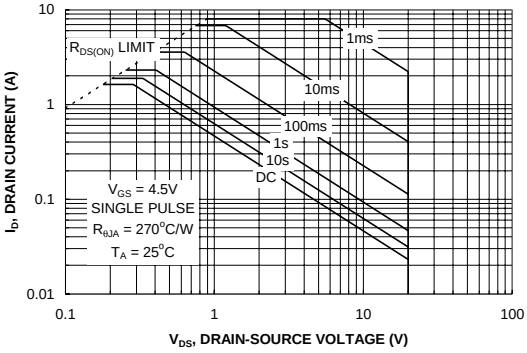


Figure 9. Maximum Safe Operating Area.

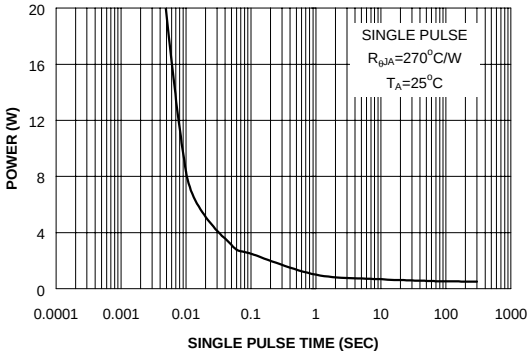


Figure 10. Single Pulse Maximum Power Dissipation.

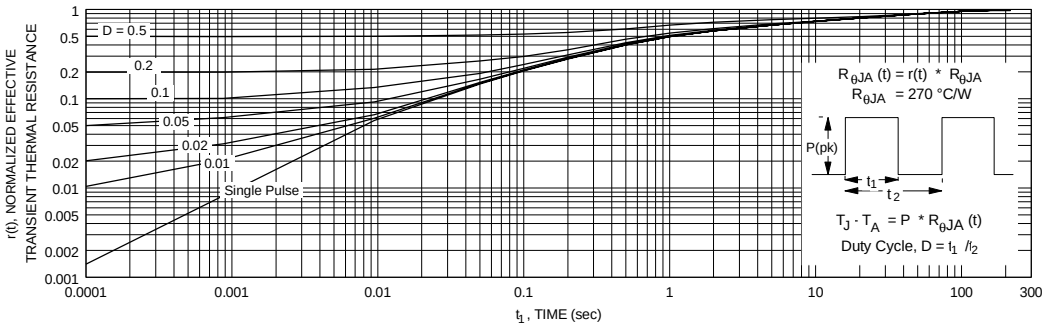
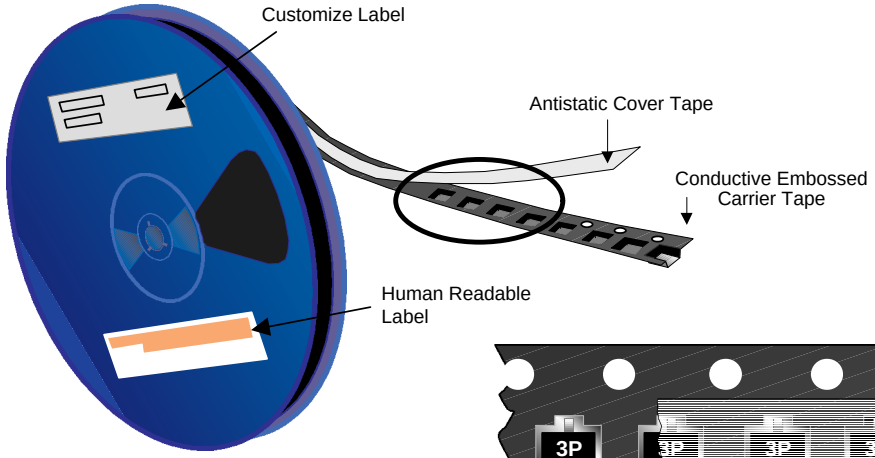


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

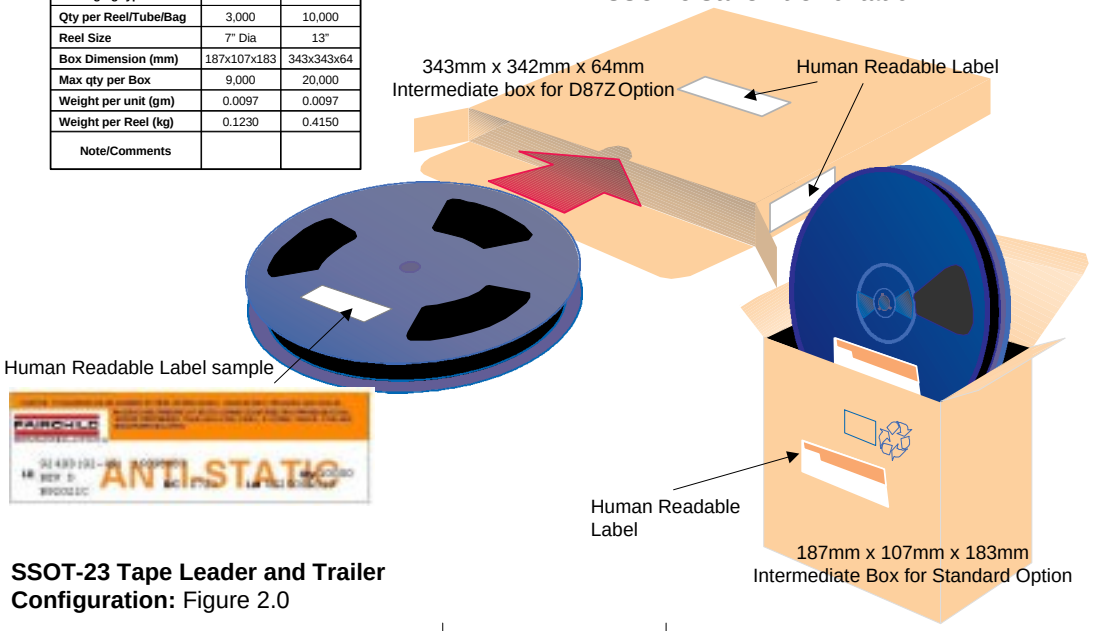
SuperSOT™-3 Tape and Reel Data and Package Dimensions

SSOT-3 Packaging
Configuration: Figure 1.0

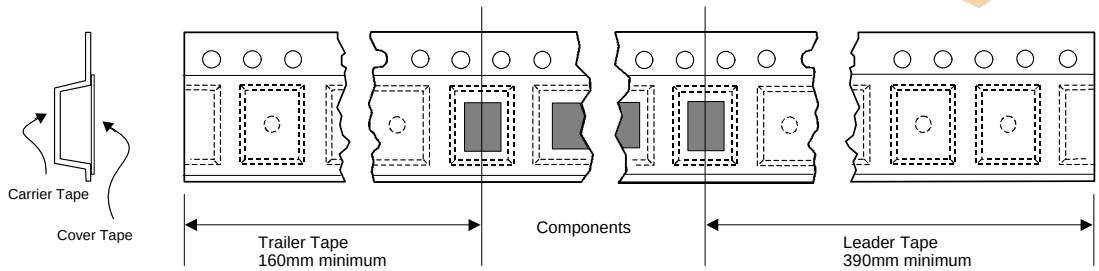


SSOT-3 Std Packaging Information		
Packaging Option	Standard (no flow code)	D87Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	10,000
Reel Size	7" Dia	13"
Box Dimension (mm)	187x107x183	343x343x64
Max qty per Box	9,000	20,000
Weight per unit (gm)	0.0097	0.0097
Weight per Reel (kg)	0.1230	0.4150
Note/Comments		

SSOT-3 Std Unit Orientation

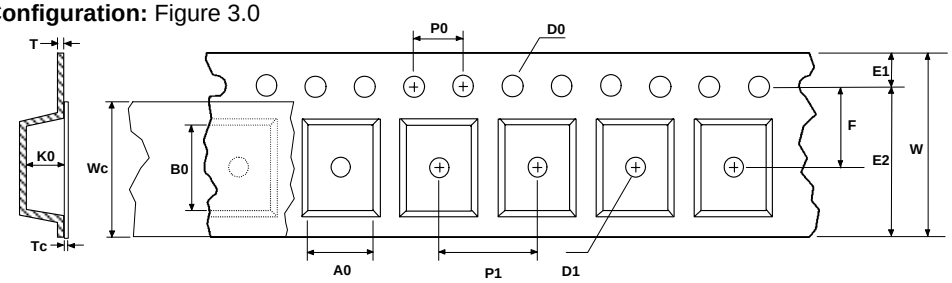


SSOT-23 Tape Leader and Trailer
Configuration: Figure 2.0



SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

SSOT-3 Embossed Carrier Tape
Configuration: Figure 3.0

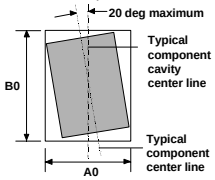


User Direction of Feed

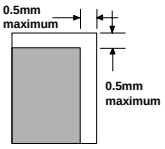
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.00 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

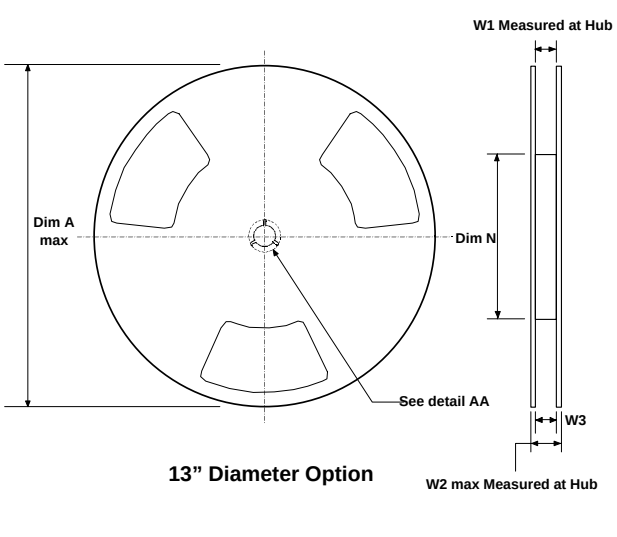


Sketch B (Top View)
Component Rotation

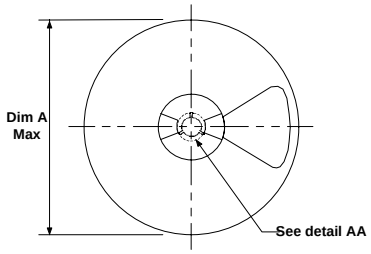


Sketch C (Top View)
Component lateral movement

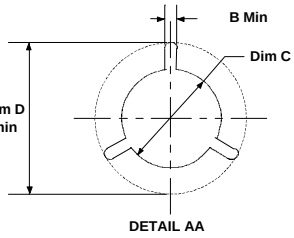
SSOT-3 Reel Configuration: Figure 4.0



13" Diameter Option



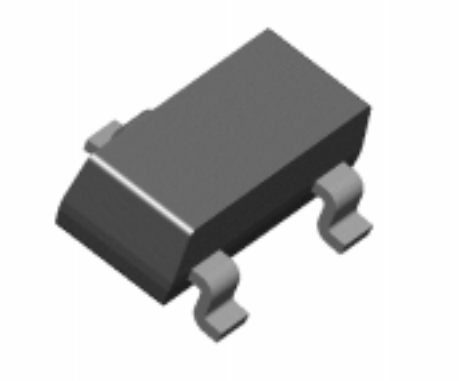
7" **Diameter Option**

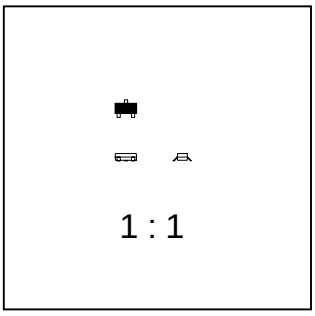


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 – 0.429 7.9 – 10.9

SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-3 (FS PKG Code 32)

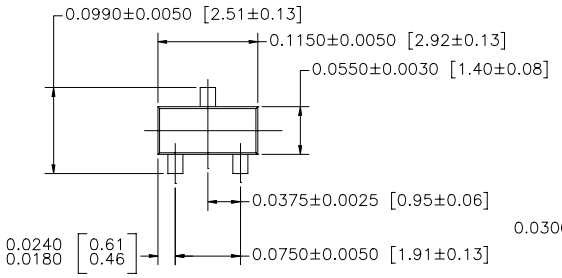


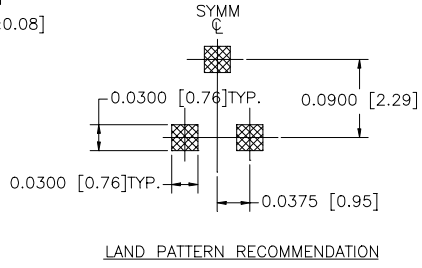


Scale 1:1 on letter size paper

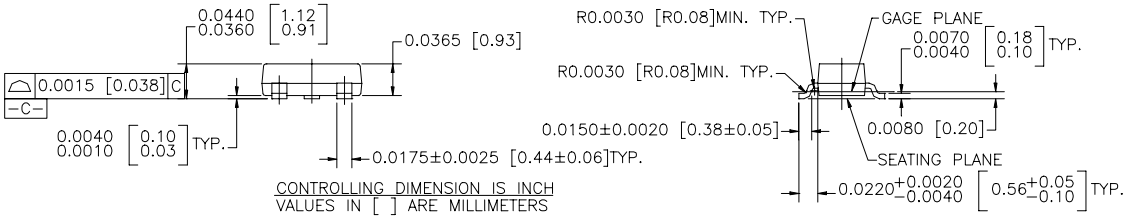
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097





LAND PATTERN RECOMMENDATION



NOTES : UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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