

February 1999

Advance Information

1.0 Features

- On-board crystal oscillator
- Phase-locked loop (PLL) synthesizes desired CLK frequency
- Internal loop filter
- Internal crystal oscillator load capacitance (16pF nominal)
- Only external components required are decoupling capacitors
- Minimal board footprint (8-pin 0.150" SOIC package)

2.0 Description

The FS6118 is a monolithic CMOS frequency synthesizer IC designed for cost sensitive or space limited applications.

An on-board crystal oscillator accepts a quartz crystal and provides a different, synthesized frequency on the CLK output. The device is packaged in an 8-pin SOIC package for a minimal board footprint.

Custom factory-programmed clock frequencies are available. Please contact your local AMI sales representative for more information.

Figure 1: Block Diagram

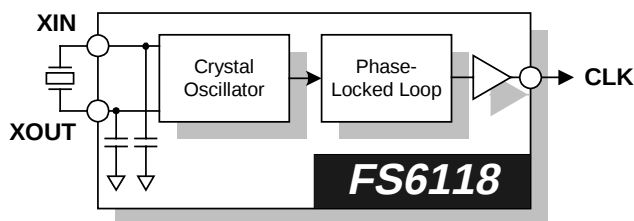


Figure 2: Pin Configuration

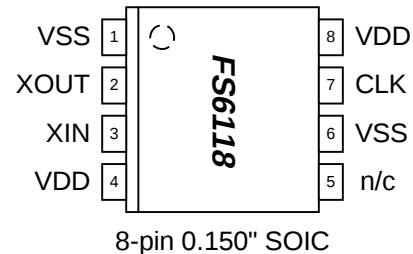


Table 1: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	P	VSS	Ground
2	AO	XOUT	Crystal oscillator feedback
3	AI	XIN	Crystal oscillator drive
4	P	VDD	Power supply (+5V)
5	--	N/C	No Connection
6	P	VSS	Ground
7	DO	CLK	Clock Output
8	P	VDD	Power Supply (+5V)

Table 2: Font Description

DEVICE	CRYSTAL FREQUENCY (MHz)	CLK FREQUENCY (MHz)
FS6118-01	14.31818	40.0000

Custom frequencies available – contact AMI for more information

FS6118

Clock Generator IC



Advance Information

February 1999

3.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	$V_{SS}-0.5$	7	V
Input Voltage, dc	V_I	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	V_O	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV



CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}	5V $\pm$ 10%	4.5	5.0	5.5	V
Ambient Operating Temperature Range	T_A		0		70	°C

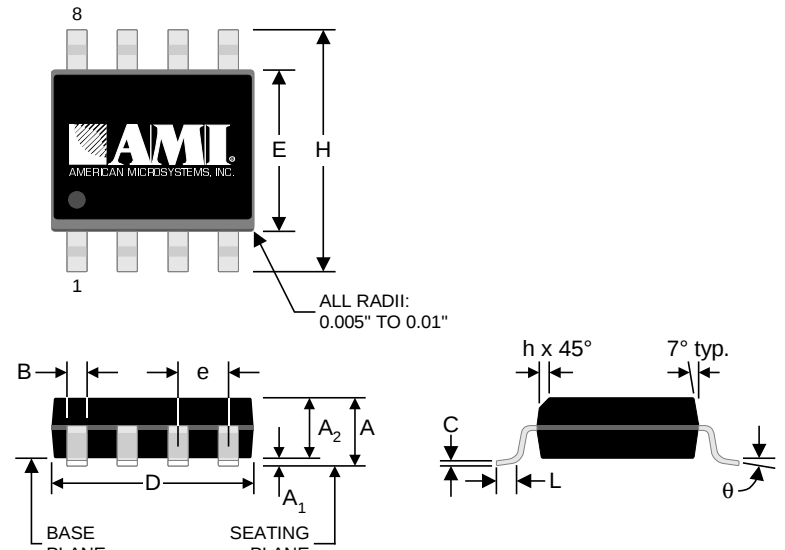
February 1999

Advance Information

4.0 Package Information

Table 5: 8-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.189	0.196	4.80	4.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
θ	0°	8°	0°	8°



The diagram illustrates the mechanical dimensions of the 8-pin SOIC package. It includes a top view showing the package body with pins 1 through 8, and a side view showing the profile. Key dimensions labeled include: A (package height), A1 (lead height at seating plane), A2 (lead height at base plane), B (lead thickness), C (lead thickness at heel), D (package width), E (pitch), e (pitch), h (lead thickness), L (lead length), and θ (lead angle). A note specifies 'ALL RADII: 0.005" TO 0.01"'. The side view also shows a 45° fillet and a 7° typical lead angle.

Table 6: 8-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	θ_{JA}	Air flow = 0 m/s	173	°C/W
Lead Inductance, Self	L_{11}	Corner lead	2.0	nH
		Center lead	1.6	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.27	pF

FS6118

Clock Generator IC



Advance Information

February 1999

5.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-802	FS6118-01	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape-and-Reel
11640-812	FS6118-01	8-pin (0.150") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tubes

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