# HA12240FP

## Bus Interface Driver/Receiver IC

REJ03F0095-0100Z
Rev.1.0
Dec.01.2003

### Description

The HA12240FP is developed to be used as a bus interface driver/receiver IC in automotive audio equipment controllers. It implements a two-wire serial bus.

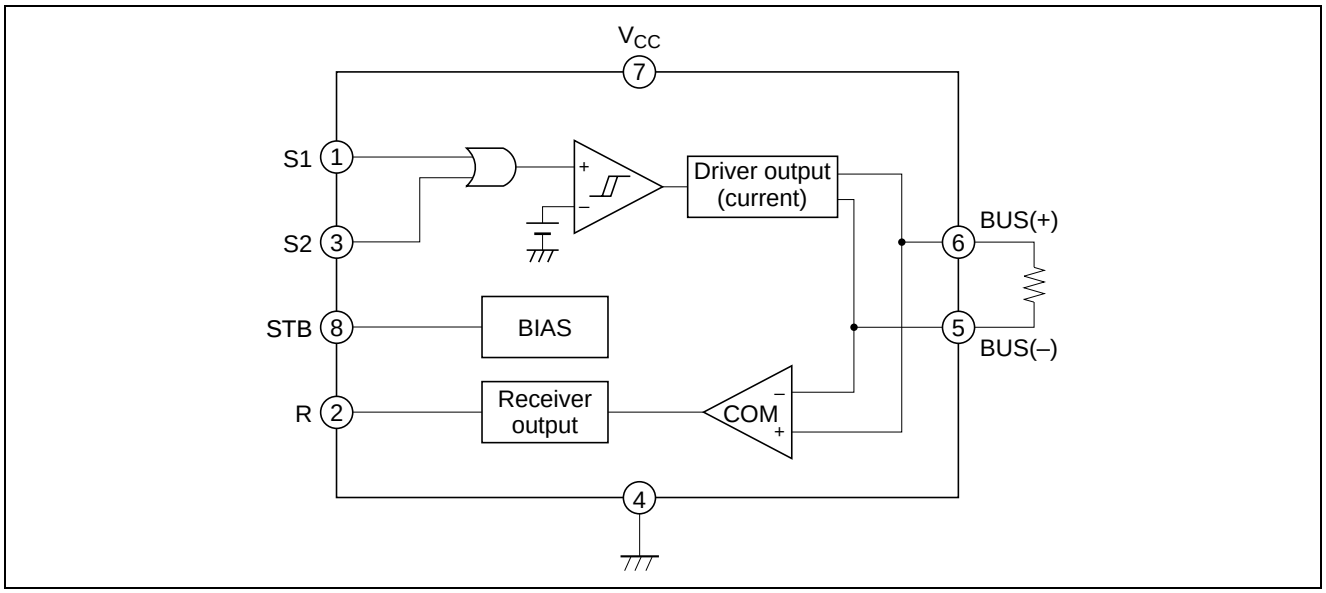
### Functions

- Two-input OR circuit
- Input comparator circuit (3.3 V and 5.0 V available)
- Current output driver circuit
- Receiver input comparator circuit
- Receiver output circuit (Open-collector output)
- Standby circuit

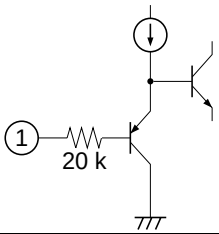
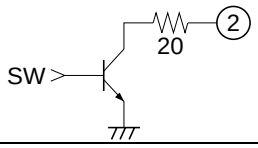
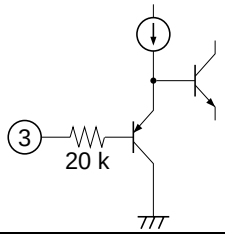
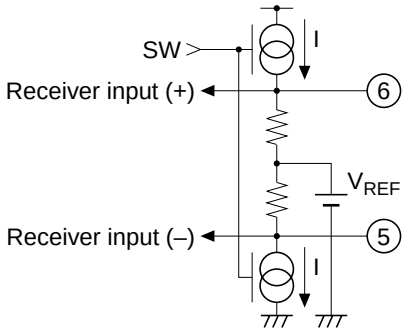
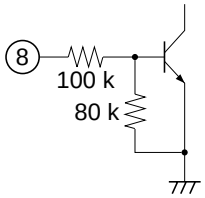
### Features

- Supports two data inputs (Pins 1 and 3 are the input pins)
- Comparators with hysteresis characteristics are adopted for the inputs (3.3 V and 5.0 V available)
- Current drive output drivers adopted (Output current: 3.8 mA typical)
- Comparators with hysteresis characteristics are adopted for the receivers
- Wide receiver common-mode input operating range (Common-mode input operating range: 0 to 5 V typical)
- The driver output /the receiver input (pins 5 and 6) can withstand high voltages (Maximum ratings of 18 V)
- Standby functions (standby mode when pin 8 becomes low level)
- Operating power-supply voltage range of 5 V ± 0.5 V

### Block Diagram



## Pin Functions

| Pin No. | Symbol | Function | Equivalent Circuit |
|---|---|---|---|
| 1 | S1 | Data input pin 1 |  |
| 2 | R | Receiver output pin |  |
| 3 | S2 | Data input pin 2 |  |
| 4 | GND | GND pin | |
| 5 | BUS(–) | Bus output (–),<br>Receiver input (–) pin |  |
| 6 | BUS(+) | Bus output (+),<br>Receiver input (+) pin | |
| 7 | $V_{CC}$ | Power supply pin | |
| 8 | STB | Standby input pin (Lo: ON, Hi: OFF) |  |

## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Ratings | Unit | Note |
|---|---|---|---|---|
| Power-supply voltage | $V_{CC}$ | 7 | V | |
| Input voltage | $V_{IN}$ | GND–0.3 to $V_{CC}$+0.3 | V | |
| Bus input voltage | Vbus | 18 | V | |
| Allowable power dissipation | Pd | 400 | mW | Ta ≤ 85°C |
| Operating temperature | Topr | –40 to +85 | °C | |
| Storage temperature | Tstg | –55 to +125 | °C | |

Note: Recommended operating power supply voltage range: 5 V ± 0.5 V

## Electrical Characteristics

($V_{CC}$ = 5.0 V, Ta = 25°C)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Test Pin | Test Circuit |
|---|---|---|---|---|---|---|---|---|---|
| S1 | High-level input voltage | $V_{IHS1}$ | 2.1 | — | — | V | V1 = 0→5 V, V3 = 0 V, V6 – V5 = 110 mV↑ | 1 | Fig. 1 |
| | Low-level input voltage | $V_{ILS1}$ | — | — | 1.65 | V | V1 = 5→0 V, V3 = 0 V, V6 – V5 = 30 mV↓ | 1 | |
| | High-level input current | $I_{IHS1}$ | — | — | 1 | µA | V1 = 5 V, V3 = 0 V | 1 | |
| | Low-level input current | $I_{ILS1}$ | — | — | 1 | µA | V1 = 0 V, V3 = 0 V | 1 | |
| S2 | High-level input voltage | $V_{IHS2}$ | 2.1 | — | — | V | V3 = 0→5 V, V1 = 0 V, V6 – V5 = 110 mV↑ | 3 | Fig. 1 |
| | Low-level input voltage | $V_{ILS2}$ | — | — | 1.65 | V | V3 = 5→0 V, V1 = 0 V, V6 – V5 = 30 mV↓ | 3 | |
| | High-level input current | $I_{IHS2}$ | — | — | 1 | µA | V1 = 0 V, V3 = 5 V | 3 | |
| | Low-level input current | $I_{ILS2}$ | — | — | 1 | µA | V1 = 0 V, V3 = 0 V | 3 | |
| Driver | High-level output voltage (+) | $V_{OHD+}$ | 1.8 | 2.5 | 3.2 | V | V1 = 5 V, V3 = 0 V | 6 | Fig. 1 |
| | High-level output voltage (–) | $V_{OHD–}$ | 1.8 | 2.5 | 3.2 | V | V1 = 5 V, V3 = 0 V | 5 | |
| | High-level output current | $I_{OH}$ | 3.1 | 3.8 | 4.5 | mA | V1 = 5 V, V3 = 0 V, $I_{OH} = ((V_{OHD+}) – (V_{OHD–}))/60$ | 5, 6 | |
| | Low-level output current | $I_{OL}$ | — | — | 1 | µA | V1 = 0 V, V3 = 0 V, $I_{OL} = ((V_{OP+}) – (V_{OP–}))/R_I$ | 5, 6 | |
| Reference operating voltage (+) | | $V_{OP+}$ | 2.3 | 2.5 | 2.7 | V | V1 = 0 V, V3 = 0 V | 6 | Fig. 1 |
| Reference operating voltage (–) | | $V_{OP–}$ | 2.3 | 2.5 | 2.7 | V | V1 = 0 V, V3 = 0 V | 5 | Fig. 1 |
| Driver output resistance *[1] | | $R_O$ | 5 | 10 | 15 | kΩ | V1 = 5 V, V3 = 0 V, V8 = 5 V, $R_O$ = 0.6 V/(I6A – I6B) | | Fig. 3 |

Note: 1. Measure the current when V6 = ($V_{OP+}$) + 0.3 V to make I6A and measure the current when V6 = ($V_{OP+}$) – 0.3 V to make I6B.

## Electrical Characteristics (cont.)

($V_{CC}$ = 5.0 V, Ta = 25°C)

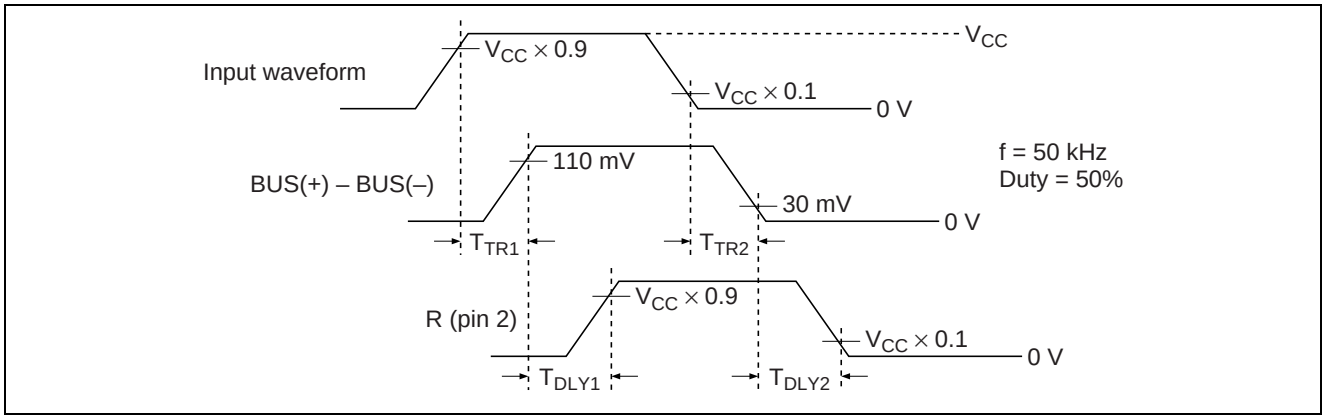
| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions | Test Pin | Test Circuit |
|---|---|---|---|---|---|---|---|---|---|
| Receiver | High-level input voltage (1) | $V_{IH1}$ | — | 80 | 110 | mV | V6 = 0→5 V, Pin2 = 4 V or more, V1 = 0 V, V3 = 0 V, V5 = 0 V, $V_{IH1}$ = V6 – V5 | 2 | Fig. 2 |
| | High-level input voltage (2) | $V_{IH2}$ | — | 80 | 110 | mV | V6 = 0→5 V, Pin2 = 4 V or more, V1 = 0 V, V3 = 0 V, V5 = 4.5 V, $V_{IH2}$ = V6 – V5 | 2 | |
| | Low-level input voltage (1) | $V_{IL1}$ | 30 | 50 | — | mV | V6 = 5→0 V, Pin2 = 1 V or less, V1 = 0 V, V3 = 0 V, V5 = 0 V, $V_{IL1}$ = V6 – V5 | 2 | |
| | Low-level input voltage (2) | $V_{IL2}$ | 30 | 50 | — | mV | V6 = 5→0 V, Pin2 = 1 V or less, V1 = 0 V, V3 = 0 V, V5 = 4.5 V, $V_{IL2}$ = V6 – V5 | 2 | |
| | Input hysteresis voltage (1) | $V_{IHYS1}$ | 15 | 30 | 45 | mV | $V_{IHYS1}$ = $V_{IH1}$ – $V_{IL1}$ | | |
| | Input hysteresis voltage (2) | $V_{IHYS2}$ | 15 | 30 | 45 | mV | $V_{IHYS2}$ = $V_{IH2}$ – $V_{IL2}$ | | |
| | High-level common-mode input voltage | $V_{IHCOM}$ | 4.5 | — | — | V | V5 = 0→5 V, V5 when pin2 = 4 V or less, V1 = 0 V, V3 = 0 V, V6 – V5 = 110 mV | 5 | Fig. 2 |
| | Low-level common-mode input voltage | $V_{ILCOM}$ | 5 | — | — | V | V5 = 0→5 V, V5 when pin2 = 0.3 V or more, V1 = 0 V, V3 = 0 V, V6 – V5 = 30 mV | 5 | |
| | Input resistance *[1] | $R_I$ | 25 | 35 | 45 | kΩ | V1 = 0 V, V3 = 0 V, V8 = 5 V, $R_I$ = 0.6 V/(I6A – I6B) | 5, 6 | Fig. 3 |
| | High-level output leakage current 1 | $I_{OH1}$ | — | — | 1 | μA | V1 = 5 V, V3 = 0 V, V8 = 5 V | 2 | Fig. 1 |
| | High-level output leakage current 2 | $I_{OH2}$ | — | — | 1 | μA | $V_{CC}$ = 0 V, V1,V3,V8 = 0 V | 2 | |
| | High-level output leakage current 3 | $I_{OH3}$ | — | — | 1 | μA | V1,V3,V8 = 0 V | 2 | |
| | Low-level output voltage 1 | $V_{OL1}$ | — | — | 0.6 | V | V1 = 0 V, V3 = 0 V, V8 = 5 V, Adjust $V_{RL}$ to make apply current = 1.5 mA | 2 | |
| | Low-level output voltage 2 | $V_{OL2}$ | — | — | 0.3 | V | V1 = 0 V, V3 = 0 V, V8 = 5 V, Adjust $V_{RL}$ to make apply current = 200 μA | 2 | |
| Quiescent current 1 | | $I_{CC}H$ | 4.5 | 6.5 | 8.5 | mA | V1 = 5 V, V3 = 0 V | 7 | Fig. 1 |
| Quiescent current 2 | | $I_{CC}L$ | 1.05 | 1.46 | 1.87 | mA | V1 = 0 V, V3 = 0 V | 7 | Fig. 1 |
| Driver delay time (L→H) | | $T_{TR1}$ | — | 100 | 300 | ns | See operating waveform figure | 5, 6 | Fig. 5 |
| Driver delay time (H→L) | | $T_{TR2}$ | — | 100 | 300 | ns | See operating waveform figure | 5, 6 | |
| Receiver delay time (L→H) | | $T_{DLY1}$ | — | 600 | 1200 | ns | See operating waveform figure | 2 | |
| Receiver delay time (H→L) | | $T_{DLY2}$ | — | 200 | 600 | ns | See operating waveform figure | 2 | |

Note: 1. Measure the current when V6 = ($V_{OP+}$) + 0.3 V to make I6A and measure the current when V6 = ($V_{OP+}$) – 0.3 V to make I6B.

## Electrical Characteristics (cont.)

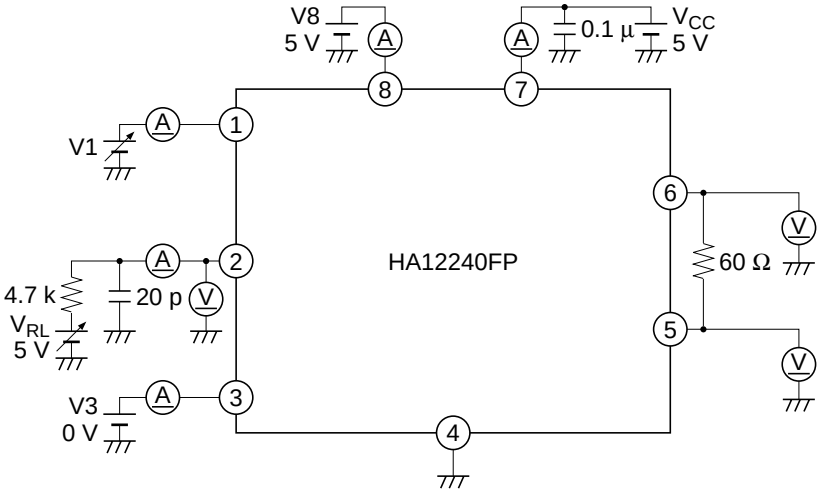
($V_{CC}$ = 5.0 V, Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Test Pin | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power-supply off output leakage current | $I_{OLEAK}$ | — | — | 1 | µA | $V_{CC}$ = 0 V, V8 = 0 V, V6 = 5 V, V1 = 0 V, V3 = 0 V, SW1 ON | 6 | Fig. 4 |
| Standby mode current drain | $I_{CCstb}$ | — | — | 1 | µA | V1 = 5 V, V3 = 0 V, V8 = 0 V | 7 | Fig. 4 |
| Standby mode output leakage current | Istb-Leak | — | — | 1 | µA | V1 = 5 V, V3 = 0 V, V8 = 0 V, V6 = 5 V, SW1 ON | 6 | Fig. 4 |
| Standby mode high-level input voltage | VstbH | 2 | — | — | V | V8 = 0→5 V, V8 when pin5,6 = 2.3 V or more, V1 = 0 V, V3 = 0 V | 8 | Fig. 1 |
| Standby mode low-level input voltage | VstbL | — | — | 0.9 | V | V8 = 5→0 V, V8 when current flowing into pin7 = 1 µA or less, V1 = 5 V, V3 = 0 V | 8 | Fig. 1 |
| Standby mode high-level input current | IstbH | — | 50 | 100 | µA | V1 = 5 V, V3 = 0 V, V8 = 5 V | 8 | Fig. 1 |
| Standby mode low-level input current | IstbL | — | — | 1 | µA | V1 = 5 V, V3 = 0 V, V8 = 0 V | 8 | Fig. 1 |

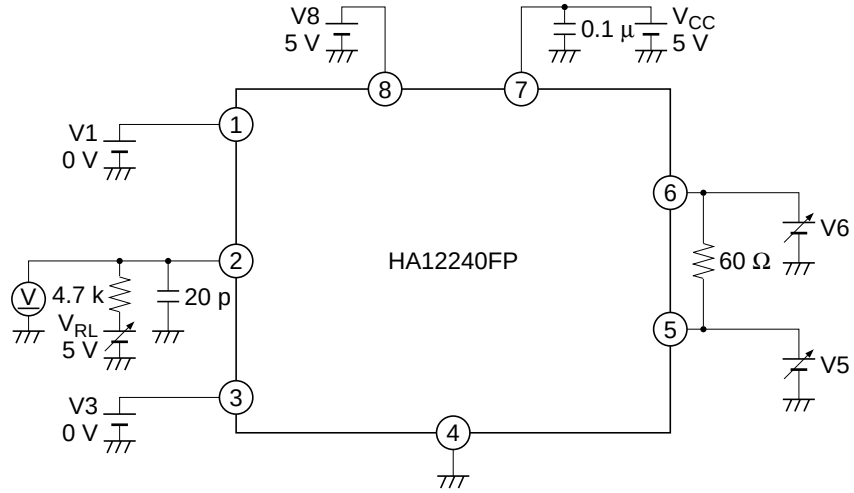



**Input/Output Waveform Figure**

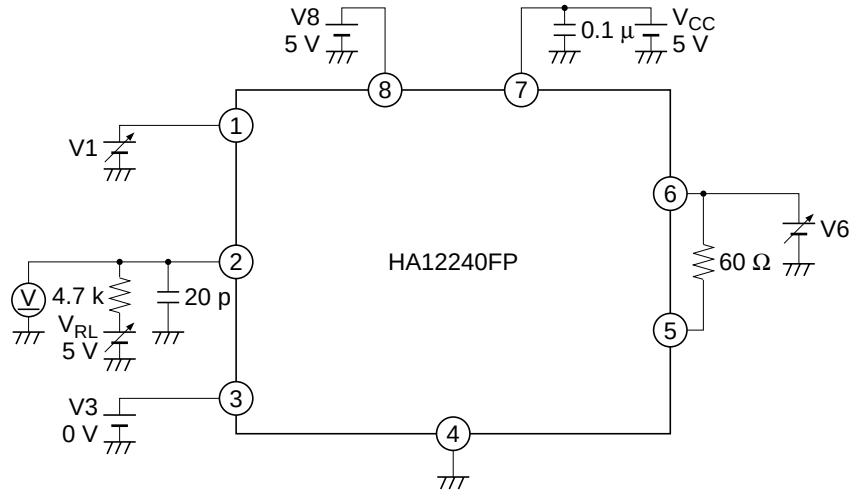
## Test Circuits



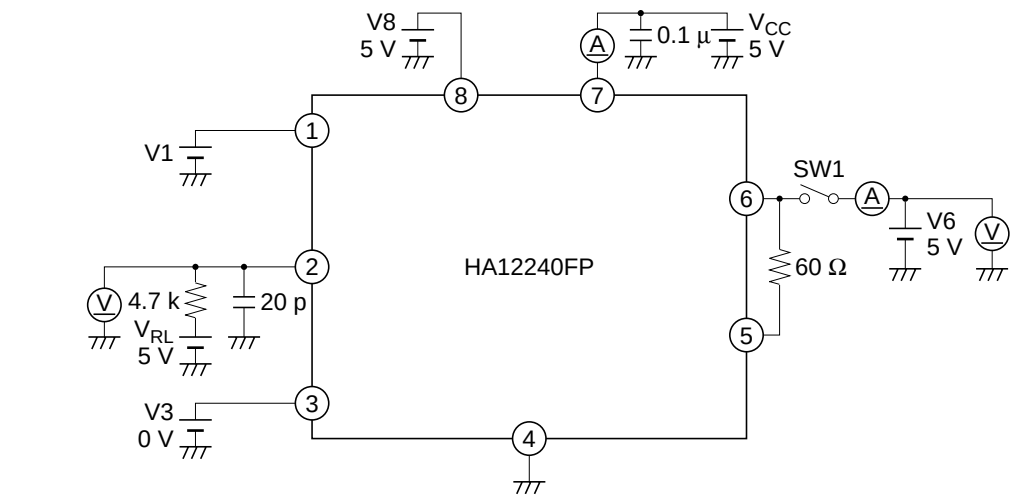

Test Circuit 1



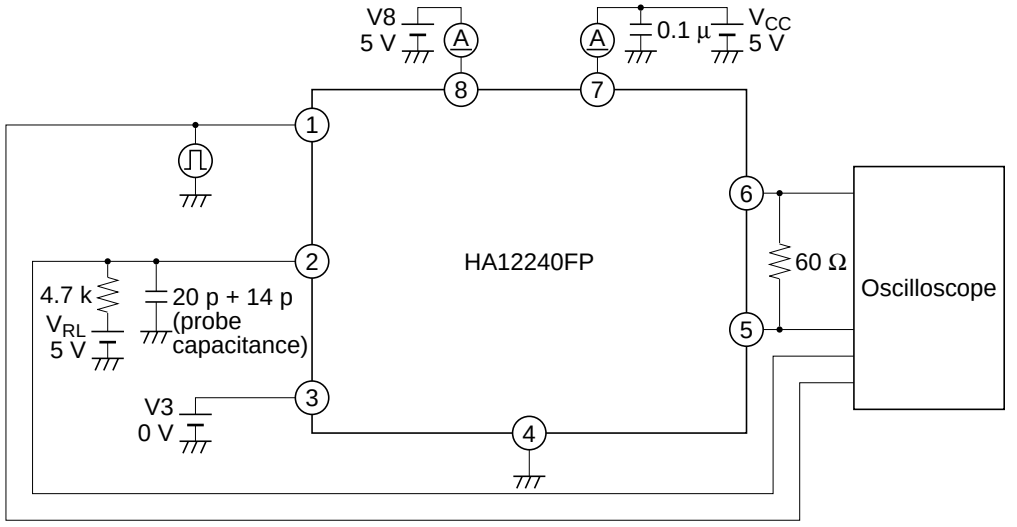

Test Circuit 2




Test Circuit 3

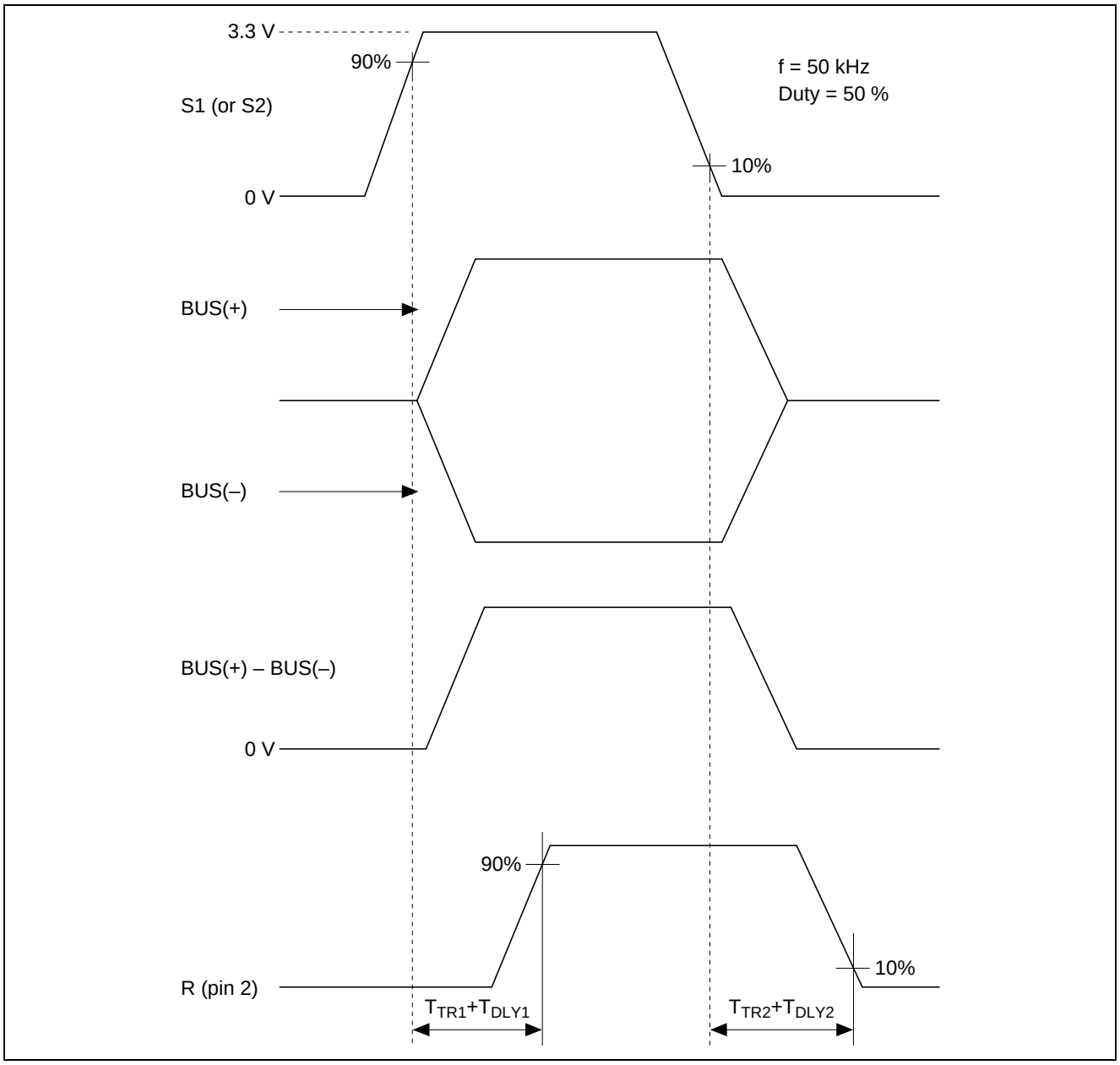



Test Circuit 4

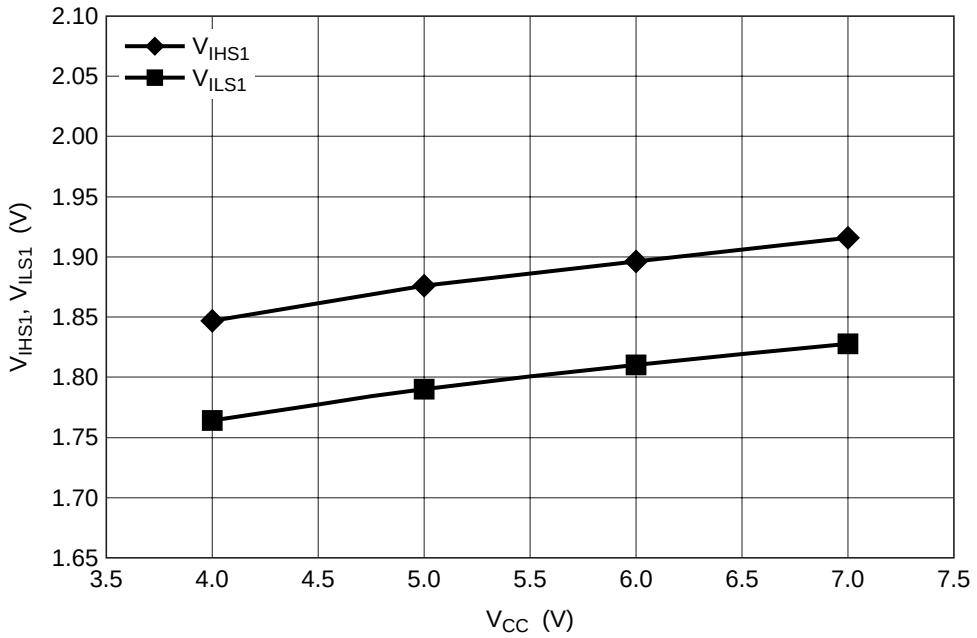


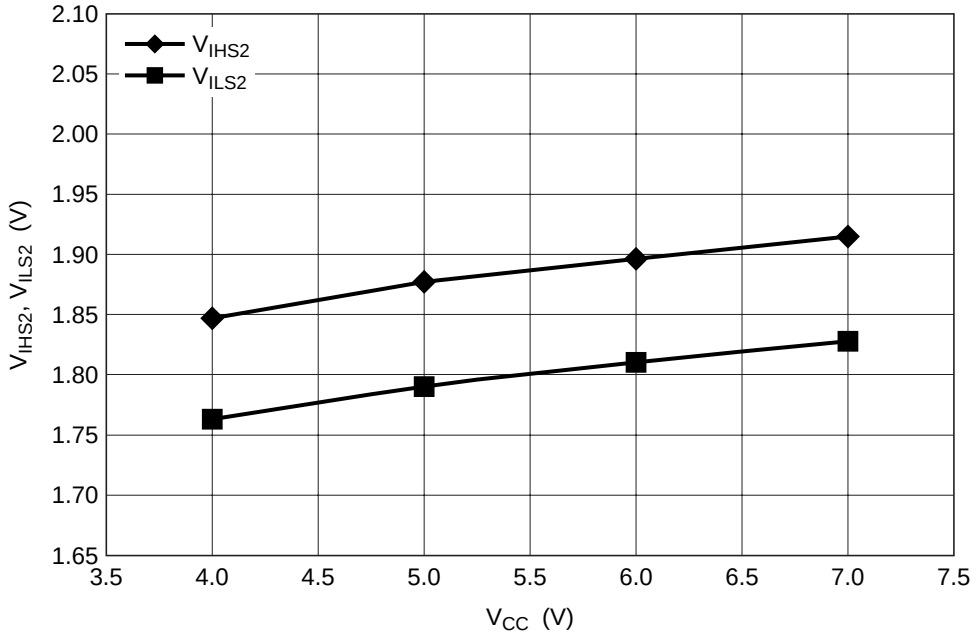

Test Circuit 5

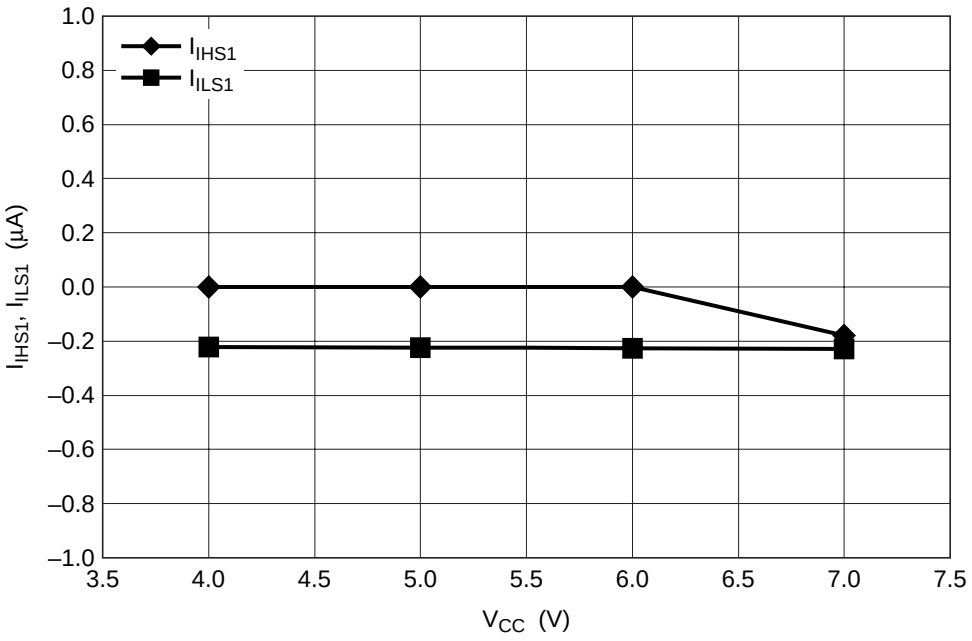
## Operating Waveforms



## Main Characteristics

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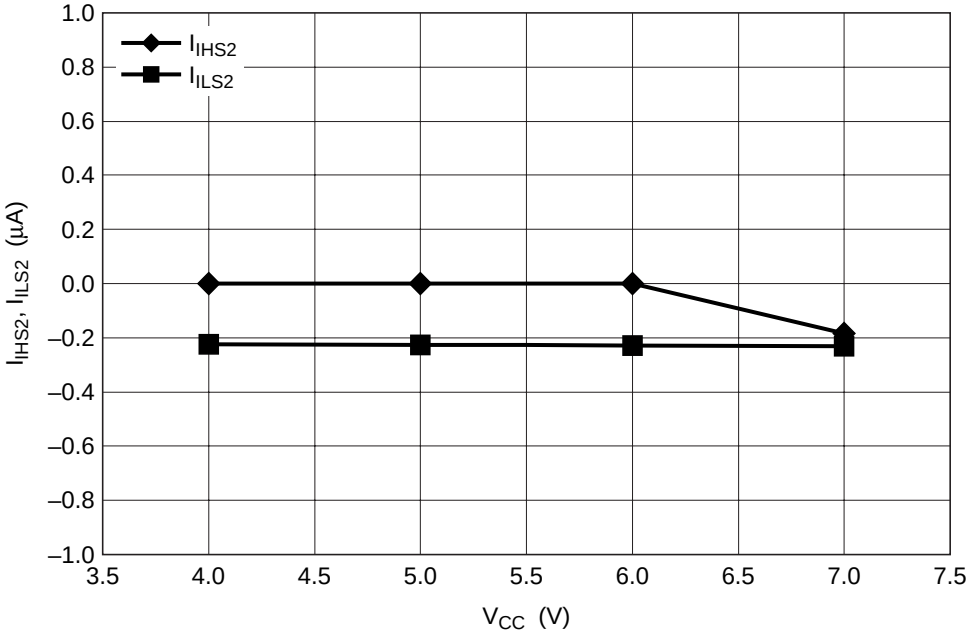
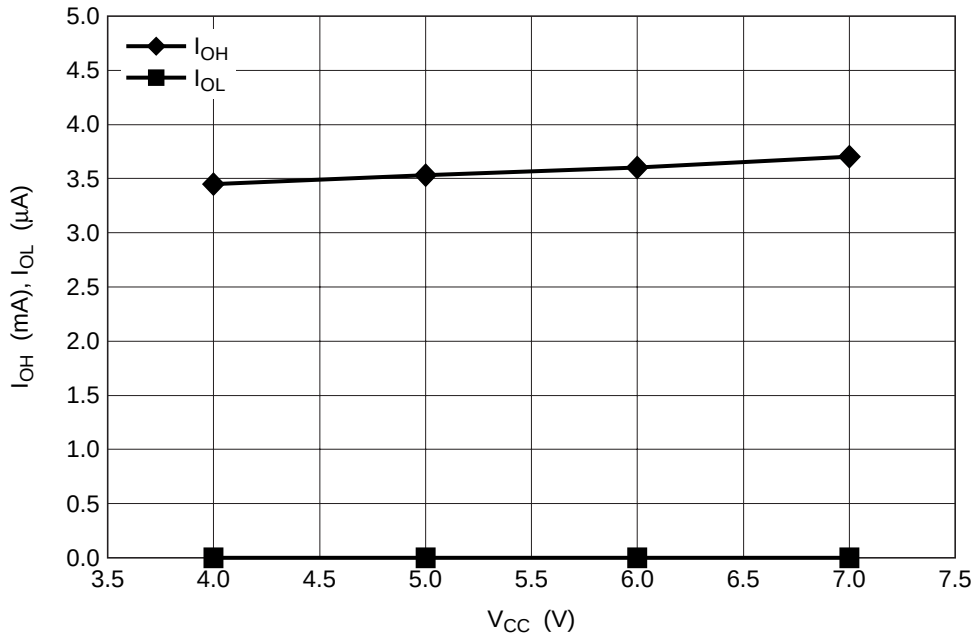
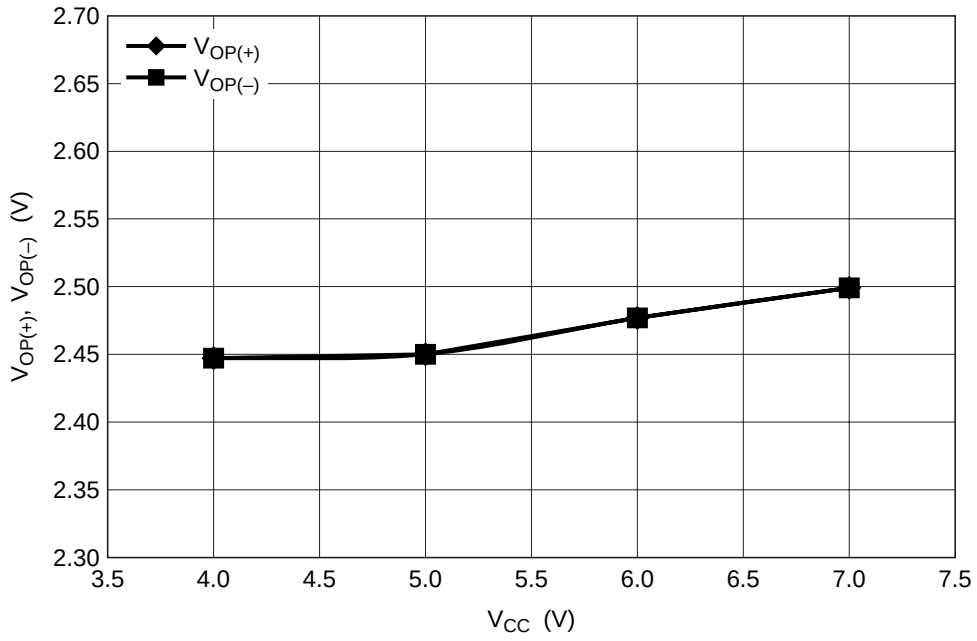
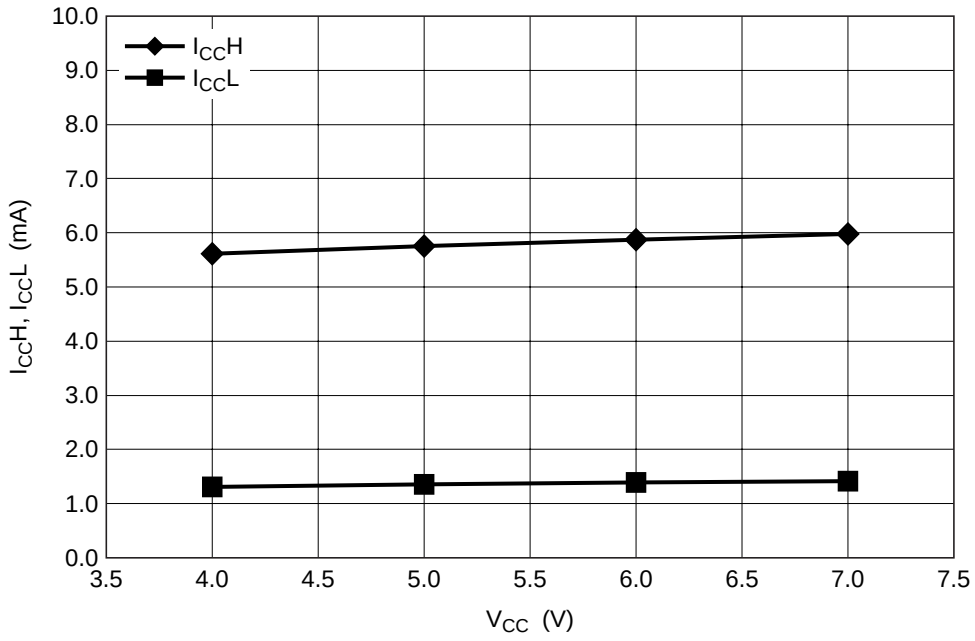
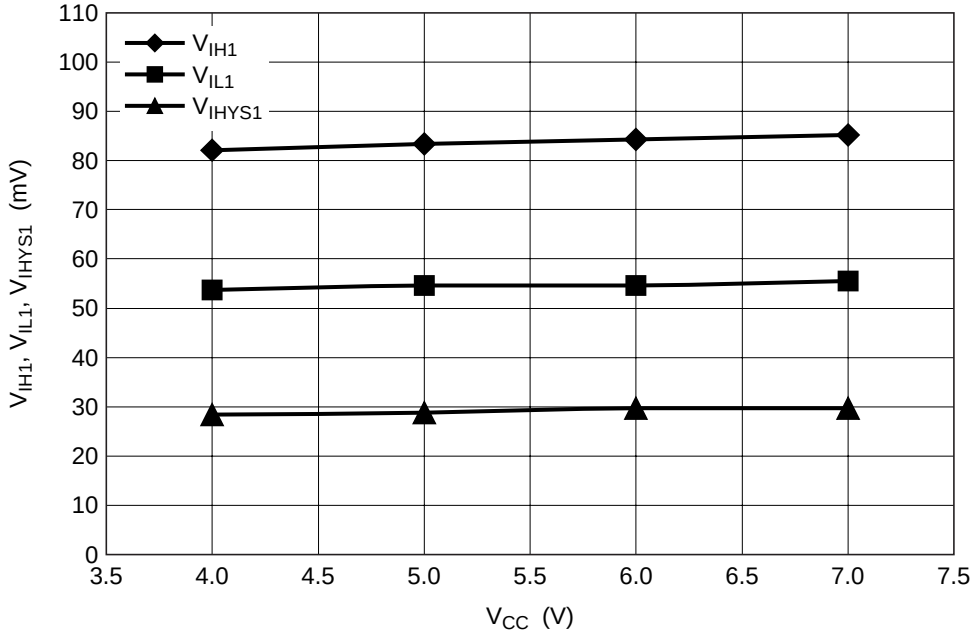
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
$I_{IHS1}$
$I_{ILS1}$
$I_{IHS1}$, $I_{ILS1}$ (µA)
$V_{CC}$ (V)

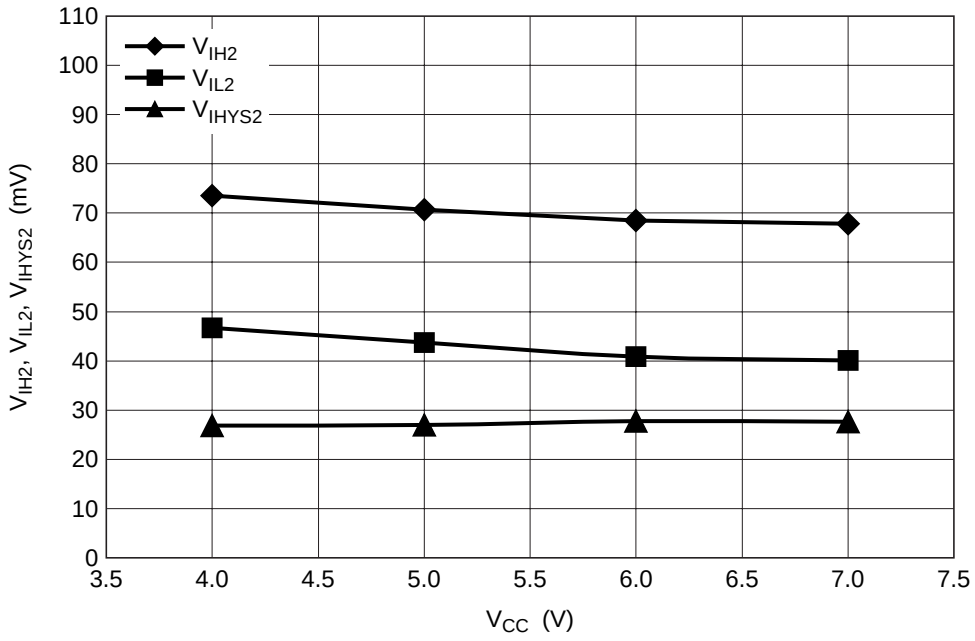

1.0
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
$I_{IHS2}$
$I_{ILS2}$
$I_{IHS2}$, $I_{ILS2}$ (µA)
$V_{CC}$ (V)

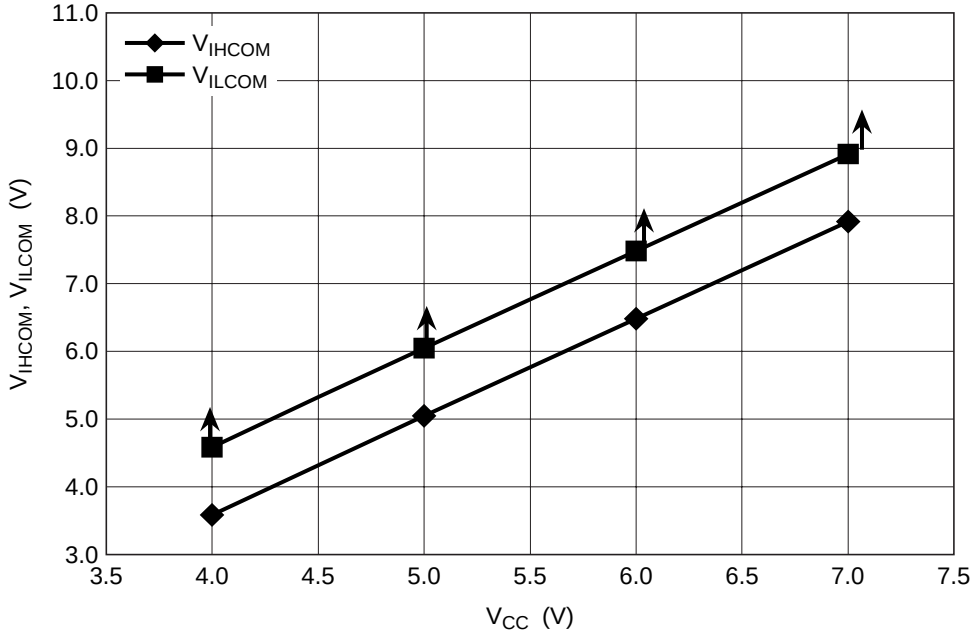

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
IOH
IOL
IOH (mA), IOL (µA)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)


2.70
2.65
2.60
2.55
2.50
2.45
2.40
2.35
2.30
VOP(+)
VOP(–)
VOP(+), VOP(–) (V)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)


10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
ICCH
ICCL
ICCH, ICCL (mA)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)


110
100
90
80
70
60
50
40
30
20
10
0
VIH1
VIL1
VIHYS1
VIH1, VIL1, VIHYS1 (mV)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)


110
100
90
80
70
60
50
40
30
20
10
0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VIH2
VIL2
VIHYS2
VIH2, VIL2, VIHYS2 (mV)
VCC (V)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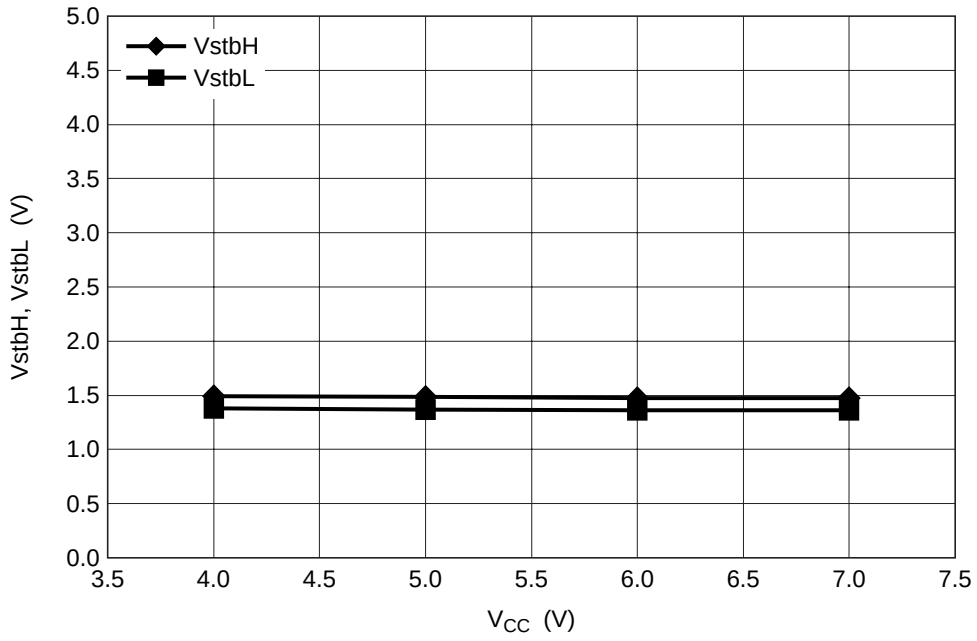
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VIHCOM
VILCOM
VIHCOM, VILCOM (V)
VCC (V)


VstbH
VstbL
VstbH, VstbL (V)
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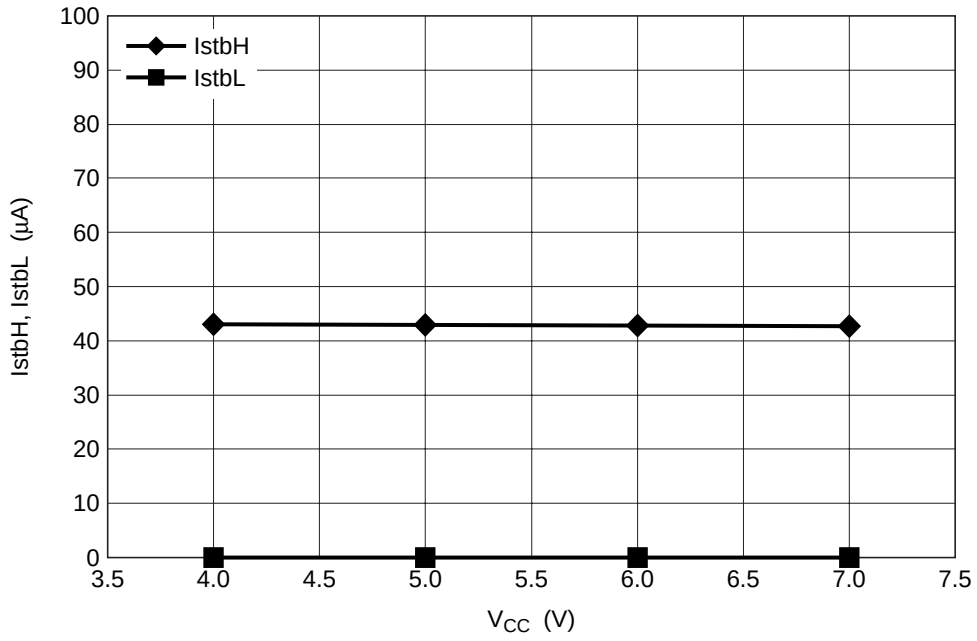
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)


IstbH
IstbL
IstbH, IstbL (µA)
100
90
80
70
60
50
40
30
20
10
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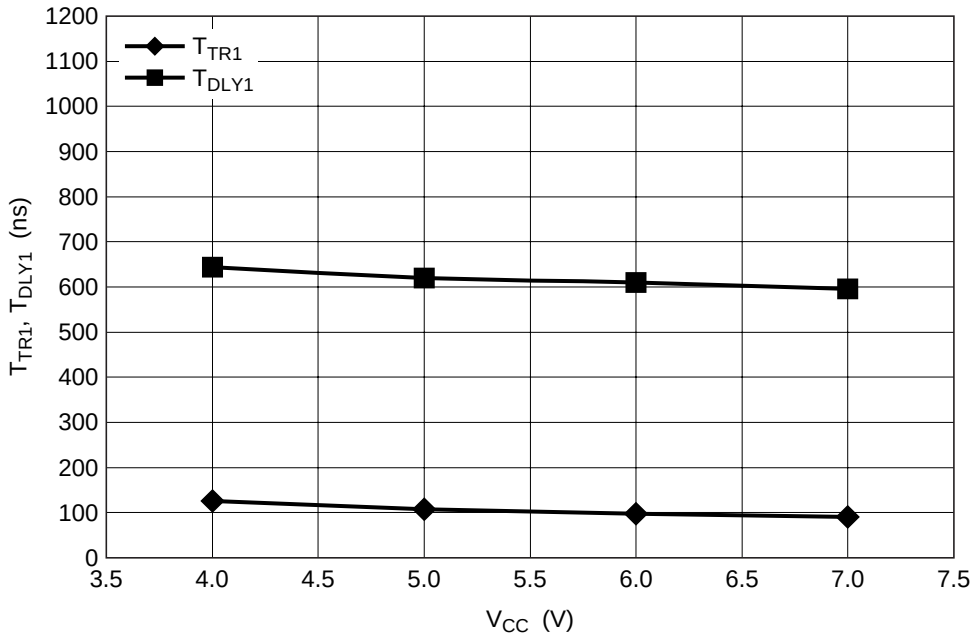
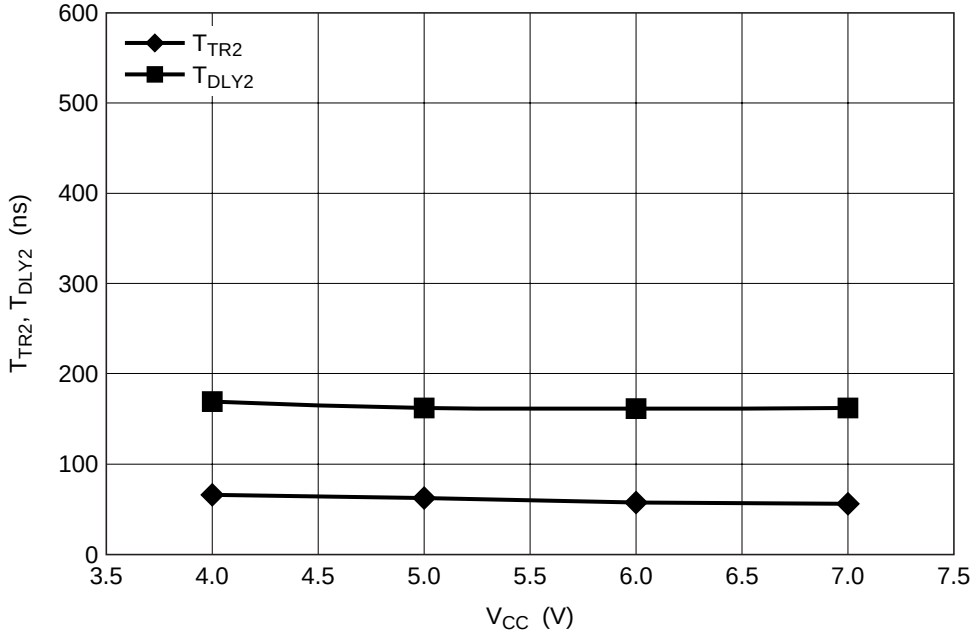
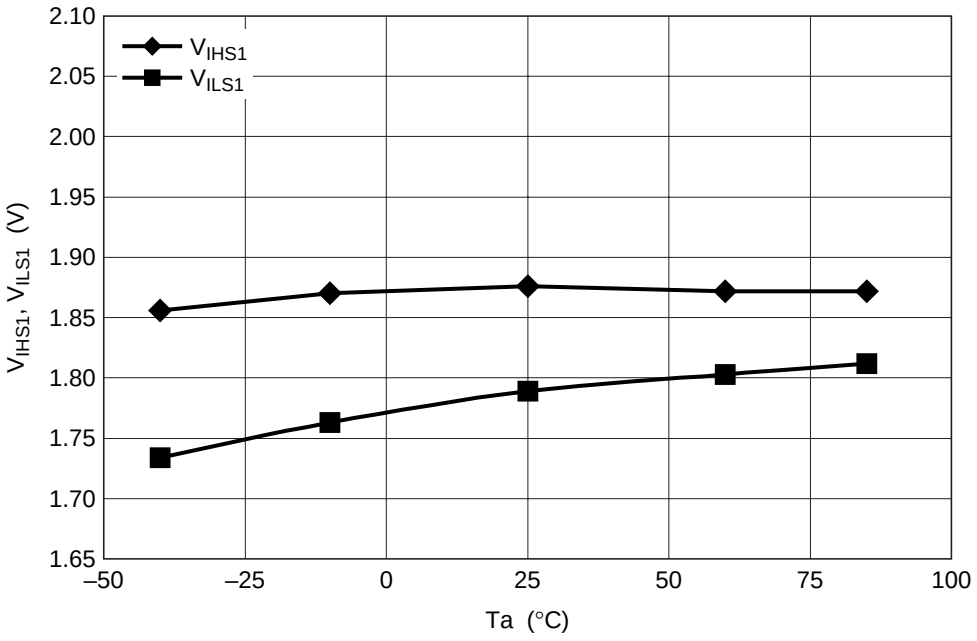
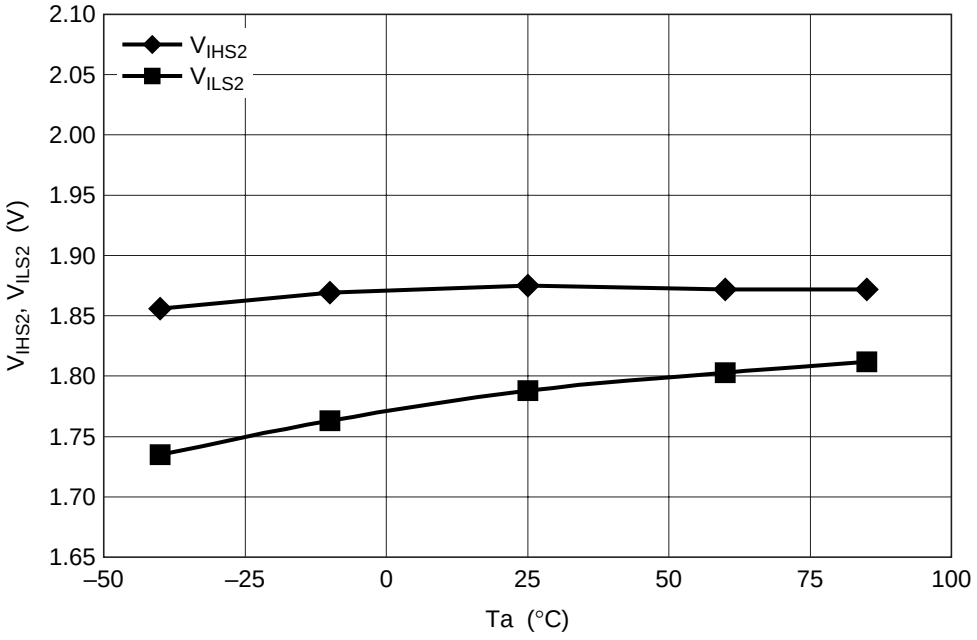
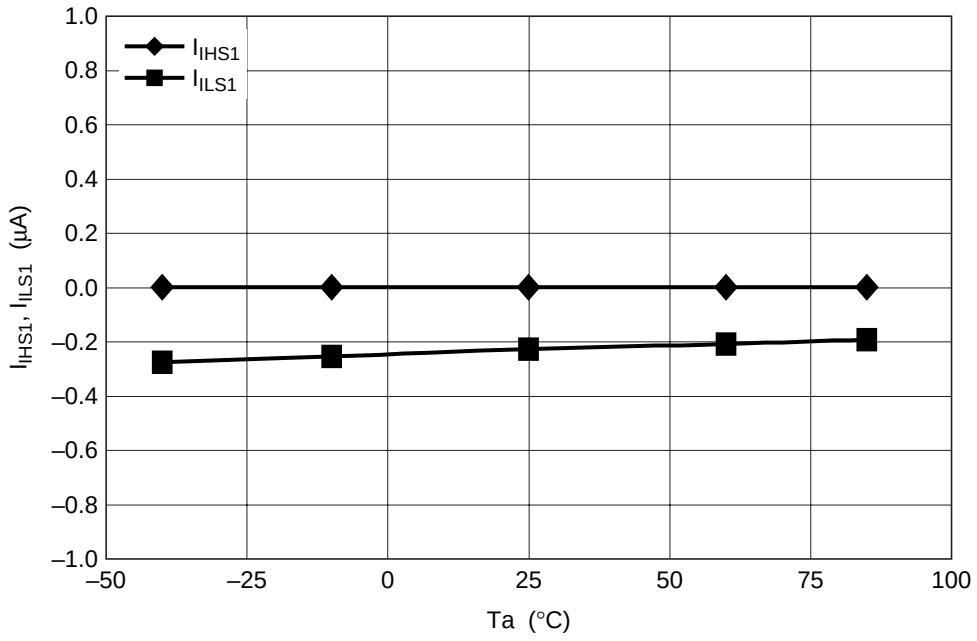
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
VCC (V)

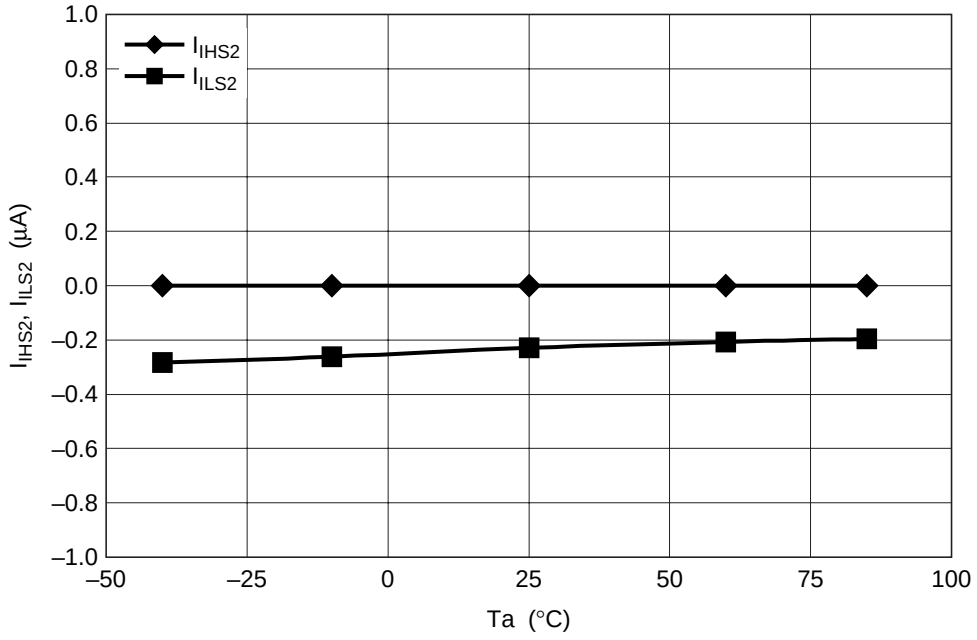

1200
1100
1000
900
800
700
600
500
400
300
200
100
0
$T_{TR1}$
$T_{DLY1}$
$T_{TR1}$, $T_{DLY1}$ (ns)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
$V_{CC}$ (V)

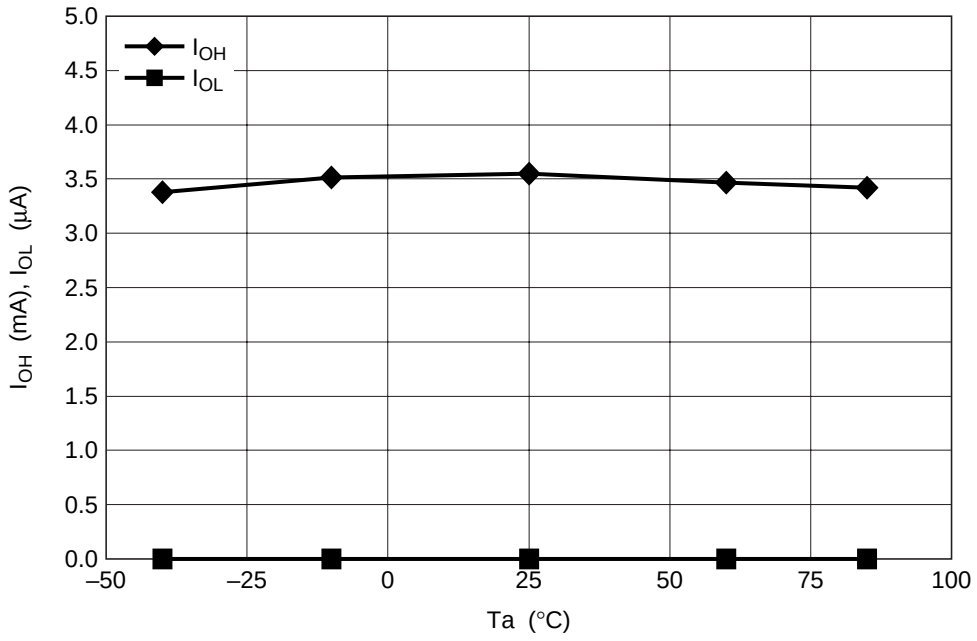

600
500
400
300
200
100
0
$T_{TR2}$
$T_{DLY2}$
$T_{TR2}$, $T_{DLY2}$ (ns)
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
7.5
$V_{CC}$ (V)

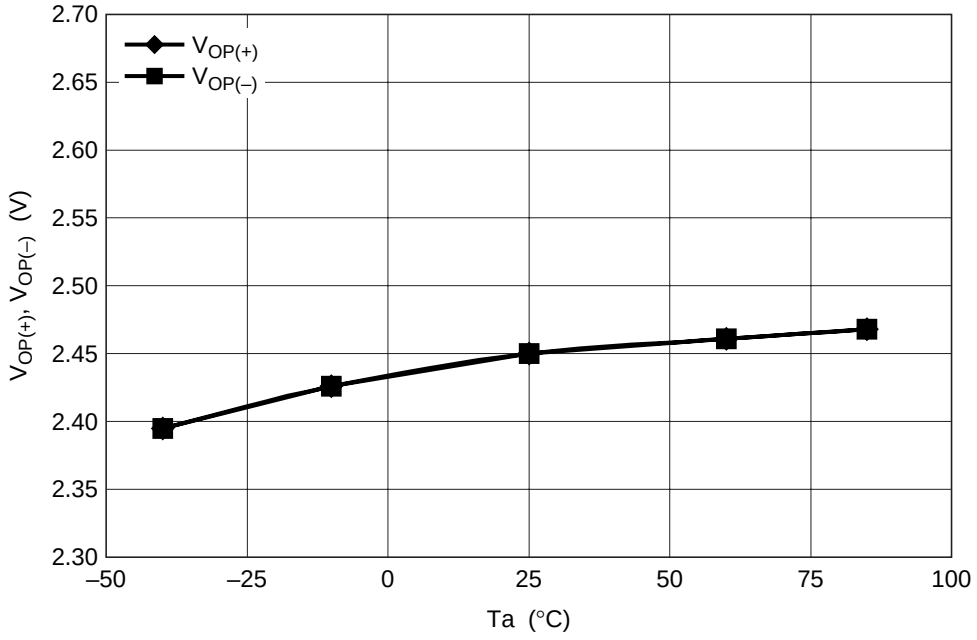

2.10
2.05
2.00
1.95
1.90
1.85
1.80
1.75
1.70
1.65
VIHS1
VILS1
VIHS1, VILS1 (V)
–50
–25
0
25
50
75
100
Ta (°C)

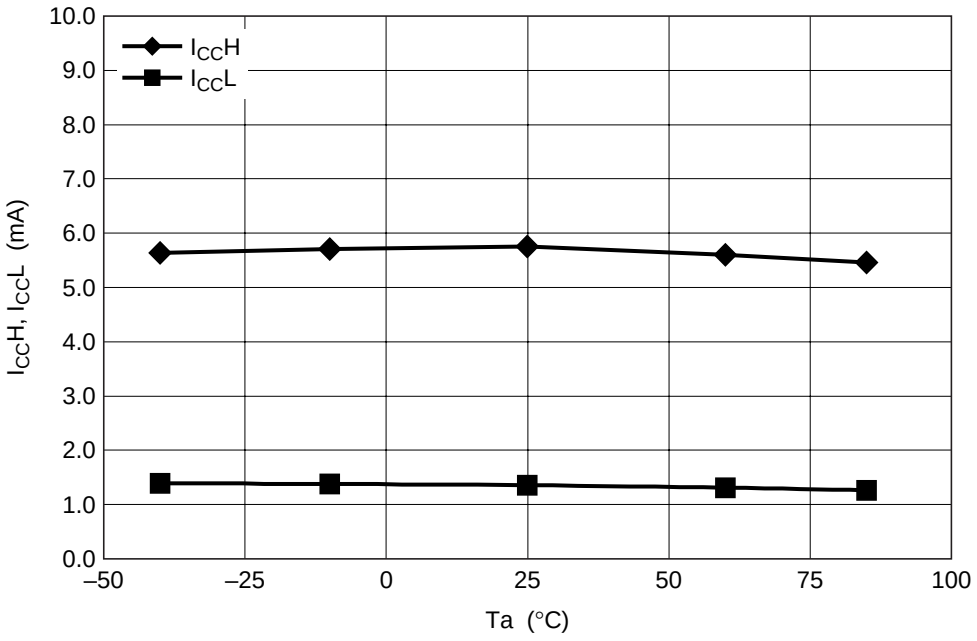

2.10
2.05
2.00
1.95
1.90
1.85
1.80
1.75
1.70
1.65
VIHS2
VILS2
VIHS2, VILS2 (V)
–50
–25
0
25
50
75
100
Ta (°C)

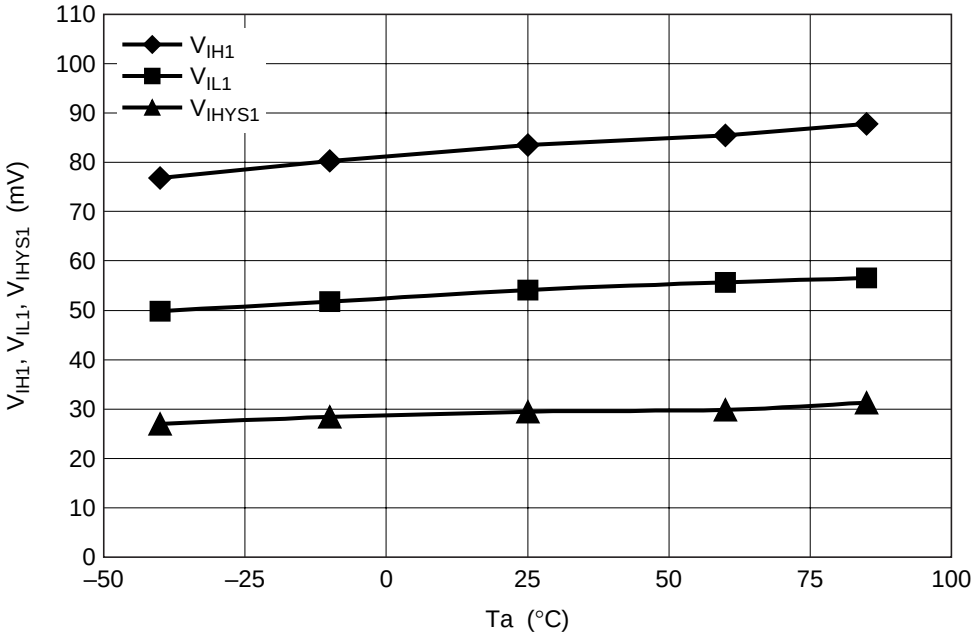

1.0
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
–50
–25
0
25
50
75
100
Ta (°C)
IIHS1, IILS1 (µA)
IIHS1
IILS1

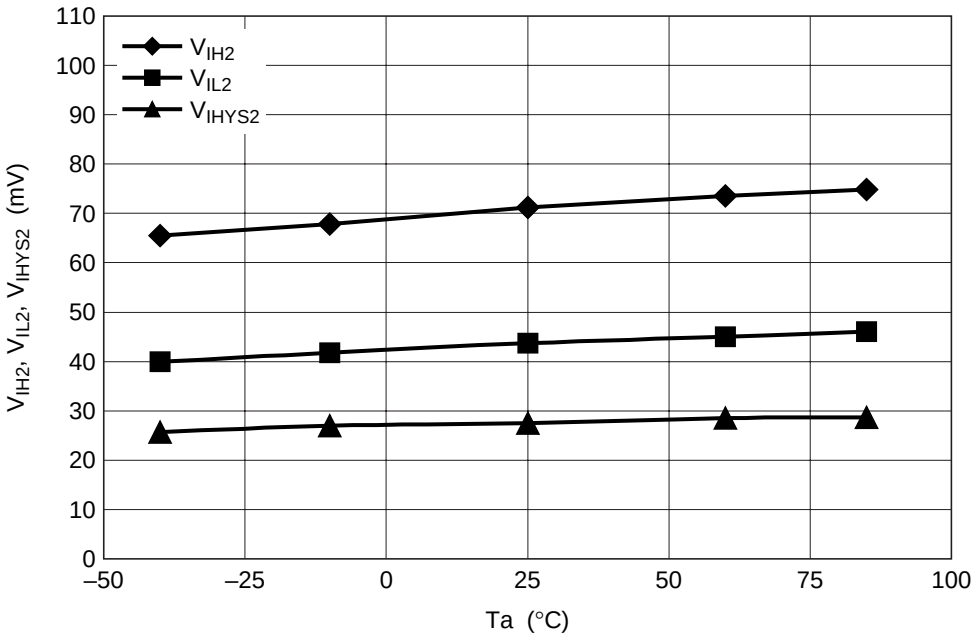

1.0
0.8
0.6
0.4
0.2
0.0
–0.2
–0.4
–0.6
–0.8
–1.0
–50
–25
0
25
50
75
100
Ta (°C)
IIHS2, IILS2 (µA)
IIHS2
IILS2

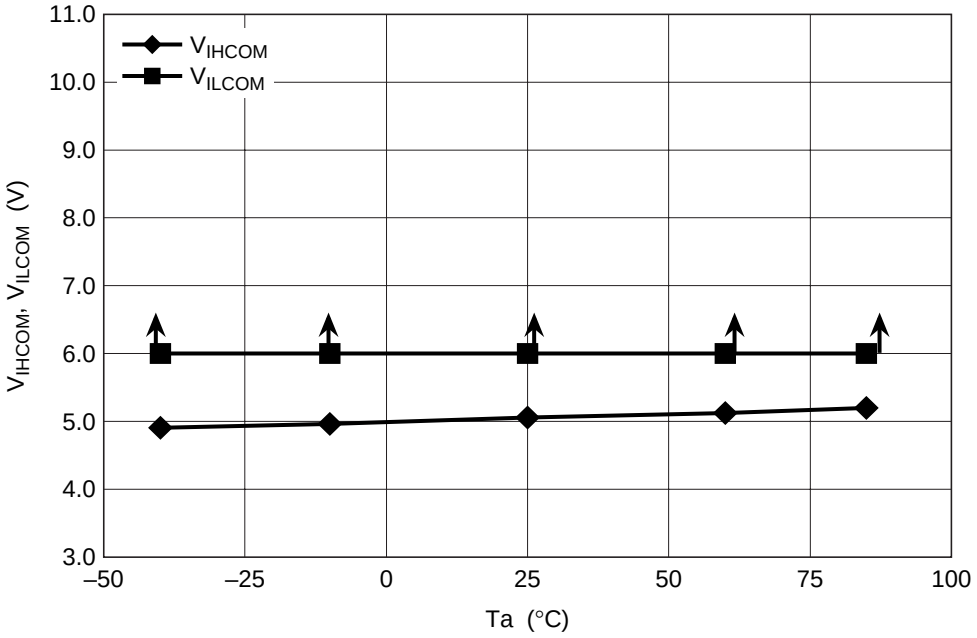

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
IOH
IOL
IOH (mA), IOL (µA)
–50
–25
0
25
50
75
100
Ta (°C)

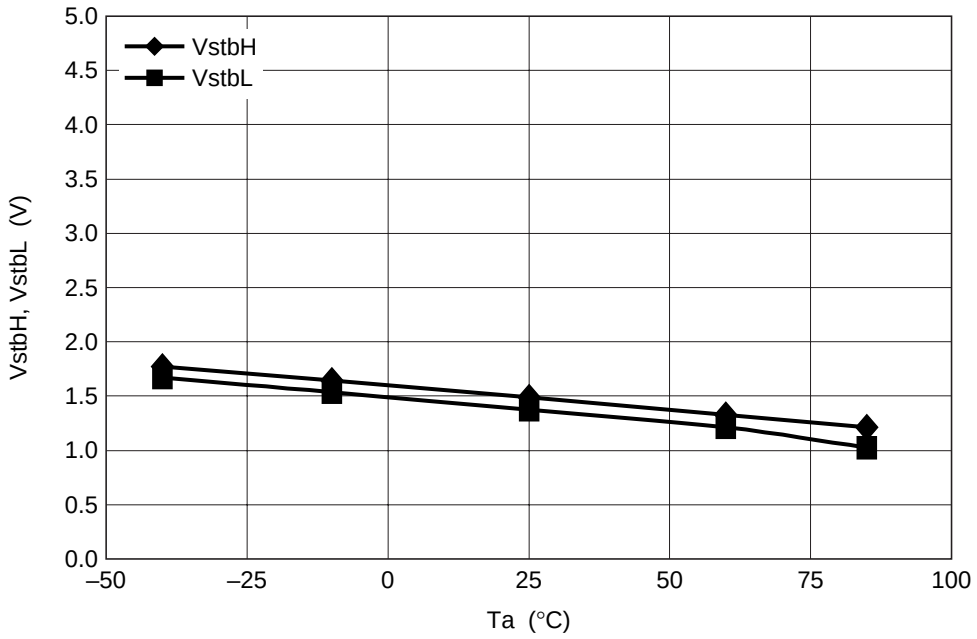

2.70
2.65
2.60
2.55
2.50
2.45
2.40
2.35
2.30
VOP(+)
VOP(–)
VOP(+), VOP(–) (V)
–50
–25
0
25
50
75
100
Ta (°C)

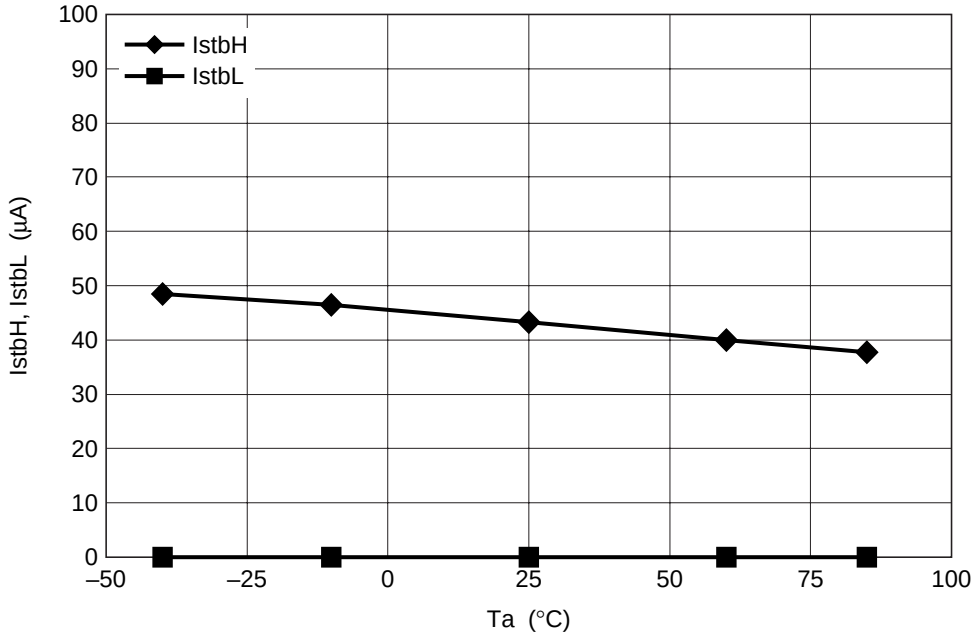

10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
ICCH
ICCL
ICCH, ICCL (mA)
–50
–25
0
25
50
75
100
Ta (°C)

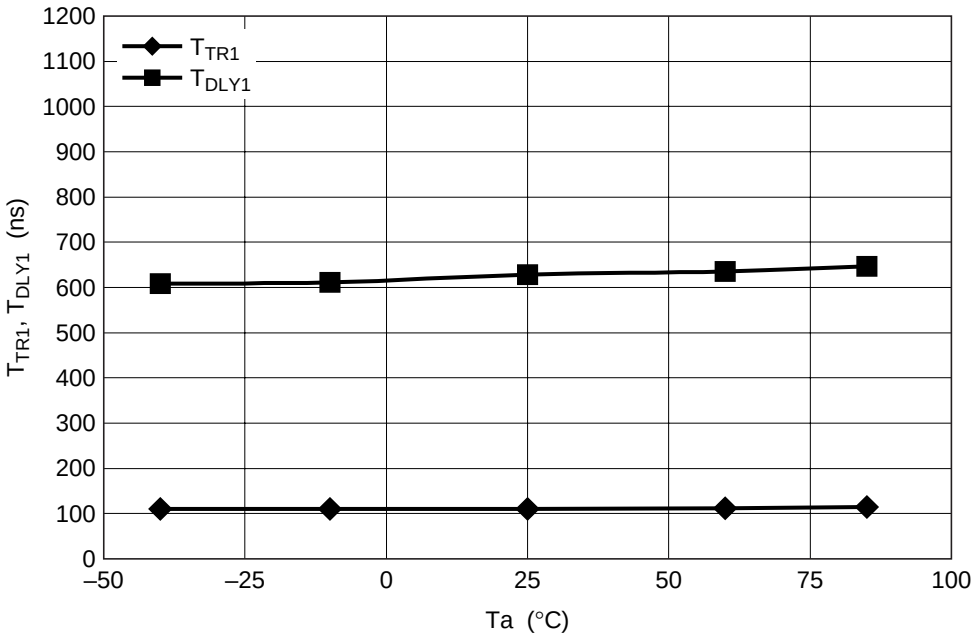

110
100
90
80
70
60
50
40
30
20
10
0
VIH1
VIL1
VIHYS1
VIH1, VIL1, VIHYS1 (mV)
–50
–25
0
25
50
75
100
Ta (°C)

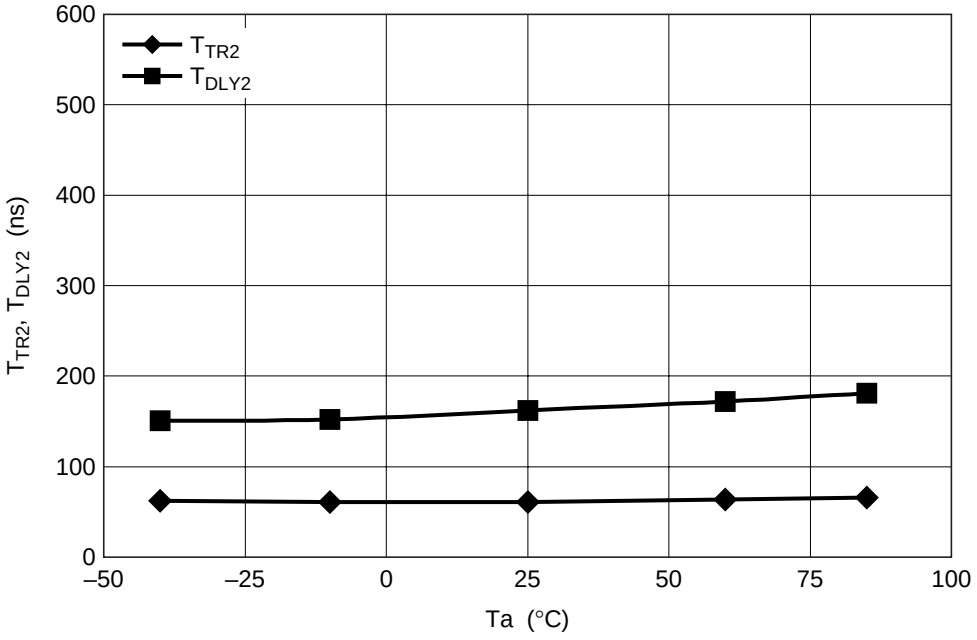

110
100
90
80
70
60
50
40
30
20
10
0
–50
–25
0
25
50
75
100
VIH2
VIL2
VIHYS2
VIH2, VIL2, VIHYS2 (mV)
Ta (°C)


11.0
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
–50
–25
0
25
50
75
100
VIHCOM
VILCOM
VIHCOM, VILCOM (V)
Ta (°C)


VstbH
VstbL
VstbH, VstbL (V)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
–50
–25
0
25
50
75
100
Ta (°C)

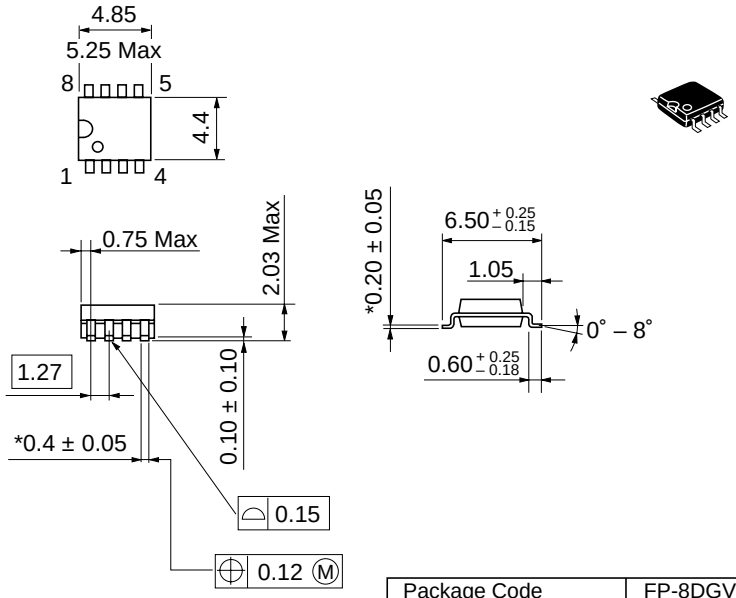

IstbH
IstbL
IstbH, IstbL (µA)
100
90
80
70
60
50
40
30
20
10
0
–50
–25
0
25
50
75
100
Ta (°C)


1200
1100
1000
900
800
700
600
500
400
300
200
100
0
$T_{TR1}$
$T_{DLY1}$
$T_{TR1}$, $T_{DLY1}$ (ns)
–50
–25
0
25
50
75
100
Ta (°C)


600
500
400
300
200
100
0
$T_{TR2}$
$T_{DLY2}$
$T_{TR2}$, $T_{DLY2}$ (ns)
–50
–25
0
25
50
75
100
Ta (°C)

## Package Dimensions

Unit: mm




*Dimension including the plating thickness

| | |
|---|---|
| Package Code | FP-8DGV |
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.10 g |

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