DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4534B
LSI
Real time 5-decade counter

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Real time 5-decade counter

HEF4534B
LSI

DESCRIPTION

The HEF4534B is a 5-decade ripple counter. The binary outputs of the decade counters are time-multiplexed by an internal scanner on four BCD outputs (O_0 to O_3). The selected decade is indicated by a logic HIGH on the appropriate digit select output (OS_0: units, 1; OS_1: tens, 10; OS_2: hundreds, 10^2; OS_3: thousands, 10^3; OS_4: ten thousands, 10^4).

The binary outputs (O_0 to O_3) and the select outputs ($\overline{OS_0}$ to $\overline{OS_4}$) are 3-state controlled via enable inputs $\overline{EO}$ and $\overline{EOS}$ respectively, allowing interface with other bus orientated devices. Cascading may be accomplished by using the carry out (TC). The counter is triggered by a LOW to HIGH transition on the decade clock (CPA) and is reset by a HIGH level on the master reset (MR). The scanner is triggered by a LOW to HIGH transition on the scanner clock (CPS) and is reset (select ten thousand counter) by a HIGH level on the scanner reset (MR_{SC}).

The counter can operate in four modes depending on the state of the mode select inputs (S_A, S_B). The error detector will detect an error when a positive edge on CPA is not accompanied by a negative edge on the error detector clock $\overline{CPE}$ or vice versa, within time limits adjusted by external capacitors connected to $C_{ext\,1}$ and $C_{ext\,2.}$ Three or more detected errors result in a HIGH level on the error output (OER). The error detector is reset by a HIGH level on MR.

Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times.

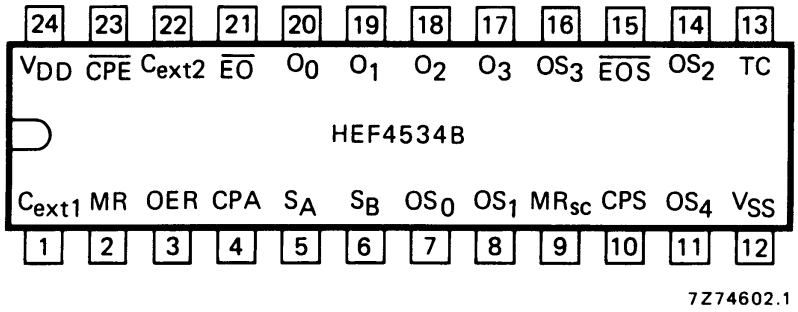


Fig.1 Pinning diagram.

HEF4534BP(N): 24-lead DIL; plastic (SOT101-1)
HEF4534BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
HEF4534BT(D): 24-lead SO; plastic (SOT137-1)
( ): Package Designator North America

PINNING

O_1 to O_3	BCD outputs
OS_0 to OS_3	digit select outputs
OER	error output
CPA	decade clock input
CPS	scanner clock input
$\overline{CPE}$	error detector clock input
S_A, S_B	mode select inputs
MR	master reset input
MR_{SC}	scanner reset input
TC	carry out

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

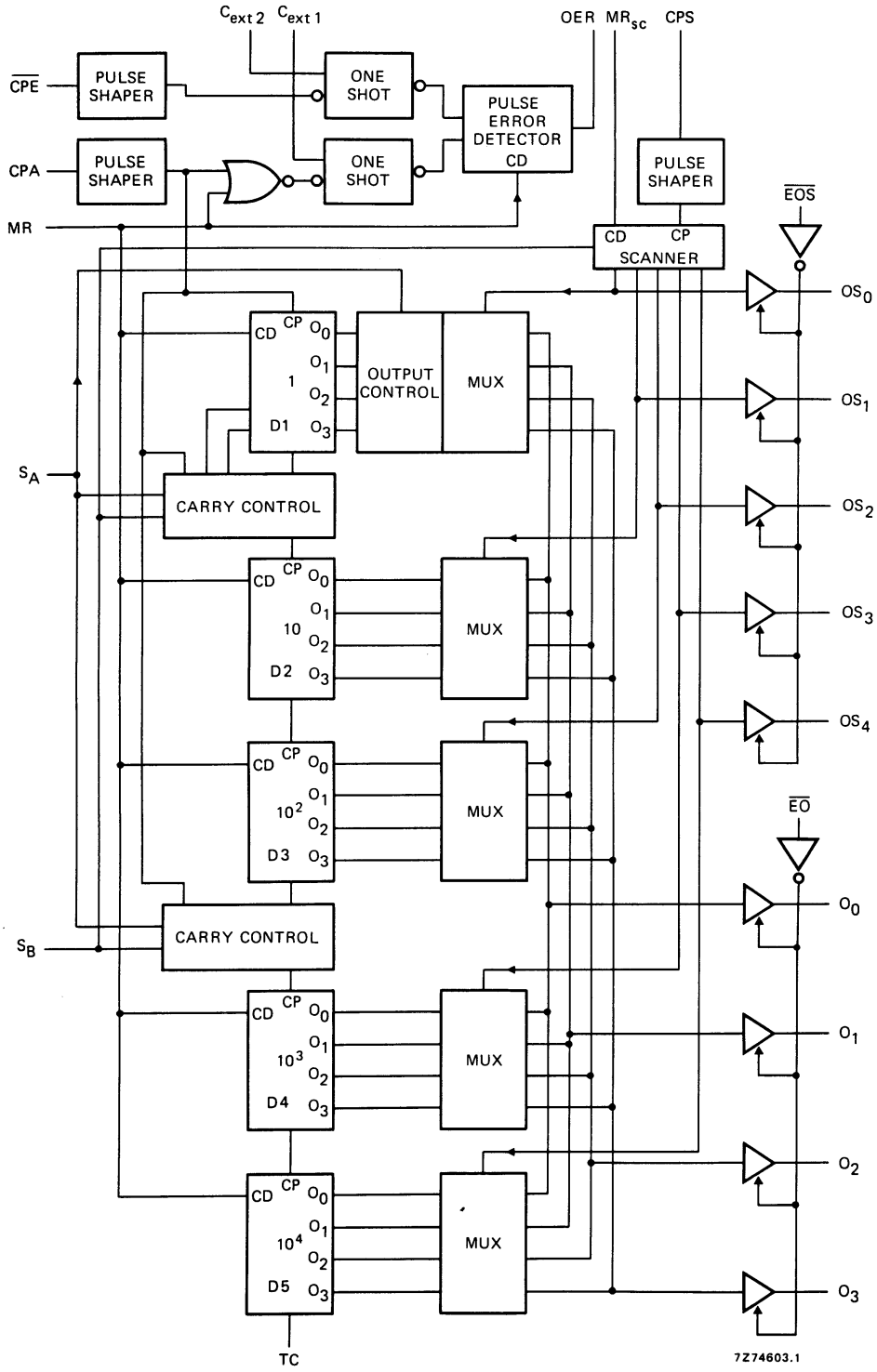


Fig.2 Functional block diagram.

MODE CONTROL FUNCTION TABLE

SELECT INPUTS		1ST DECADE OUTPUT	CARRY TO 2ND STAGE	CARRY TO 4TH STAGE	MODE
S_A	S_B				
L	L	normal count and display	at 9 to 0 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	5-decade counter
L	H	inhibited	input clock	input clock	test purposes: clock directly into stages 1, 2 and 4
H	H	inhibited	at 4 to 5 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter with ÷ 10 and round-off at front end
H	L	display counts: 3, 4, 5, 6, 7 = 5 8, 9, 0, 1, 2 = 0	at 7 to 8 transition of the 1st decade	at 9 to 0 transition of the 3rd decade	4-decade counter; ½-pence capability

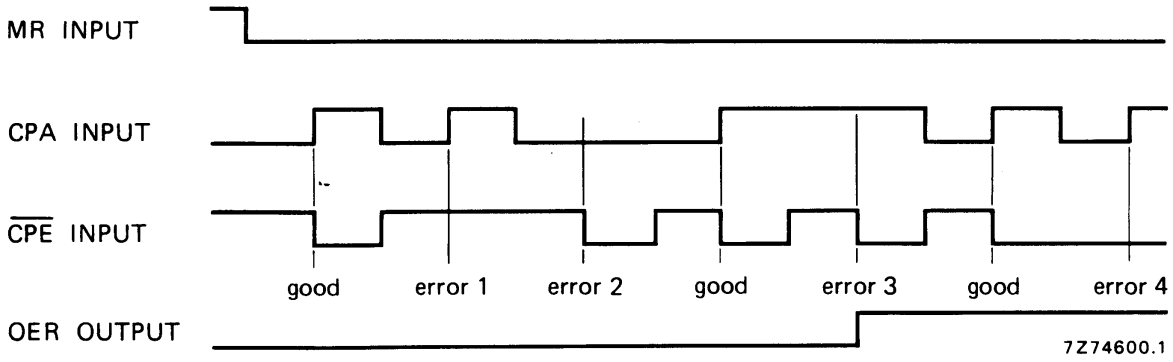


Fig.3 Error detection timing diagram.

The skew time is the time difference between the LOW to HIGH transition of CPA and the HIGH to LOW transition of $\overline{CPE}$ or vice versa (see Fig.4). The skew time is typically proportional to the external capacitor (C_{ext}) connected from C_{ext1} and C_{ext2} (pins 1 and 22) to V_{SS}. The error detector will count an error when a positive edge on the counter clock CPA is not succeeded by a negative edge on the error detector clock $\overline{CPE}$ within a skew time t_{SK1} (adjustable by C_{ext1} at pin 1). The same holds for a negative edge at $\overline{CPE}$ succeeded by a positive on CPA within a skew time t_{SK2} (adjustable by C_{ext2} at pin 22). If error detection is not needed, $\overline{CPE}$ must be either HIGH or LOW and no C_{ext} is applied. For further information see Fig.5.

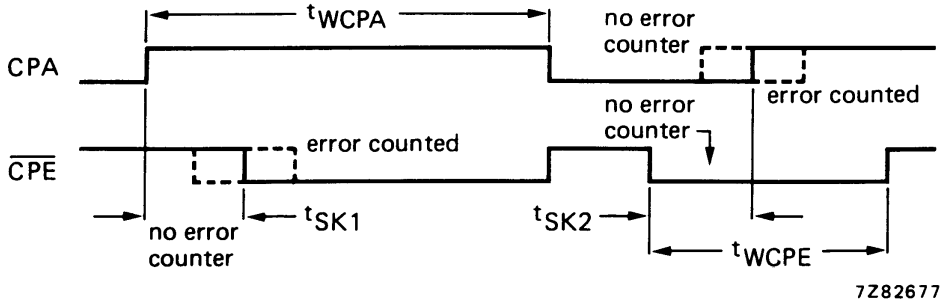
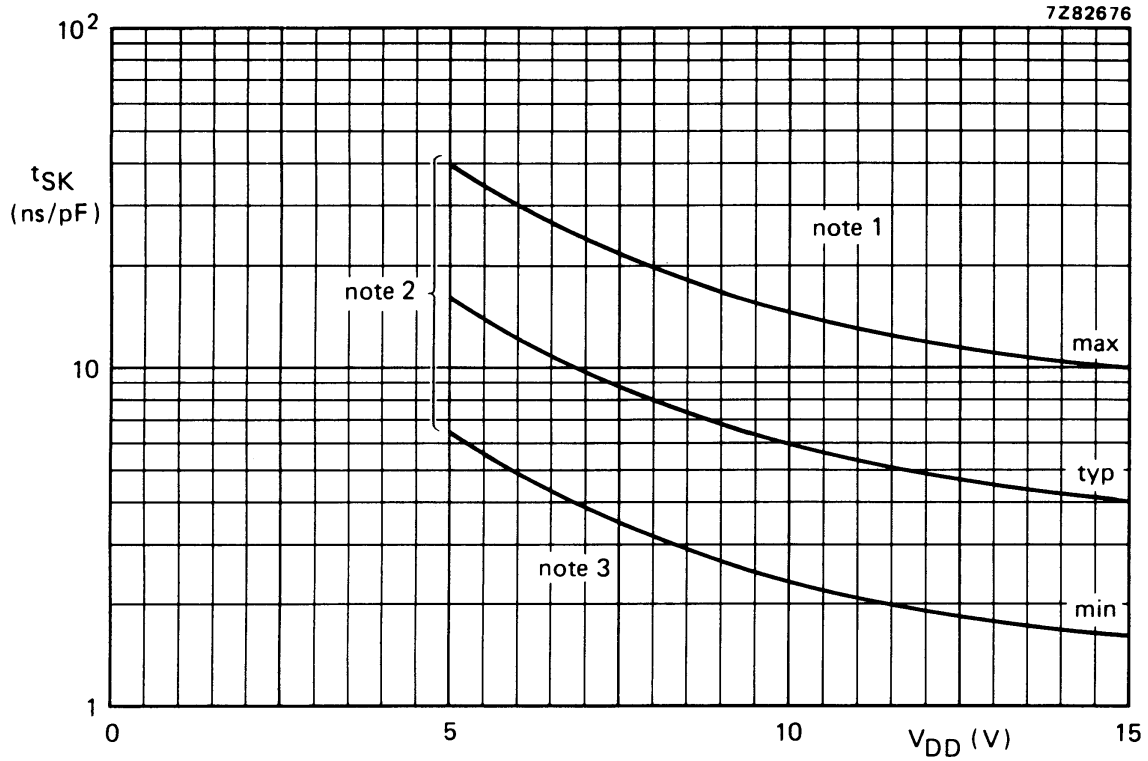


Fig.4 Skew times timing diagram; $t_{WCPA} > t_{SK1}$; $t_{WCPE} > t_{SK2}$.



Note 1: Skew in this area results in counted error.

Note 2: Skew in the area between max. and min. curves may or may not result in counted error.

Note 3: Skew in this area results in no error counted.

Fig.5 Typical clock skew as a function of the supply voltage. This graph is accurate for $C_{ext} \geq 100$ pF and $T_{amb} = 25$ °C.

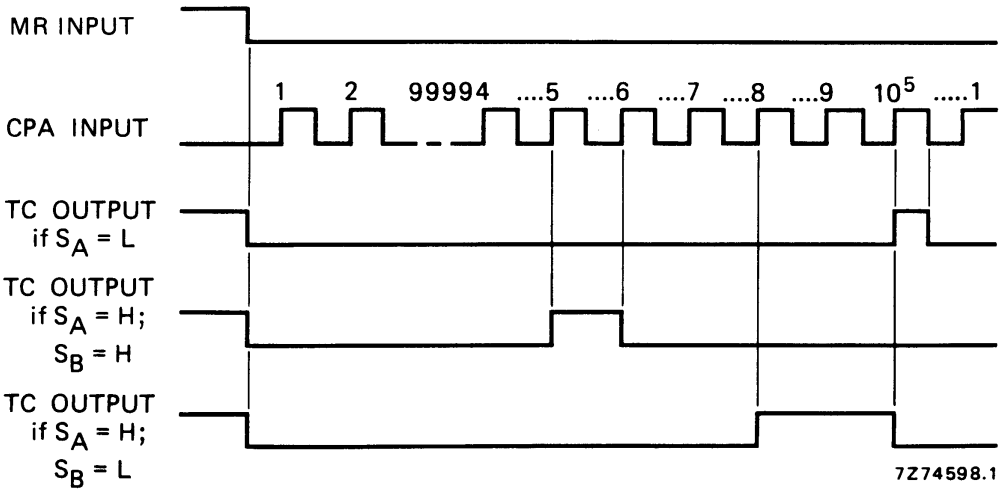
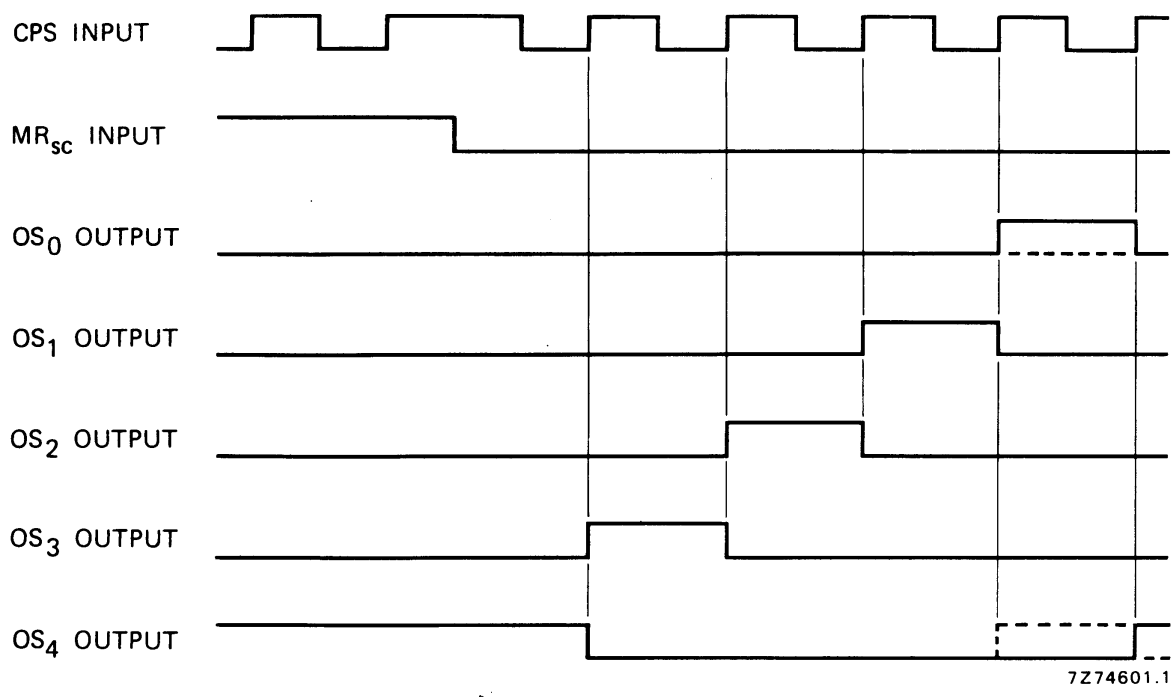


Fig.6 Carry timing diagram.



Note: If S_B = H, the 1st decade is inhibited and the cycle will be shortened to four stages (see dotted lines).

Fig.7 Scanner timing diagram.

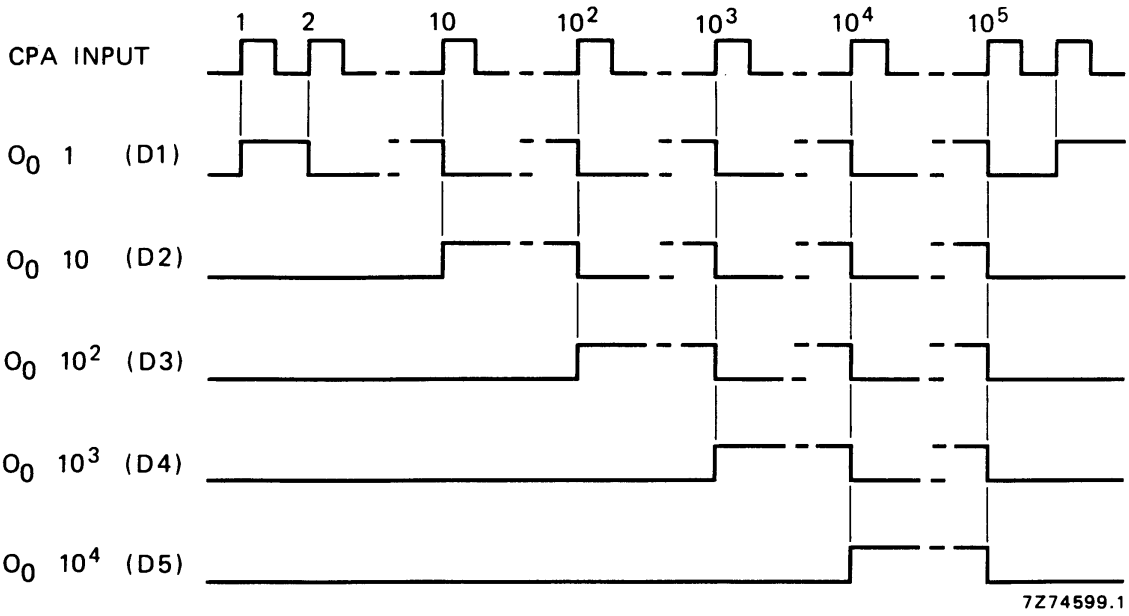


Fig.8 Counter timing diagram.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
CPA → O_n	5			300	600	ns	283 ns + (0,55 ns/pF) C_L
D1 selected	10	t_{PHL}		130	260	ns	119 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			95	190	ns	87 ns + (0,16 ns/pF) C_L
	5			240	480	ns	213 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		100	200	ns	89 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
CPA → O_n	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
D5 selected	10	t_{PHL}		230	460	ns	219 ns + (0,23 ns/pF) C_L
HIGH to LOW	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
	5			550	1100	ns	523 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		230	460	ns	219 ns + (0,23 ns/pF) C_L
	15			170	340	ns	162 ns + (0,16 ns/pF) C_L
CPA → TC	5			420	840	ns	393 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		190	380	ns	179 ns + (0,23 ns/pF) C_L
	15			140	280	ns	132 ns + (0,16 ns/pF) C_L
MR → O_n	5			200	400	ns	173 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
MR → OER	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPS → O_n	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	190	ns	84 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
CPS → OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
CPS → OS_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow O_n$;	5			30	60	ns	
$\overline{EOS} \rightarrow OS_n$	10	t_{PHZ}		25	50	ns	
HIGH	15			20	40	ns	
	5			40	80	ns	
LOW	10	t_{PLZ}		25	50	ns	
	15			20	40	ns	
Output enable times							
$\overline{EO} \rightarrow O_n$;	5			35	70	ns	
$\overline{EOS} \rightarrow OS_n$	10	t_{PZH}		20	40	ns	
HIGH	15			15	30	ns	
	5			50	100	ns	
LOW	10	t_{PZL}		25	50	ns	
	15			15	30	ns	
Minimum clock pulse	5		70	35		ns	
width; CPA, CPS	10	t_{WCPH}	40	20		ns	
HIGH	15		30	15		ns	
Minimum reset pulse	5		90	45		ns	
width; MR, MR_{sc}	10	t_{WMRH}	60	30		ns	
HIGH	15		40	20		ns	
Recovery time	5		120	60		ns	
for MR	10	t_{RMR}	60	30		ns	
	15		50	25		ns	
Recovery time	5		60	30		ns	
for MR_{sc}	10	t_{RMR}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Maximum clock	5		2,5	5	MHz	
pulse frequency	10	f_{max}	6	12	MHz	
CPA and CPS	15		8	16	MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$1\,100\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$4\,800\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)(1)	15	$12\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load cap. (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

Note

1. $C_{ext} = 0$.

APPLICATION INFORMATION

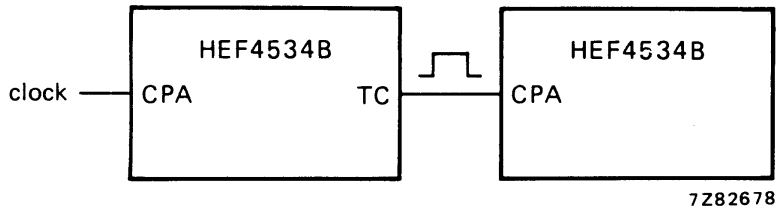


Fig.9 Two HEF4534B ICs connected for cascade operation. TC is HIGH for a single clock period when all five BCD decades go to zero. TC also goes HIGH when MR is applied.

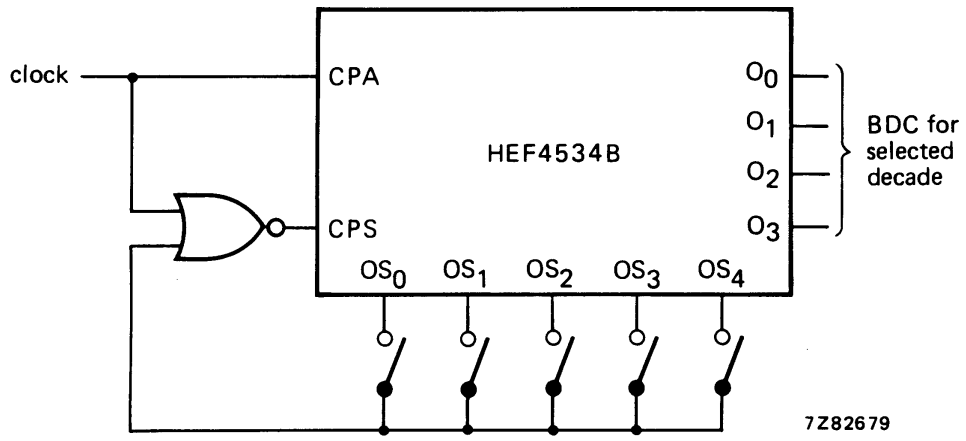


Fig.10 Forcing a decade to the O_n outputs. When the O_n outputs of a given decade are required, this configuration will lock-up the selected decade within four clock cycles. The select line feed back may be hardwired or switched.