

HG61H SERIES

The HG61H series is a master slice CMOS gate array using 2-layer metal interconnect technology. This series has six master chips with wide range of gate count of 448 to 2560, and of I/O terminal count of 54 to 108. These chips can replace not only CMOS logics but also TTL logics thanks for their high speed of 2.0 ns typ and compatibility of input and output buffers at TTL/CMOS level.

LSI design is fully automated by DA (Design Automation) system and custom LSI is developed based on logic diagram and test pattern from customer in a short time and with reasonable cost. EWS (LOGICIAN/DAISY) interface is also available.

■ FEATURES

● Fast operation

Internal gate (2-input NAND, FO=3, AL=3mm)

..... 2.0 ns typ

Input buffer (FO=3, AL=3mm) 7.7 ns typ

Output buffer ($C_L=50\text{pF}$) 9.5 ns typ

Memory access time (HD61MM) 40 ns typ

● Low power dissipation

At 10MHz operation (Internal gate) . . . 175 μW /gate typ

● Abundant input and output configuration

Allocation of all pins except power supply pins to input/output/input-output common

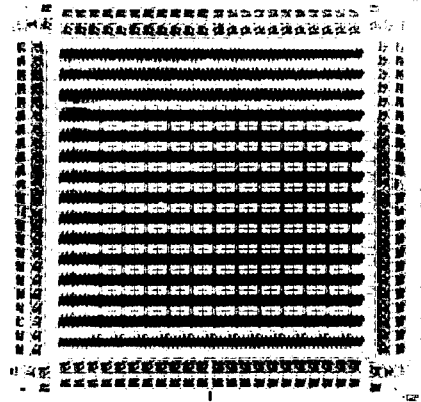
Output can be CMOS/open drain/3-state

● Oscillator, Schmitt input available

● Memory on-chip

Flexibility of memory capacity and word organization

Selection of single port/dual port memory



● Wide operation temperature range

-20 to +75°C

● Wide package selection

Especially plastic packages with high pin count

..... DILP64/FPP100

● Powerful design support

User-Defined-Macro

Test pattern evaluation with fault simulator

Design support at local Design Center

● Quick turn around time and reasonable development cost

■ LINE UP

		Δ HG61H04	HG61H06	HG61H09	HG61H15	HG61H20	Δ HG61H25
Gate count		448	660	968	1560	2010	2560
I/O count (max)		54	66	80	84	96	108
RAM on chip		8 ^b × 8 ^w	12 ^b × 12 ^w	16 ^b × 16 ^w	16 ^b × 24 ^w	16 ^b × 28 ^w	16 ^b × 32 ^w
Available I/O count	DP 28	Δ 26	—	○26	—	—	—
	DP 40	Δ 38	○38	○38	○38	○38	Δ 38
	DP 64	Δ 52	○60	○60	○60	○60	Δ 60
	FP 64	Δ 52	Δ 60	—	—	—	—
	FP 80	—	○64	○76	○76	Δ 76	—
	FP 100	—	—	—	—	Δ 94	Δ 96

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Δ : Under development

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	$-0.3 \sim +6.7$	V
Terminal Voltage	V_T	$-0.3 \sim V_{CC}+0.3$	V
Output Current	per one output	I_O	$-8 \sim +8$ mA
	total	I_{OT}	$-40 \sim +40$ mA
Operating Temperature	T_{opr}	$-20 \sim +75$	°C
Storage Temperature	with Bias	T_{bias}	$-20 \sim +85$ °C
	without Bias	T_{stg}	$-55 \sim +125$ °C

Note) Permanent damage may occur if maximum ratings are exceeded.

Normal operation should be under recommended operating condition, that is

$$GND \leq (V_{in} \text{ and/or } V_{out}) \leq V_{CC}$$

If these conditions are exceeded, it could affect reliability of LSI.

* With respect to GND.

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_a = -20$ to 75°C)

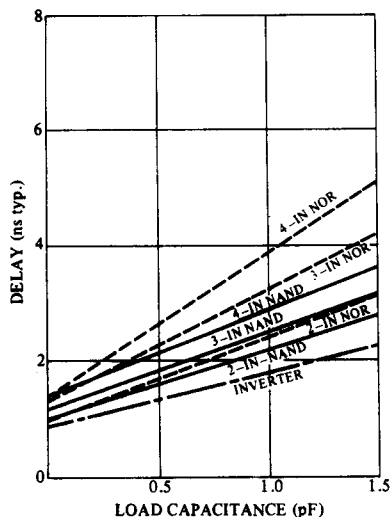
Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Voltage (TTL Level)	V_{IHT}		2.2	—	$V_{CC}+0.3$	V
	V_{ILT}		-0.3	—	0.8	V
Input Voltage (CMOS Level)	V_{IHC}		3.5	—	$V_{CC}+0.3$	V
	V_{ILC}		-0.3	—	1.5	V
Output Voltage	V_{OH}	$I_{OH} = -2\text{mA}$	3.5	—	—	V
	V_{OL}	$I_{OL} = 5\text{mA}$	—	—	0.5	V
Input Leakage Current	I_{LI}		—	—	1	μA
Output Leakage Current	I_{LO}	at high impedance	—	—	1	μA
Gate Delay	Internal	t_{pd} 2 input NAND, FO=3, A ℓ =3mm	—	2.0	—	ns
	Input Buffer	t_{pd} FO=3, A ℓ =3mm	—	7.7	—	ns
	Output Buffer	t_{pd} $C_L=130\text{pF}$	—	19	—	ns
Power Dissipation	I_{CC}	Internal 2 input NAND 10MHz	—	35	—	$\mu\text{A}/\text{Gate}$

■ TERMINAL CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

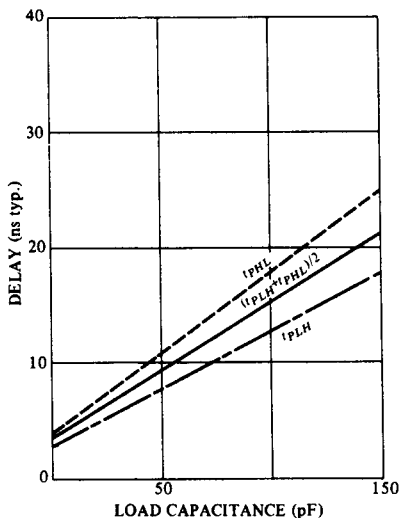
Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Terminal Capacitance	C_T	$V_{in}=0\text{V}$	—	—	12.5	pF

* This parameter is sampled and not 100% tested.

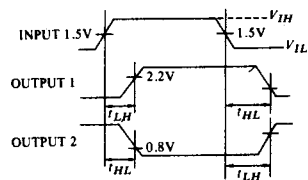
■ INTERNAL GATE DELAY vs LOAD (REFERENCE)



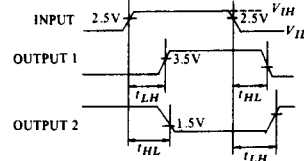
■ OUTPUT BUFFER DELAY vs LOAD (REFERENCE)



■ DELAY TIME



TTL INTERFACE



CMOS INTERFACE

■ DEVELOPMENT FLOW

Development flow of gate arrays is shown below. Logic design and test vectors development are done by users. These are fed to a computer which performs logic simulation. The machine drawn logic diagram is checked by the user. The test pattern is evaluated by the fault simulator then automatic layout is done and precise delay simulation with wiring information. After these design check, PG tape and test tape are generated. Sample production takes very short time because it needs only metal wiring on inventory wafers.

Finished wafers are probed with test vectors from users, then

assembled, tested again and shipped.

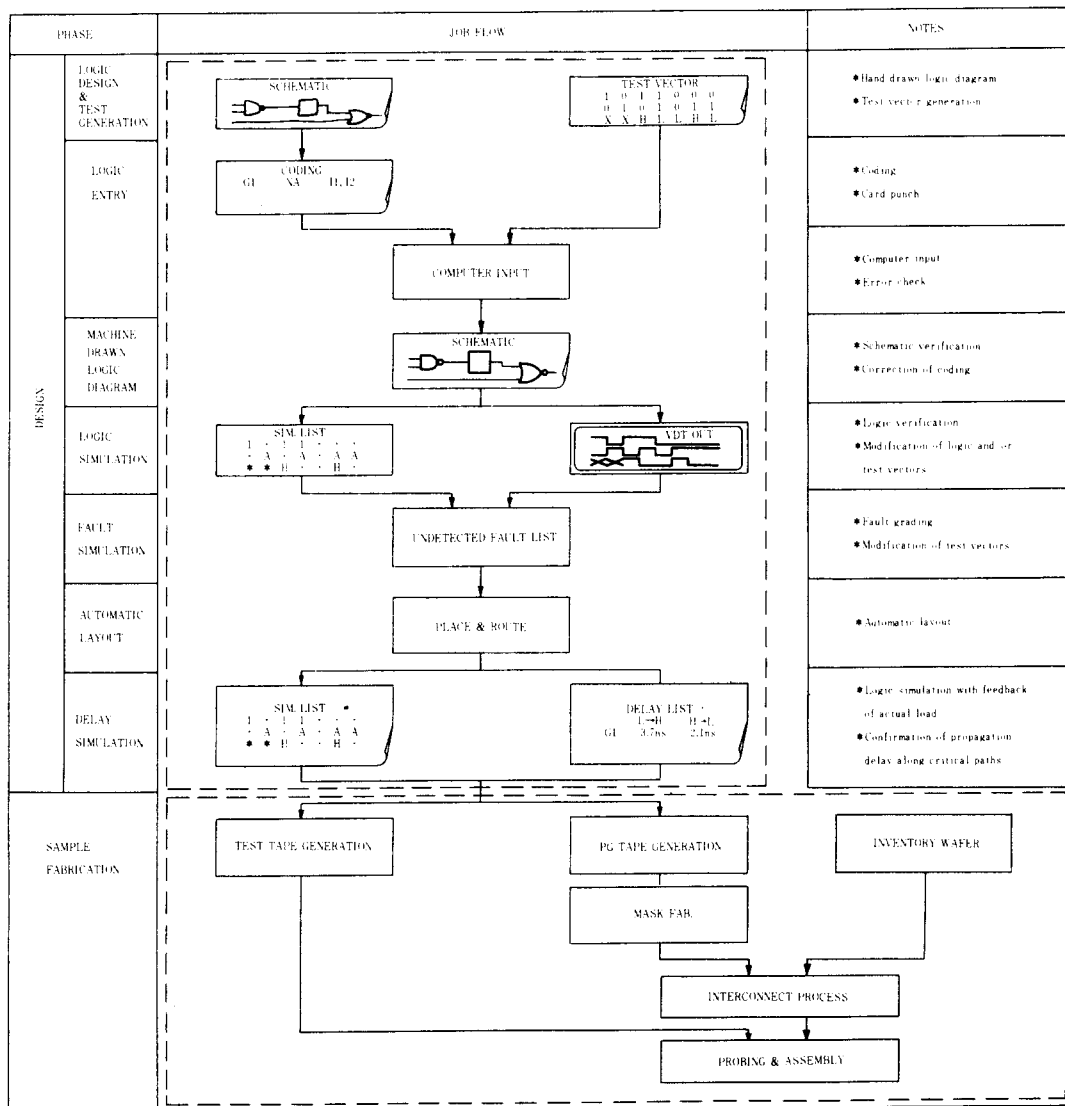
There are two standard interfaces between a user and Hitachi, Namely:

(1) Logic diagram interface

The user supplies logic diagram and test vectors to Hitachi. Further jobs are done by Hitachi except for some confirmation by the user.

(2) Logic file interface

The user performs simulations by himself at Hitachi Design Center and supplies Hitachi with complete logic file.

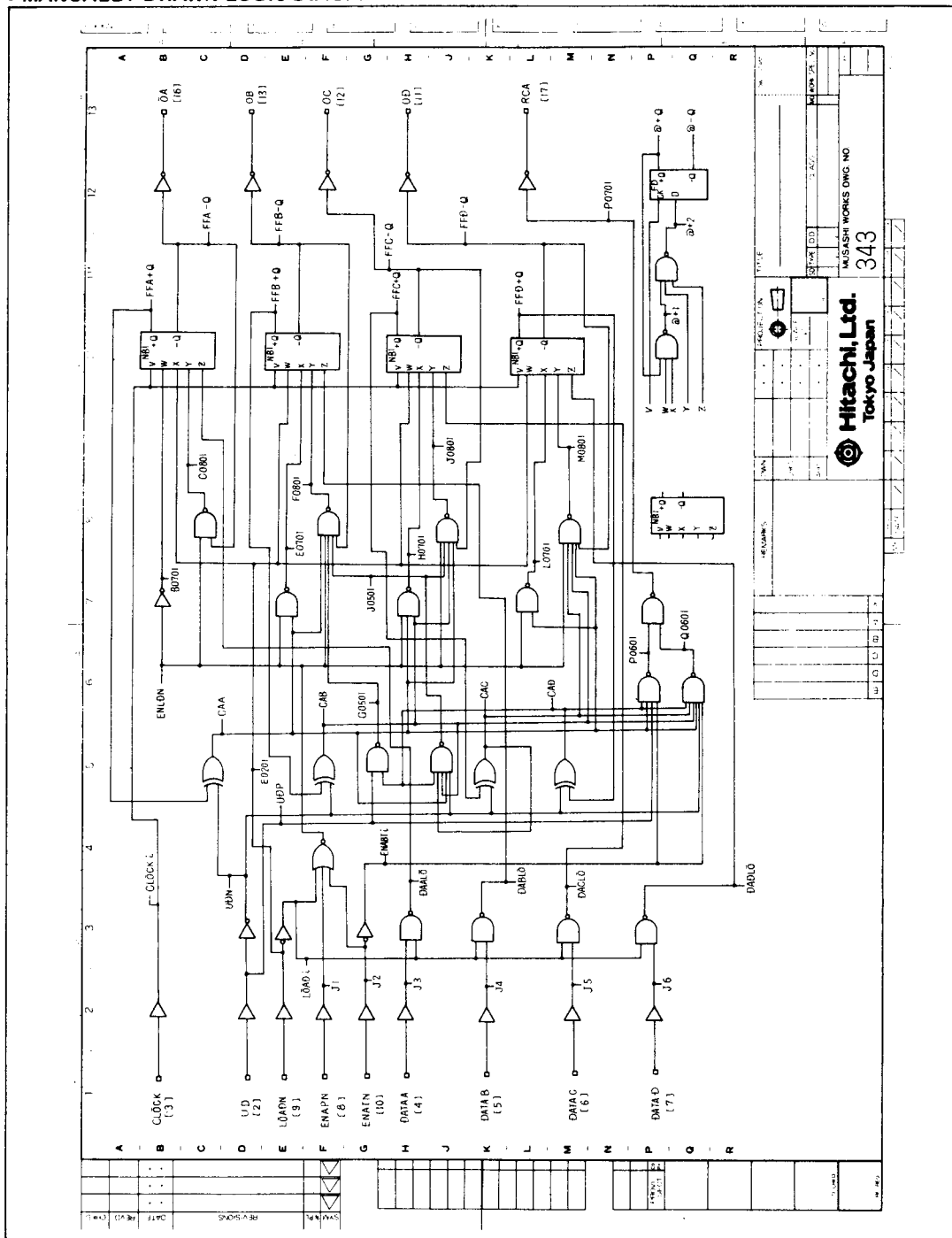


■ HOW TO WRITE LOGIC DIAGRAM

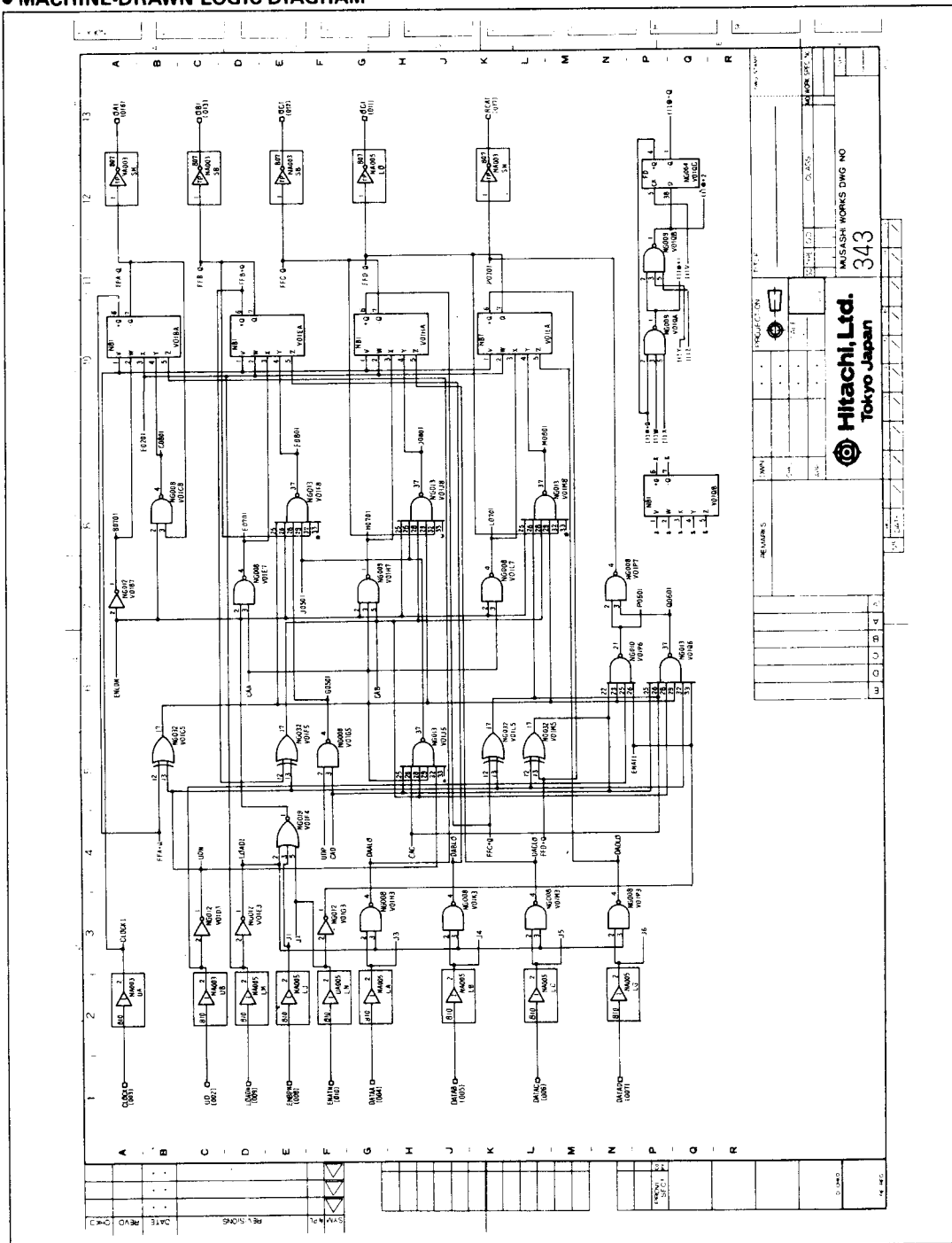
No.	Item	Rules	Examples										
1.	Forms	Size A-3 forms supplied by Hitachi											
2.	Logic symbol	(1) Draw logic diagram with exactly the same symbols as shown in Macrocell Library including function name, terminal name and the size. (2) The internal symbol surrounded by dotted line can be omitted but macro function name must be described and the position of terminal can not be changed instead. (3) The template shall be provided. (4) 3-state gate will occupy 2 blocks in the drawing form.	Function name FDPCL CK +Q Pin function name D - Q PR CL Open terminal (# may be omitted) NRA23										
3.	Characters	(1) 2 to 3mm higher or larger alphabets, +, -, 0 to 9 in total 38 characters. (2) The letters shown in the table must be written as in the bottom column.	<table><tr><td>Alphabet</td><td>I</td><td>J</td><td>O</td><td>U</td></tr><tr><td>Script</td><td>i</td><td>j</td><td>ō</td><td>u</td></tr></table>	Alphabet	I	J	O	U	Script	i	j	ō	u
Alphabet	I	J	O	U									
Script	i	j	ō	u									
4.	Signal name	(1) Name all pins of LSI within 2 to 5 letters beginning with alphabet (2) For the user's convenience, it is not necessary to name all internal nodes except those which come and go over multi pages. (3) Naming the internal nodes (A) Name macros within 2 to 5 letters beginning with alphabet (B) Memory macros should be named within 3 letters (c) Tri-state gate should be named within 4 letters (d) Output signal name of a macro which has only one output terminal is macro name itself. (e) Output signal names of a macro which has two or more terminals are composite of macro name and terminal name. (f) Combination of location and page number of symbol makes it easy to give name to macros. ex. B0205 (Symbol in page 05, location B02)	add terminal name LD G +Q XYZ +Q D -Q XYZ -Q customer specifies this part EN EN Not Applicable EN EN Correct example										
5.	UD-MACRO	The User can define his own macro's. (1) Give name within 4 letters beginning with @ + or @ - to macros which compose UD macro. (2) Give name within 2 letters beginning with alphabet to input terminals. (3) Give function name to UD macros within 5 letters beginning with an alphabet. (4) Define output terminals of UD macro. Then output terminal names will be signal name without @. (5) Now UD-MACRO's can be used in a same way as macros in cell library. Width of UD-MACRO's should be symbol No. A size as shown in the cell library. Height can be determined in proportion to the number of input or output terminals. A B C @+S @-CO UD macro function name Terminal name A B C ADDER +S -CO											

No.	Item	Rules	Examples
5.	Signal line	(1) LSI input/output signal must be shown by and LSI pin number in [1]. (2) Up to three lines can be connected to one junction point.	
6.	Symbol layout	(1) A signal should flow from left to right. (2) No symbol is allowed to be placed in the first, the 13th column and in the R row. (Shadow area) (3) Keep at least one spacing row every four adjacent occupied rows to keep area for wiring. (4) Keep at least one spacing column in every other column, to assure indication of signal names.	
7.	Cross reference	(1) When signal line extends to another sheet of machine drawing, following informations are indicated automatically. K...15, B-10 ↳ logic location to be connected ↳ page number of logic diagram to be connected ↳ terminal specification of signal destination K Sink S Source Z 3-state output N 3-state control	

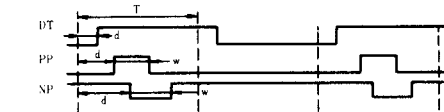
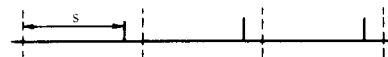
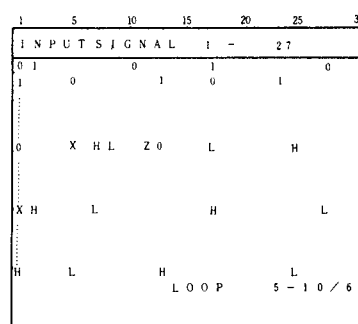
● MANUALLY-DRAWN LOGIC DIAGRAM



● MACHINE-DRAWN LOGIC DIAGRAM

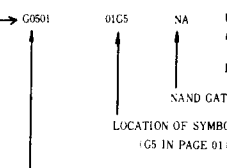


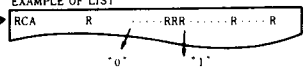
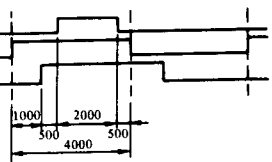
■ DESTINATION OF TEST VECTORS

No.	Item	Rules	Examples																																												
1.	Limitation of timing: $T \geq 150$ $d \geq 20$ $W \geq 50$ $S \geq 20$ $T-(d+w) \geq 40$ $T-S \geq 30$	1. 3 different format of input signal  2. 1 strobe timing for output 	<table> <tr> <th colspan="2">Test Rate</th><th colspan="3">300 ns</th></tr> <tr> <th></th><th>Timing No.</th><th>Format</th><th>d(ns)</th><th>w(ns)</th></tr> <tr> <td rowspan="6">Input</td><td>I₀</td><td>DT</td><td>—</td><td>—</td></tr> <tr> <td>I₁</td><td>DT</td><td>20</td><td>—</td></tr> <tr> <td>I₂</td><td>PP</td><td>50</td><td>150</td></tr> <tr> <td>I₃</td><td>NP</td><td>70</td><td>100</td></tr> <tr> <td>I₄</td><td></td><td></td><td></td></tr> <tr> <td>I₅</td><td></td><td></td><td></td></tr> <tr> <td>Output</td><td>O₁</td><td colspan="3">250 ns</td></tr> </table> [Notes] 1. Number of input timing pulses: up to 7. 2. I₀ must be DT format with d = 0.	Test Rate		300 ns				Timing No.	Format	d(ns)	w(ns)	Input	I ₀	DT	—	—	I ₁	DT	20	—	I ₂	PP	50	150	I ₃	NP	70	100	I ₄				I ₅				Output	O ₁	250 ns						
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Output	O ₁	250 ns																																													
2.	Test Patterns	(1) Specify signal order. iT = input (TTL Level) iC = input (CMOS Level) iT$\bar{O}$ = I/O (TTL Level) iC$\bar{O}$ = I/O (CMOS Level) $\bar{O}$T = output OZ = 3-state output $\bar{O}$DN = open drain output (2) Describe test pattern with following expression. Horizontal axis shows time. <table> <tr> <th>Input</th><th>DT format</th><th>0,1</th></tr> <tr> <td></td><th>PP format</th><th>0,1</th></tr> <tr> <td></td><th>NP format</th><th>0,1</th></tr> <tr> <th>Output</th><td colspan="2">H, L, Z, X</td></tr> </table> (Note 1) In PP and NP format 1 shows an active pulse. (Note 2) Z high impedance X indefinite or masked (Note 3) Blank can be applied for no signal change. (3) When the same vectors are repeated, describe like the following next to signal block. Nesting of LOOP is not allowed. - To repeat whole input block input signal block LOOP N - To repeat specified columns input signal block LOOP S1-e1/N1, S2-e2/N2 N : number of repeat Sn : start column of repeat en : end column of repeat	Input	DT format	0,1		PP format	0,1		NP format	0,1	Output	H, L, Z, X		<table> <tr> <th>Signal name</th><th>I/$\bar{O}$ Format</th><th>Pin No.</th><th>Timing</th></tr> <tr> <td>INP-1</td><td>iT</td><td>15</td><td>I₁</td></tr> <tr> <td>INP-2</td><td>iC</td><td>7</td><td>I₃</td></tr> <tr> <td>:</td><td></td><td></td><td></td></tr> <tr> <td>BUS-1</td><td>iT$\bar{O}$</td><td>41</td><td>I₀</td></tr> <tr> <td>:</td><td></td><td></td><td></td></tr> <tr> <td>OUT-1</td><td>$\bar{O}$T</td><td>22</td><td></td></tr> <tr> <td>:</td><td></td><td></td><td></td></tr> </table> [Notes] 1. Signal name order may be free 2. BUS-1 input timing is I₀ and output strobe timing is O.  [Notes] 1-27 in the line beginning with INPUT SIGNAL shows the valid columns in the following data. When these figure are omitted, 1 to 40 columns are regarded valid.	Signal name	I/ $\bar{O}$ Format	Pin No.	Timing	INP-1	iT	15	I ₁	INP-2	iC	7	I ₃	:				BUS-1	iT $\bar{O}$	41	I ₀	:				OUT-1	$\bar{O}$ T	22		:			
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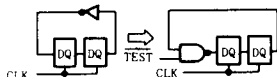
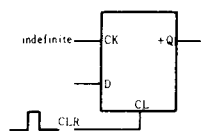
No.	Item	Rules	Examples
3.	Fault detection rate	Fault detection rate of test vectors shall be as high as possible (final target $\geq 95\%$) because it is used in final testing of products. Furthermore, undetected fault by the test vectors is strongly suggested to be checked in the system test at the user's assembly line.	
4.	Limitation of test vectors	(1) Up to 10 sets of test vectors (2) Up to 4000 test cycles after expanding the LOOP's in a set of test vectors (3) Up to 4000 steps in total for all sets of test vectors (LOOP is counted as 1 time.) (4) Up to 100ms test time	

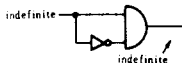
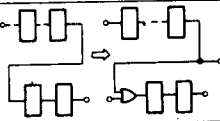
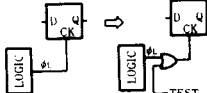
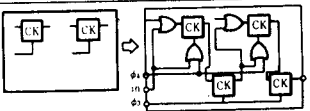
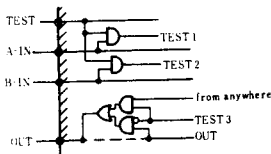
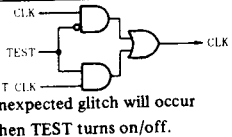
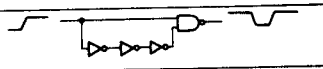
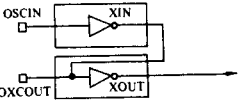
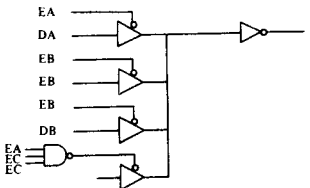
■ EXAMPLE OF LOGIC DESCRIPTION

Schematic description	*1 HG61H09B01 HG61H09	TRANS TYPE	FP80B0	Device type, master type package
	NB1 @+1 @+2 @ 01Q08 01Q10 01Q11 01Q12 BLOCK NA NA FD BEND V,W,X,Y,Z @+Q,W,X @+1,Y,Z V,@+2 @+Q,@-Q			UD-macro definition
	UP CLOCK DATAA DATAB DATAC DATAD ENAPN LOADN ENATN OD OC OB OA RCA 02 INPUT 03 INPUT 04 INPUT 05 INPUT 06 INPUT 07 INPUT 08 INPUT 09 INPUT 10 INPUT 11 OUTPUT 12 OUTPUT 13 OUTPUT 16 OUTPUT 17 OUTPUT			Description of I/O terminal including pin assignment. → LOADN is an input pin located at pin 9 of the package.
	CLOCK1 UDP E021 J1 J2 J3 J4 J5 J6 QA1 QB1 OC1 OD1 RCA1 UDN LOADI ENATI B0701 DAALO DABLO DACLO DADLO G0501 E0701 L0701 P0701 C0801 H0701 P0601 ENLND J0501 Q0601 F0801 J0801 M0801 CAA CAB CAC CAD FFA FFB FCC FFD 01B2 IT 01D2 IT 01E2 IT 01F2 IT 01G2 IT 01H2 IT 01K2 IT 01M2 IT 01P2 IT 01B12 OT 01D12 OT 01F12 OT 01H12 OT 01L12 OT 01D3 OT 01E3 NA 01G3 NA 01B7 NA 01H3 NA 01K3 NA 01M3 NA 01P3 NA 01G5 NA 01E7 NA 01L7 NA 01P7 NA 01C8 NA 01H7 NA 01P6 NA 01F4 NR 01J5 NA 01Q6 NA 01F8 NA 01J8 NA 01M8 NA 01C5 EOR 01F5 EOR 01L5 EOR 01M5 EDR 01B10 NB1 01E10 NB1 01H10 NB1 01L10 NB1 IT UD LOADN ENAPN ENATN DATAA DATAB DATAC DATAD FFA-Q FFB-Q FFC-Q FFD-Q P0701 UDP E0201 J2 ENLDN J3, LOADI J4, LOADI J5, LOADI J6, LOADI UDP_CAD ENLDN, CAA P0601, Q0601 ENLDN, FFA-Q ENLDN, CAA, CAB CAD, CAA, UDP, ENATI LOADI, J1, J2 CAD, CAC, CAB, CAA, UDN CAD, CAC, CAB, CAA, UDN, ENATI CAA, ENLDN, G0501, J0501, FFB-Q ENLDN, J0501, CAB, CAA, FFC-Q ENLDN, CAC, CAB, CAA, FFD-Q FE+A,Q, UDN FFB+Q, UDN FFC+Q, UDN UDN, FFD+Q CLOCKI, B0701, E0201, C0801, DAALO CLOCKI, E0201, E0701, F0801, DABLO CLOCKI, E0201, H0701, J0801, DACLO CLOCKI, E0201, L0701, M0801, DADLO END			Detail description of logic  INPUT SIGNALS LOCATION OF SYMBOL (GS IN PAGE 01) OUTPUT SIGNAL PAGE01

Output definition	*2 <pre> HD61J001 RTSL CLOCK OUTDEF C UD OUTDEF U LOADN OUTDEF L ENAPN OUTDEF P ENATN OUTDEF T DATAA OUTDEF A DATAB OUTDEF B DATAC OUTDEF C DATAD OUTDEF D RCA OUTDEF R OA OUTDEF 1 OB OUTDEF 2 OC OUTDEF 4 OD OUTDEF 8 CAA OUTDEF A CAB OUTDEF B CAC OUTDEF C CAD OUTDEF D INTV 4000/2500 EDTIME 100000 EDITIME 0, 0, 4000, 2500 END </pre>	Description of signals which you want to look at in the simulation lists. (Internal signals can be monitored as well.) Example of list EXAMPLE OF LIST  → Sampling period (ns) → Start time in sampling (ns) → Maximum simulation step → Sampling period and start time for fault simulation.
Timing	*4 <pre> CLOCK STL UD CLK LOADN SIG ENAPN SIG ENATN SIG DATAA SIG DATAB SIG DATAC SIG DATAD SIG END </pre> 4000 L, 0/1500, 1/2000, 0/500 1000  → Test period (x 0.1 ns) per cycle	
Test vectors	*5 <pre> INPUT SIGNAL 1 - 30 (1 STEP - 60 STEP) 1 01 01 0 101 10 1 0 10 1 0 01 0 01 0 01 0 0 INPUT SIGNAL LOOP 2 (61 STEP - 83 STEP) 01010 01 0 0 101 01 0 01 0 01 0 0 INPUT SIGNAL LOOP 1-2/10- END </pre>	→ Defines that column 1 to column 30 are valid. → The test vectors from column 1 to column 30 are repeated twice. → Sequential step number (This is just a comment) → This expression means that the first two steps are repeated 10 times.
	*6	

■ NOTES FOR LOGIC DESIGN

No.	Item	Notes																	
1.	Utilization	Must be 90% or less in order to place and route successfully. Maximum gate counts for each master chip is shown in the table. (Utilization factor is subject to be a little bit less than the figure in the table when RAM is used.)	Maximum gate counts to be used actually. <table><tr><th>H04</th><th>H06</th><th>H09</th><th>H15</th><th>H20</th><th>H25</th></tr><tr><td>400</td><td>590</td><td>870</td><td>1400</td><td>1800</td><td>2300</td></tr></table>	H04	H06	H09	H15	H20	H25	400	590	870	1400	1800	2300				
H04	H06	H09	H15	H20	H25														
400	590	870	1400	1800	2300														
2.	Gate Delay	Gate delay is obtained more accurately after place and route. However rough estimate should also be done using the equations shown right to prevent timing design errors in the earlier design phase. Effective Fan Out is calculated as sum of <u>Normalized Loading Factor</u> of the output node. These equation may contain the design margin a little bit.	$t_{PLH} = t_{OLH} + K_{LH} \cdot C_L$$t_{PHL} = t_{OHL} + K_{HL} \cdot C_L$ Where, for internal gates $C_L = 0.4 \times EFO$ $EFO = \sum \frac{NLF}{Fanout}$ for output buffers $C_L = 130pF$ And the variation is 30% to 220%.																
3.	Maximum Fanout	A clock driver, which drives CK inputs of FF's, has a restriction on the number of applicable fanouts, though the other signals have no limitation if lower speed is acceptable.	○ Max. Fanout of CK driver Power Inverter . . . 20 The others 10 ○ The other signals 24																
4.	Automatic Modification of unconnected inputs of macro	When an input of a macro is left unconnected, the automatic router connects it to either VCC ("1" level) or GND ("0" level). The macrocell list shows which input of each macro will be connected to which level. An input of AND or NAND gates will be connected to VCC, and that of OR or NOR gates to GND, even though these are not indicated in the list. "@" beside an input shows that the input will be connected to VCC, and "#" to GND. It is not allowed to leave an input unconnected dropping "@" nor "#" except the cases of AND, NAND, OR or NOR.	 When inputs are left open, input A will be fixed to "0" input Y will be fixed to "1".																
5.	Simultaneous Turn on/off of Output Buffers	The number of output buffers which simultaneously change their output levels must be equal to or less than the figures in the table respectively depending on the prebuffers.	<table><tr><th>Buffer Prebuffer</th><th>OT</th><th>ODN</th><th>OZ</th></tr><tr><td>Inverter</td><td>10</td><td>8</td><td>8</td></tr><tr><td>2 input NOR</td><td>14</td><td>10</td><td>8</td></tr><tr><td>3 input NOR</td><td>16</td><td>12</td><td>8</td></tr></table>	Buffer Prebuffer	OT	ODN	OZ	Inverter	10	8	8	2 input NOR	14	10	8	3 input NOR	16	12	8
Buffer Prebuffer	OT	ODN	OZ																
Inverter	10	8	8																
2 input NOR	14	10	8																
3 input NOR	16	12	8																
6.	Testing	(1) All the logic must be able to be initialized by external inputs. (2) Restriction due to the Simulator. (a) When one or more inputs associated with FF such as CK, CL and PR is indefinite the output is also indefinite. For example, output of FF will not be fixed when CK input is indefinite even if it is quite evident logically that CK input is stable either in high or low level.   																	

No.	Item	Notes	
		(b) For the given logical variables X, Y, suppose that there is the following relation between them $X = \bar{Y}$ When X or Y is indefinite, both $X + Y$ and $X \cdot Y$ are also indefinite contrary to the theoretical result. (3) It is preferable to split a multistage shift registers and/or counters to provide test signals in the proper positions in order to improve the efficiency of testing. (4) It is preferable to provide test clock in addition to the original clock whose frequency is much lower than other clocks such as a system clock. (5) It is recommended to employ a test circuit that enables memory element to be set and read out by scanning. (6) The figure shows an example of additional test logic to generate several test signals from a single TEST pin, which is helpful when we suffer from the shortage of pins. Another example shown here is to share the output pin to monitor another internal signal. (7) It is very important to do timing design of test logic as well. Is test logic speed OK? Won't unexpected events occur at the transition time from test to normal mode or contrary?	     
7.	Others	(1) As far as a macro is concerned, one signal is prohibited to be employed to multi-input terminals. (2) Output-to-output connection is not allowed except among 3-state buffers. (3) A chopper circuit using gate delay is prohibited. (4) Oscillator circuit should be built as shown. Oscin and OSC OUT pins should be assigned next to the pins which never change their levels, such as V_{CC} and GND. (5) Internal bus lines should be prevented from floating. Dummy 3-state buffer is recommended to be added.	    

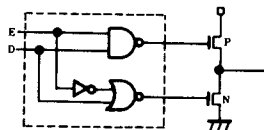
■ MACROCELL LIBRARY

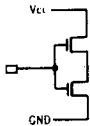
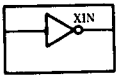
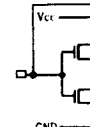
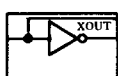
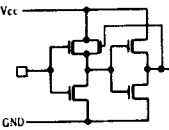
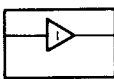
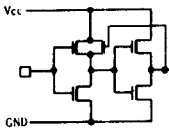
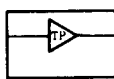
1. I/O BUFFERS

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
Input Buffer TTL Level		—	—			D1	5.5	0.3	6.5	0.4
IT										
Input Buffer CMOS Level		—	—			D1	7.5	0.4	7.3	0.3
IC										
I/O Buffer TTL Level		—	4.9 3.7			D1	Input See "Input Buffer"			
ITO							Output See "3-state Buffer"			
I/O Buffer CMOS Level		—	4.9 3.7			D1	Input See "Input Buffer CMOS Level"			
ICO							Output See "3-state Buffer"			
3-State Buffer		—	4.9 3.7			D1	1.8	0.10	2.5	0.13
OZ										
OUTPUT		—	8			D1	2.8	0.10	3.8	0.14
OT										
Open Drain Output		—	3.7			D1	—	—	2.4	0.13
ODN										

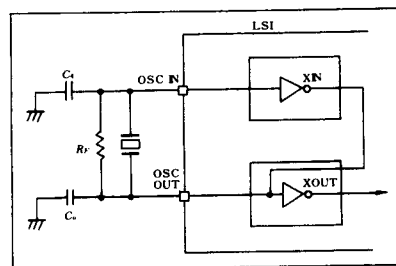
Note) Application of Tri-state buffer

Equivalent circuit

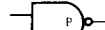
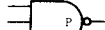
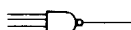
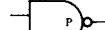
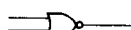
This control circuit has
to be built by internal
gate

Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Symbol No.	Delay			
Function	Equivalent Circuit						tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
OSC In		—	—			D1	6.2	0.8	6.3	0.8
XIN										
OSC OUT		—	—			D1	7.9	1.0	5.0	0.9
XOUT										
SCHMITT TTL Level		—	—			D1	8.5	0.4	21.9	0.6
ITS										
SCHMITT CMOS Level		—	—			D1	10.3	0.5	12.6	0.4
ICS										

		DP-28	DP-40	DP-64	FP-64	FP-80	FP-100
H04	IN	TBD	TBD	TBD	TBD		
	OUT	TBD	TBD	TBD	TBD		
H06	IN		12	18	TBD	14	
	OUT		11	17	TBD	13	
H07	IN	9	12	18		14	
	OUT	8	11	17		13	
H15	IN		11	17		13	
	OUT		12	18		14	
H20	IN		11	17		13	16
	OUT		12	18		14	17
H25	IN		TBD	TBD			TBD
	OUT		TBD	TBD			TBD

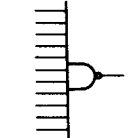
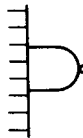
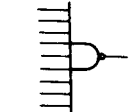
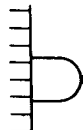
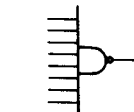


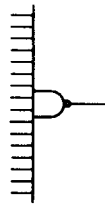
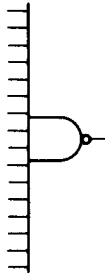
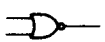
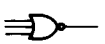
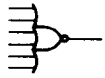
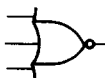
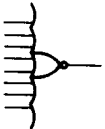
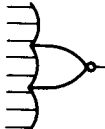
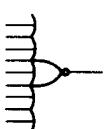
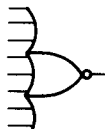
2. POWER GATES

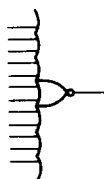
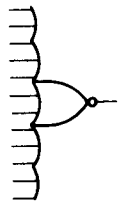
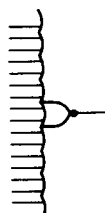
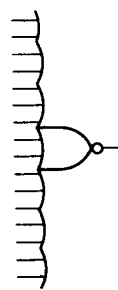
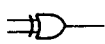
Macrocell		Equiv- alent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay				
Function	Equivalent Circuit					Symbol No.	tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
Power inverter NAP		1	1.4	@		—	0.9	0.6	0.3	0.5
Power-2 input NAND NAP		2	1.4			—	1.1	0.6	0.5	0.6
Power-3 input NAND NAP		3	1.4			—	1.3	0.6	0.7	0.8
Power-4 input NAND NAP		4	1.4			—	1.5	0.6	1.1	0.9
Power-2 input NOR NRP		2	1.4			—	1.1	1.1	0.4	0.5
Power-3 input NOR NRP		3	1.4			—	1.7	1.5	0.5	0.5
Power-4 input NOR NRP		4	1.4			—	2.5	2.0	0.6	0.5

3. GATES

3. GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay				
Function	Equivalent Circuit					Symbol No.	tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
Inverter NA		1	1	@		—	1.0	1.1	0.7	0.8
2-Input NAND NA		1	1			—	1.0	1.2	1.0	1.2
3-Input NAND NA		2	1			—	1.0	1.2	1.3	1.5
4-Input NAND NA		2	1			—	1.6	1.2	1.2	1.8
6-Input NAND NA		5	1			—	2.3	1.1	2.6	0.6
8-Input NAND NA		6	1			—	2.5	1.1	3.1	0.6
9-Input NAND NA		7	1			—	2.4	1.1	3.5	0.7
12-Input NAND NA		8	1			—	2.6	1.1	4.1	0.7

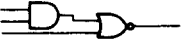
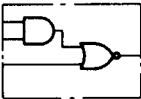
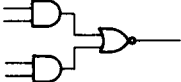
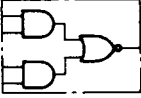
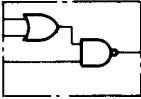
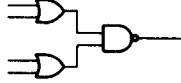
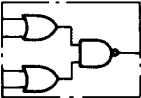
Macrocell		Equiv- alent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay				
Function	Equivalent Circuit					Symbol No.	tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
16-Input NAND		11	1			—	2.7	1.1	4.9	0.8
NA										
2-Input NOR		1	1			—	1.3	2.1	0.6	0.8
NR										
3-Input NOR		2	1			—	1.9	3.1	0.7	0.8
NR										
4-Input NOR		2	1			—	2.1	4.1	0.7	0.8
NR										
6-Input NOR		5	1			—	3.4	1.1	1.9	0.6
NR										
8-Input NOR		6	1			—	4.2	1.1	2.0	0.6
NR										
9-Input NOR		7	1			—	3.8	1.1	2.1	0.6
NR										

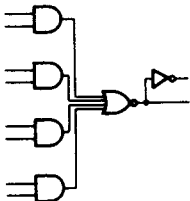
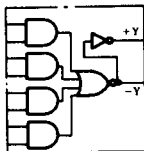
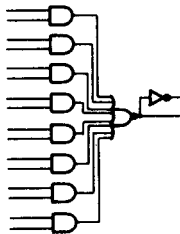
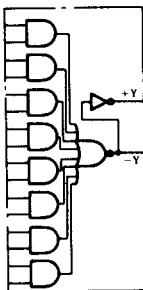
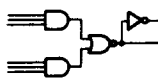
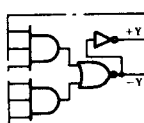
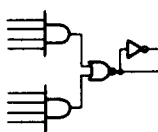
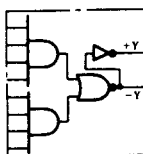
Macrocell		Equiva- lent Gate Count	Normalized Load Factor	Clamp Level when Open	Symbol	Delay				
Function	Equivalent Circuit					Symbol No.	tPLH (ns)		tPHL (ns)	
Macro Function Name							tOLH	kLH	tOHL	kHL
12-Input NOR		8	1			—	4.6	1.1	2.2	0.6
NR										
16-Input NOR		11	1			—	5.3	1.1	2.4	0.6
NR										
2-Input EOR		3	1.4			—	2.1	2.1	0.8	1.1
EOR										

4. 3-STATE GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
3-State Inverter (Internal)		1	1	# @ @		—	D		1.0	1.0	1.4	1.3
NAZ							E/ $\bar{E}$		0.8		1.2	
3-State Buffer (Internal)		3	1.4	# @ @		—	D		1.0	1.1	1.6	0.6
ANZ							E		1.9		1.6	

5. AND-NOR, OR-NAND GATES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2-AND-NOR		2	1			A1	AND Input		1.7	2.1	0.9	1.1
NRA23							NOR Input		1.3		0.9	
2 Wide-2 Input AND-NOR		2	1			A1			1.6	1.6	1.1	1.1
NR2A2												
2-OR-NAND		2	1			A1	OR Input		1.6	2.1	0.9	1.1
NAR23							NAND Input		1.1		0.9	
2 Wide-2 Input OR-NAND		2	1			A1			1.9	2.1	1.0	0.9
NA2R2												

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
4 Wide-2 Input AND-NOR		5	1	#####		A4	-Y	3.8	2.6	1.7	1.1	
NR4A2N							+Y	2.5	1.1	4.3	0.8	
8 Wide-2 Input AND-NOR		10	1	#####		A5	-Y	2.9	1.1	4.4	1.0	
NR8A2N							+Y	4.8	1.1	3.1	0.6	
2 Wide-3 Input AND-NOR		4	1			A2	-Y	2.5	1.4	2.0	1.4	
NR2A3N							+Y	2.7	1.7	2.6	1.3	
2 Wide-4 Input AND-NOR		5	1			A4	-Y	2.5	1.4	2.6	1.8	
NR2A4N							+Y	3.5	2.2	2.7	1.2	

6. LATCHES

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay										
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)						
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}					
$\overline{R}\overline{S}$ -Latch		3	1			A3	$\overline{S}$	+Q	2.9	1.1	—	0.6					
LRS0							$\overline{R}$		1.5		1.9						
							$\overline{S}$	-Q	1.5	1.1	1.9	0.6					
							$\overline{R}$		2.9		—						
RS-Latch		3	1			A3	S	+Q	1.3	1.1	2.4	0.6					
LRS3							R		—		2.8						
							S	-Q	—	1.1	2.8	0.6					
							R		1.3		2.4						
$\overline{R}2\overline{S}2$ -Latch		4	1			A4	$\overline{S}$	+Q	3.6	1.1	—	0.6					
LR2S20							$\overline{R}$		2.0		2.1						
							$\overline{S}$	-Q	2.0	1.1	2.1	0.6					
							$\overline{R}$		3.6		—						
R2S2-LATCH		4	1			A4	S	+Q	1.4	1.1	3.3	0.7					
LR2S23							R		—		4.0						
							S	-Q	—	1.1	4.0	0.7					
							R		1.4		3.3						
D-Latch		3	1.4	@		C	G	+Q	1.4	1.1	1.8	0.6					
LD							D		2.0		2.3						
							G	-Q	2.2	1.1	1.8	0.6					
							D		2.7		2.4						
D-Latch with CLR		4	1.4	@		C	G	+Q	1.8	2.1	1.9	0.7					
LDC1							CL		1.6		0.9						
							D		2.3		2.4						
							G		2.3		2.4						
							CL	-Q	1.3	1.1	0.9	0.6					
			1	#			D		2.8		2.9						
D-Latch with PRE/CLR			1.4	@			G	+Q	4.1	1.1	2.1	0.6					
							$\overline{PR}$		3.1		—						
							CL		2.0		1.7						
							D		4.1		3.1						
			1	@			G	-Q	3.5	1.1	2.7	0.6					
							$\overline{PR}$		2.0		1.7						
							CL		3.1		—						
							D		4.7		2.7						

7. FLIP-FLOPS

Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
DFF		6	1	@ @		C	CK	+Q	2.7	1.1	2.5	0.6
FD								-Q	2.9	1.1	3.0	0.5
DFF with Load		8	1	@ @ @ @ #		B4	CK	+Q	2.7	1.1	2.5	0.6
FDL							DL	4.1	4.4			
							CK	-Q	2.9	1.1	3.0	0.5
							DL	4.8	4.4			
DFF with PRE/CLR		8	1 1	@ @		C	CK	+Q	3.0	2.1	2.8	0.8
FDPC3			1.4 1.4	# #			CL	-	2.5		0.8	0.8
							CK	-Q	3.8	2.1	3.8	0.8
							CL	1.8	-		-	
							PR	-	-	0.8	0.8	
JKFF		8	1.4 1 1	@ @ @ #		C	CK	+Q	2.4	1.1	3.5	1.0
FJ								-Q	2.8	1.1	3.1	1.0
JKFF with PRE/CLR		13	1.4 1 1	@ @ @ #		C	CK	+Q	5.2	1.1	3.5	0.6
							PR	4.2	-			
							CL	-	-	2.5		
							CK	-Q	5.2	1.1	3.5	0.6
							PR	-	2.5			
FJPC1			1.4 1	@ #			CL	4.2	-	-		

8. MULTIPLEXERS

Macrocell		Equiva- lent Gate Count	Normal- ized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay										
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)						
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}					
2 to 1 Multi- plexer		3	1.4 1 1	# # #		B2	Y ₀	+Y	2.1	1.1	2.1	0.6					
M2T1N							Y ₁		2.1		2.1						
							S		2.6		2.6						
							Y ₀	-Y	1.7	2.1	1.7	1.2					
							Y ₁		1.7		1.7						
							S		2.2		2.2						
4 to 1 Multi- plexer		9	1	# # # # #		B4	Y ₀	+Y	3.4	1.1	4.6	0.9					
M4T1N							Y ₁		3.4		4.6						
							Y ₂		3.4		4.6						
							Y ₃		3.4		4.6						
							A	-Y	4.8	2.4	6.0	1.4					
							B		4.8		6.0						
							Y ₀		4.0		2.3						
							Y ₁		4.0		2.3						
							Y ₂		4.0		2.3						
							Y ₃		4.0		2.3						
							A		5.4		3.7						
							B		5.4		3.7						
1 to 2 Demulti- plexer		4	1.4	# @		B3	Y	+0	1.3	1.1	1.7	0.6					
M1T2N							A		1.8		2.3						
							Y	+1	1.3	1.1	1.7	0.6					
							A		1.2		1.7						
							Y	-0	1.5	1.1	0.9	1.1					
							A		2.0		1.4						
							Y	-1	1.5	1.1	0.9	1.1					
							A		1.5		0.9						

9. DECODERS/ENCODERS

9. DECODERS/ENCODERS												
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay					
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)	
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2-bit Decoder		8	1	# # #		B5	A	-0	1.8	1.1	2.0	1.0
							B	-0	1.8		2.0	
							A	-1	2.8	1.1	2.8	1.0
							B	-1	1.8		2.0	
							A	-2	1.8	1.1	2.0	1.0
							B	-2	2.8		2.8	
							A	-3	2.8	1.1	2.8	1.0
							B	-3	2.8		2.8	
							A	+0	2.4	1.1	2.2	0.6
							B	+0	2.4		2.2	
							A	+1	3.2	1.1	3.2	0.6
							B	+1	2.4		2.2	
D2T4N		8	1	# # #		B5	A	-0	1.8	1.1	2.0	1.0
							B	-0	1.8		2.0	
							A	-1	2.8	1.1	2.8	1.0
							B	-1	1.8		2.0	
							A	-2	1.8	1.1	2.0	1.0
							B	-2	2.8		2.8	
							A	-3	2.8	1.1	2.8	1.0
							B	-3	2.8		2.8	
							A	+0	2.4	1.1	2.2	0.6
							B	+0	2.4		2.2	
							A	+1	3.2	1.1	3.2	0.6
							B	+1	2.4		2.2	
3-bit Decoder		12	2.2	@ @ @ @ @ @ @ @		B5	A	-0	1.6	1.2	1.0	1.5
							B	-0				
							C	-0				
							A	-1				
							B	-1				
							C	-1				
							A	-2				
							B	-2				
							C	-2				
							A	-3				
							B	-3				
							C	-3				
D3T8		12	2.2	@ @ @ @ @ @ @ @		B5	A	-0	1.6	1.2	1.0	1.5
							B	-0				
							C	-0				
							A	-1				
							B	-1				
							C	-1				
							A	-2				
							B	-2				
							C	-2				
							A	-3				
							B	-3				
							C	-3				

10. OTHERS

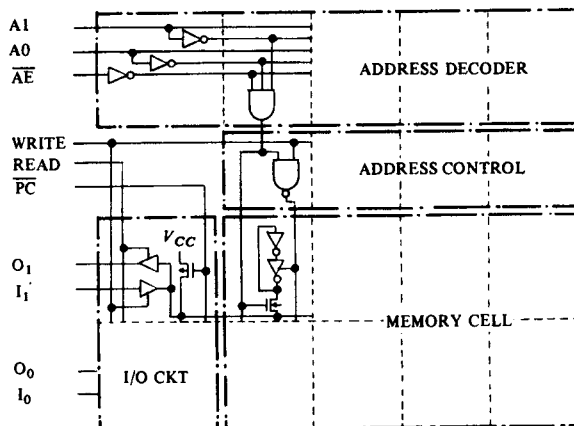
Macrocell		Equivalent Gate Count	Normalized Load Factor	Clamp Level When Open	Symbol	Symbol No.	Delay						
Function	Equivalent Circuit						Input Name	Output Name	t_{PLH} (ns)		t_{PHL} (ns)		
Function Name									t_{OLH}	K_{LH}	t_{OHL}	K_{HL}	
4-bit Equal Comparator		12	1.4	#####		B5	A ₀ A ₁ A ₂ A ₃ B ₀ B ₁ B ₂ B ₃		4.5	4.2	2.8	0.6	
ZEQC4													
2-bit SR with CLR/PRE		12	1 1 1.4 1 1.4 1	@#####		B4	CK CLA PRA CK CLB PRB	+A +B	4.3 4.1 5.1 4.3 4.1 5.1	2.1	4.1 1.1 — 4.1 1.1 —	0.6 — — 0.6 — —	
ZSRCP3													
2-bit SR		10	1	@@		B1	CK	+A +B	3.5 3.5	1.1	2.9	0.6 0.6	
ZSR													

11. RAM

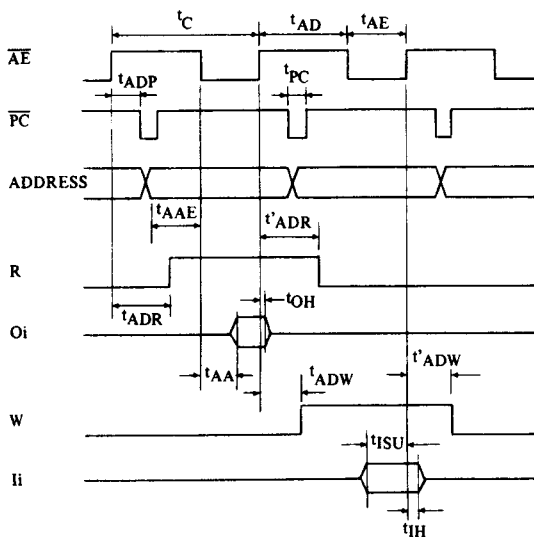
Macrocell		Equivalent Gate Count	Normalized Load Factor	Symbol	Symbol No.	Delay														
Function	Equivalent Circuit																			
Function Name																				
Single Port RAM b bits/word $w=2^l$ word $b=2, 4, \dots, 16$ $w=1, 2, \dots, 32$		$1.5 \cdot b \cdot w$ $+$ $3b$ $+$ $6w$ $+$ 70		when $b-1 \geq 10$, the expressions are like follows. <table border="1"> <tr> <td>b-1</td><td>--8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>--</td></tr> <tr> <td>Expressions</td><td>--8</td><td>9</td><td>A</td><td>B</td><td>C</td><td>--</td></tr> </table>	b-1	--8	9	10	11	12	--	Expressions	--8	9	A	B	C	--	A	40 ns
b-1	--8	9	10	11	12	--														
Expressions	--8	9	A	B	C	--														
Dual Port RAM b bits/words $w=2^l$ words $b=2, 4, \dots, 16$ $w=1, 2, \dots, 32$		$2 \cdot b \cdot w$ $+$ $7.5b$ $+$ $8w$ $+$ 70			A	40 ns														
RAM Pre-charge PCC		28	1		B1															

■ EQUIVALENT CIRCUIT OF RAM (Single Port RAM)

The following figure is not exactly the same as the actual circuit.



■ RECOMMENDED TIMING



	Unit; ns		
	min	typ	max
t_c	400	—	30,000
t_{AD}	250	—	—
t_{AE}	150	—	—
t_{ADP}	30	80	160
t_{PC}	10	30	40
t_{AAE}	30	—	—
t_{ADR}	0	—	t_{AD}
t'_{ADR}	0	—	t_{AD}
t_{AA}	20	40	90
t_{OH}	4	10	20
t_{ADW}	0	—	t_{AD}
t'_{ADW}	0	—	t_{AD}
t_{ISU}	30	—	—
t_{IH}	30	—	—

■ FUNCTIONAL TEST FOR ON-CHIP RAM

In order to easily test on-chip RAM, the logic design should be done so as to access the RAM directly outside the chip, for instance in RAM-TEST-MODE.

■ POWER SUPPLY PIN ASSIGNMENT

Standard power supply pins are assigned as follows. Additional power supply pins may be needed for the purpose of GND NOISE immunity in case that many output buffers turn on/off simultaneously and/or output-current drains much.

		DP-28	DP-40	DP-64	FP-64	FP-80	FP-100
HG61H04	GND	7	10	16, 48	10, 42		
	V _{CC}	21	30	32, 64	26, 58		
	NC			8, 9, 24, 25 40, 41, 56, 57	1, 2, 19, 20, 33, 34, 51, 52		
HG61H06	GND		10	16, 48		12, 52	
	V _{CC}		30	32, 64		33, 73	
	NC					1, 4, 21, 24, 25, 40, 41, 44, 61, 64, 65, 80	
HG61H09	GND	7	10	16, 48		12, 52	
	V _{CC}	21	30	32, 64		33, 73	
	NC						
HG61H15	GND		10	16, 48		12, 52	
	V _{CC}		30	32, 64		33, 73	
	NC						
HG61H20	GND		10	16, 48		12, 52	
	V _{CC}		30	32, 64		33, 73	
	NC						
HG61H25	GND		10	16, 48			
	V _{CC}		30	32, 64			
	NC						

■ PACKAGE OUTLINE

Unit: mm

