

March 1997

ARINC 429 Bus Interface Line Driver Circuit

Features

- TTL and CMOS Compatible Inputs
- Adjustable Rise and Fall Times via Two External Capacitors
- Programmable Output Differential Voltage via V_{REF} Input
- Operates at Data Rates Up to 100 Kilobits/Sec
- Output Short Circuit Proof and Contains Over-Voltage Protection
- Outputs are Inhibited (0 Volts) If DATA (A) and DATA (B) Inputs are Both in the "Logic One" State
- DATA (A) and DATA (B) Signals are "AND'd" with Clock and Sync Signals
- Full Military Temperature Range

Ordering Information

PACKAGE	TEMPERATURE RANGE	PART NUMBER	PKG. NO
SBDIP	-40°C to +85°C	HS1-3182-9+	D16.3
	-55°C to +125°C	HS1-3182-8	D16.3
SMD#	-55°C to +125°C	5962-8687901EA	D16.3
CLCC	-55°C to +125°C	HS4-3182-8	J28.A
	-55°C to +125°C	5962-86879013A	J28.A

Description

The HS-3182 is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This Device is intended to be used with a companion chip, HS-3282 CMOS ARINC Bus Interface Circuit, which provides the data formatting and processor interface function.

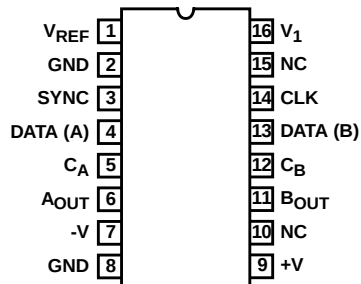
All logic inputs are TTL and CMOS compatible. In addition to the DATA (A) and DATA (B) inputs, there are also inputs for CLOCK and SYNC signals which are AND'd with the DATA inputs. This feature enhances system performance and allows the HS-3182 to be used with devices other than the HS-3182.

Three power supplies are necessary to operate the HS-3182: $+V = +15V \pm 10\%$, $-V = -15V \pm 10\%$, and $V_1 = 5V \pm 5\%$. V_{REF} is used to program the differential output voltage swing such that $V_{OUT} (DIFF) = \pm 2V_{REF}$. Typically, $V_{REF} = V_1 = 5V \pm 5\%$, but a separate power supply may be used for V_{REF} which should not exceed 6V.

The driver output impedance is $75\Omega \pm 20\%$ at 25°C. Driver output rise and fall times are independently programmed through the use of two external capacitors connected to the C_A and C_B inputs. Typical capacitor values are $C_A = C_B = 75pF$ for high-speed operation (100KBPS), and $C_A = C_B = 300pF$ for low-speed operation (12 to 14.5KBPS). The outputs are protected against over-voltage and short circuit as shown in the Block Diagram. The HS-3182 is designed to operate with a case temperature range of -55°C to +125°C, or 0°C to +70°C.

Pinouts

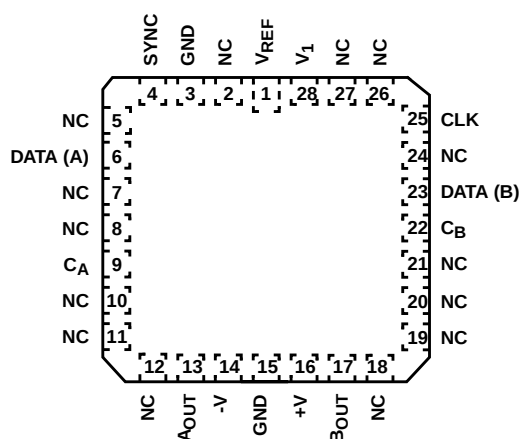
HS-3182 (SBDIP)
TOP VIEW



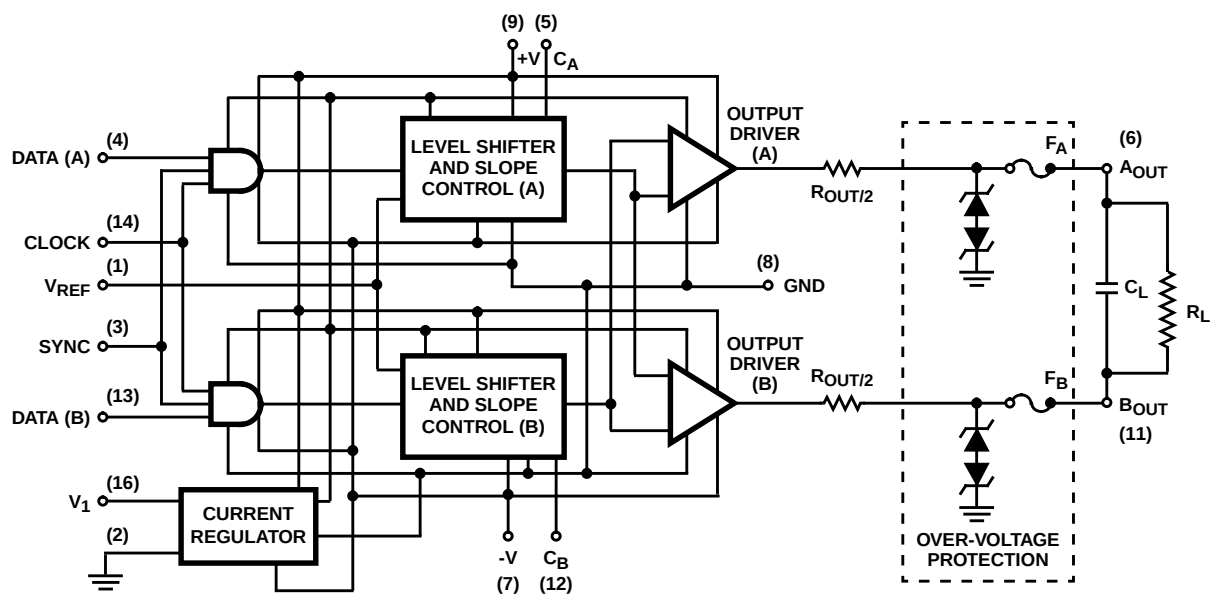
TRUTH TABLE

SYNC	CLK	DATA (A)	DATA (B)	AOUT	BOUT	COMMENTS
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	-VREF	+VREF	Low
H	H	H	L	+VREF	-VREF	High
H	H	H	H	0V	0V	Null

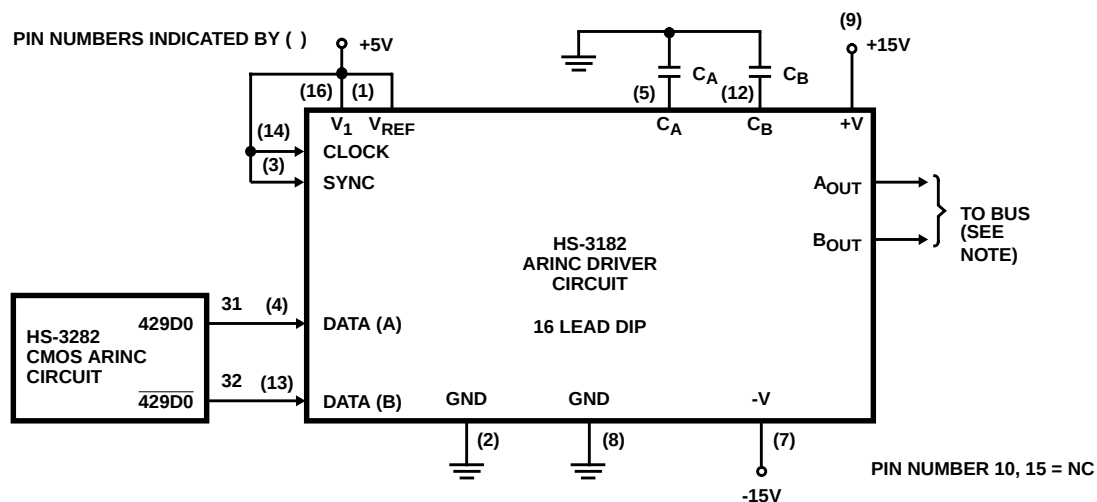
HS-3182 (CLCC)
TOP VIEW



Block Diagram



Typical Application



NOTE: The rise and fall time of the outputs are set to ARINC specified values by C_A and C_B . Typical $C_A = C_B = 75\text{pF}$ for high speed and 300pF for low speed operation. The output HI and low levels are set to ARINC specifications by V_{REF} .

Absolute Maximum Ratings

Voltage Between +V and -V Terminals	40V
V ₁	7V
V _{REF}	6V
Logic Input Voltage	GND -0.3V to V ₁ +0.3V
ESD Classification	Class 1
Output Short Circuit Duration	See Note 1
Output Over-Voltage Protection	See Note 2

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package	75°C/W	18°C/W
CLCC Package	60°C/W	14°C/W
Storage Temperature Range	-65°C to +150°C	
Maximum Junction Temperature	+175°C	
Maximum Lead Temperature (Soldering 10s)	+300°C	

Recommended Operating Conditions

Operating Voltage	
+V	+15V ± 10%
-V	-15V ± 10%
V ₁	5V ± 5%
V _{REF} (For ARINC 429)	5V ± 5%
Operating Temperature Range	
HS-3182-5	0°C to +70°C
HS-3182-8	-55°C to +125°C

Die Characteristics

Transistor Count	133
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NOTES:

- Heat sink may be required for 100K bits/s at +125°C and output short circuit at +125°C.
- The fuses used for output over-voltage protection may be blown by a fault at each output of greater than ± 6.5V relative to GND.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Performance Specifications

DC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Supply Current +V (Operating)	I _{CCOP} (+V)	No Load (0-100K bits/s)	-	16	mA
Supply Current -V (Operating)	I _{CCOP} (-V)	No Load (0-100K bits/s)	-16	-	mA
Supply Current V ₁ (Operating)	I _{CCOP} (V ₁)	No Load (0-100K bits/s)	-	975	μA
Supply Current V _{REF} (Operating)	I _{CCOP} (V _{REF})	No Load (0-100K bits/s)	-1.0	-	mA
Logic "1" Input Voltage	V _{IH}		2.0	-	V
Logic "0" Input Voltage	V _{IL}		-	0.5	V
Output Voltage High (Output to GND)	V _{OH}	No Load (0-100K bits/s)	V _{REF} (-250mV)	V _{REF} (+250mV)	
Output Voltage Low (Output to GND)	V _{OL}	No Load (0-100K bits/s)	-V _{REF} (-250mV)	-V _{REF} (+250mV)	
Output Voltage Null	V _{NULL}	No Load (0-100K bits/s)	-250	+250	mV
Input Current (Input Low)	I _{IL}		-20	-	μA
Input Current (Input High)	I _{IH}		-	10	μA
Output Short Circuit Current (Output High)	I _{OHSC}	Short to GND	-	-80	mA
Output Short Circuit Current (Output Low)	I _{OLSC}	Short to GND	80	-	mA
Output Impedance	Z _O	T _A = +25°C	60	90	Ω

NOTE:

- +V = +15V ± 10%, -V = -15V ± 10%, V₁ = V_{REF} = 5V ± 5%, unless otherwise specified T_A = 0°C to +70°C for HS-3182-5 and T_A = -55°C to +125°C for HS-3182-8.

AC Electrical Performance Specifications

AC PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Rise Time (A _{OUT} , B _{OUT})	t _R	C _A = C _B = 75pF, Note 2	1	2	μS
		(at T _A = -55°C Only)	0.9	2.4	μS
		C _A = C _B = 300pF, Note 2	3	9	μS
Fall Time (A _{OUT} , B _{OUT})	t _F	C _A = C _B = 75pF, Note 3	1	2	μS
		(at T _A = -55°C Only)	0.9	2.4	μS
		C _A = C _B = 300pF, Note 3	3	9	μS
Propagation Delay Input to Output	t _{PLH}	C _A = C _B = 75pF, No Load	-	3.3	μS
Propagation Delay Input to Output	t _{PHL}	C _A = C _B = 75pF, No Load	-	3.3	μS

NOTES:

- +V = +15V, -V = -15V, V₁ = V_{REF} = 5V, unless otherwise specified T_A = 0°C to +70°C for HS-3182-5 and T_A = -55°C to +125°C for HS-3182-8.
- t_R measured 50% to 90% times 2, no load.
- t_F measured 50% to 10% times 2, no load.

Electrical Performance Specifications

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	MIN	MAX	UNITS
Input Capacitance	C _{IN}	T _A = +25°C	-	15	pF
Supply Current +V (Short Circuit)	I _{SC} (+V)	Short to GND, T _A = +25°C	-	150	mA
Supply Current -V (Short Circuit)	I _{SC} (-V)	Short to GND, T _A = +25°C	-150	-	mA

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes affecting these parameters.

Power Specifications

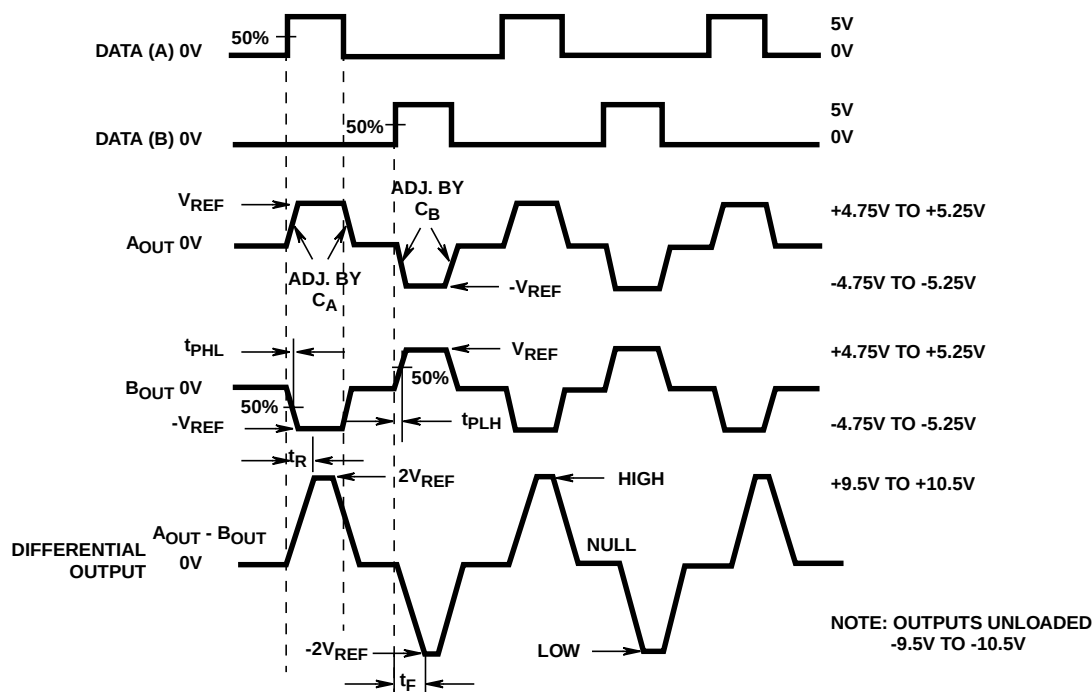
Nominal Power at +25°C, +V = +15V, -V = -15V, V₁ = V_{REF} = 5V, Notes 1, 3

DATA RATE (K BITS/s)	LOAD	+V	V-	V ₁	CHIP POWER	POWER DISSIPATION IN LOAD
0-100	No Load	11mA	-10mA	600μA	325mW	0
12.5-14	Full Load, Note 2	24mW	-24mW	600μA	660mW	60mW
100	Full Load, Note 2	46mW	-46mW	600μA	1 Watt	325mW

NOTES:

- Heat sink may be required for 100K bits/s at +125°C and output short circuit at +125°C.
Thermal characteristics: T_(CASE) = T_(Junction) - θ_(Junction - Case) P_(Dissipation).
Where: T_(Junction Max) = +175°C
θ_(Junction - Case) = 10.9°C/W (6.1°C/W for LCC)
θ_(Junction - Ambient) = 73.5°C/W (54.0°C/W for LCC)
- Full Load for ARINC 429: R_L = 400Ω and C_L = 30,000pF in parallel between A_{OUT} and B_{OUT} (see block diagram).
- Output Over-Voltage Protection: The fuses used for output over-voltage protection may be blown by a fault at each output of greater than ±6.5V relative to GND.

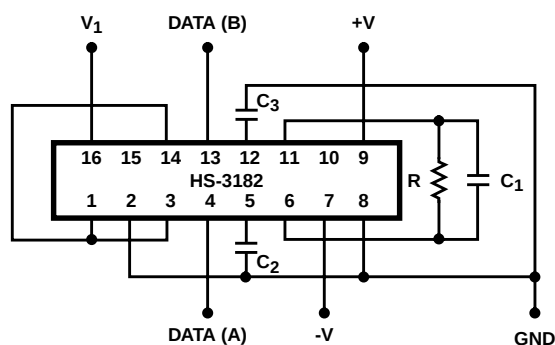
Driver Waveforms



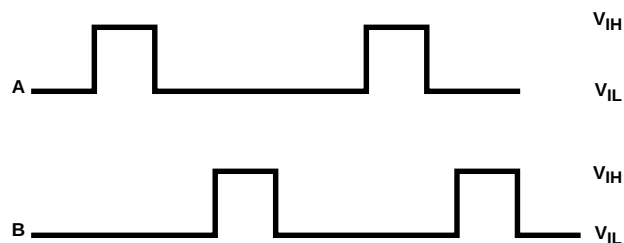
NOTES: t_R measured 50% to 90% times 2
 t_F measured 50% to 10% times 2
 $V_{IH} = 5V$ $V_{OL} = -4.75V$ to $-5.25V$
 $V_{IL} = 0V$ $V_{OH} = 4.75V$ to $5.25V$

When the Data (A) input is in the Logic One state and the Data (B) input is in the Logic Zero state, AOUT is equal to VREF and BOUT is equal to -VREF. This constitutes the Output High state. Data (A) and Data (B) both in the Logic Zero state causes both AOUT and BOUT to be equal to 0V which designates the output Null state. Data (A) in the Logic Zero state and Data (B) in the Logic One state causes AOUT to be equal to -VREF and BOUT to be equal to VREF which is the Output Low state.

Burn-In Schematic



NOTES: $R = 400\Omega \pm 5\%$
 $C_1 = 0.03\mu F \pm 20\%$
 $C_2 = C_3 = 500pF$, NPO
 $+V = +15.5V \pm 0.5V$
 $-V = -15.5V \pm 0.5V$
 $V_1 = +5.5V \pm 0.5V$
 A $0.0\mu F$ decoupling capacitor is required on each of the three supply lines (+V, -V and V1) at every 3rd Burn-In socket.



Ambient Temp. Max. = $+125^{\circ}C$.
 Package = 16 Lead Side Brazed DIP.
 Pulse Conditions = A & B = $6.25kHz \pm 10\%$. B is delayed one-half cycle and in sync with A.
 $V_{IH} = 2.0V$ Min.
 $V_{IL} = 0.5V$ Max.

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