Data Sheet May 2000 File Number 4820.2

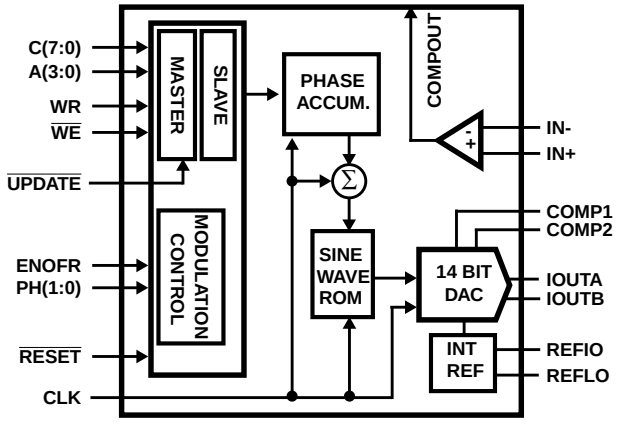
CommLink™ Direct Digital Synthesizer

The 14-bit HSP45314 provides a complete Direct Digital Synthesizer (DDS) system in a single 48-pin LQFP package. A 48-bit Programmable Carrier NCO (numerically controlled oscillator) and a high speed 14-bit DAC (digital to analog converter) are integrated into a stand alone DDS.

The DDS accepts 48-bit center and offset frequency control information via a parallel processor interface. Modulation control is provided by 3 external pins. The PH0 and PH1 pins select phase offsets of 0, 90, 180 and 270 degrees, while the ENOFR pin enables or zeros the offset frequency word to the phase accumulator.

The parallel processor interface has an 8-bit write-only data input C(7:0), a 4-bit address A(3:0) bus, a Write Strobe (WR), and a Write Enable ($\overline{WE}$). The processor can update all registers simultaneously by loading a set of master registers, then transfer all master registers to the slave registers by asserting the $\overline{UPDATE}$ pin.

Block Diagram



Features

- 125MSPS Output Sample Rate with 5V Digital Supply
- 100MSPS Output Sample Rate with 3.3V Digital Supply
- 14-bit DAC with Internal Reference
- Parallel Control Interface for Fast Tuning (50MSPS Control Register Write Rate)
- 48-bit Programmable Frequency Control
- Small 48-pin LQFP package

Applications

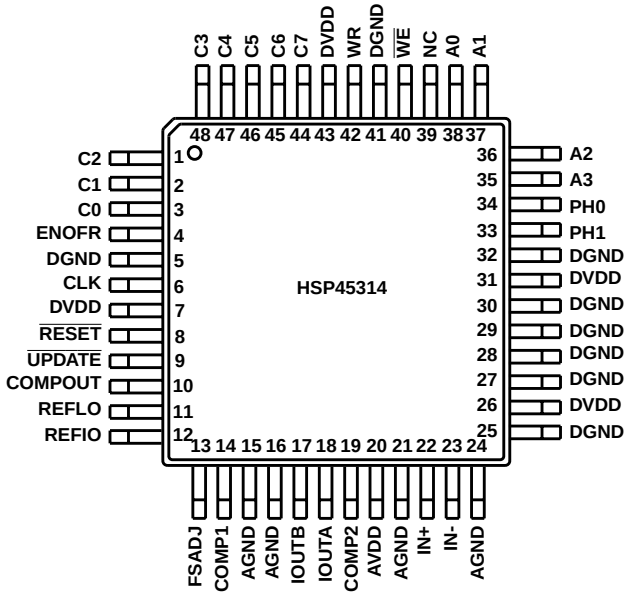
- Programmable Local Oscillator
- FSK Modulation
- Direct Digital Synthesis
- Clock Generation

Ordering Information

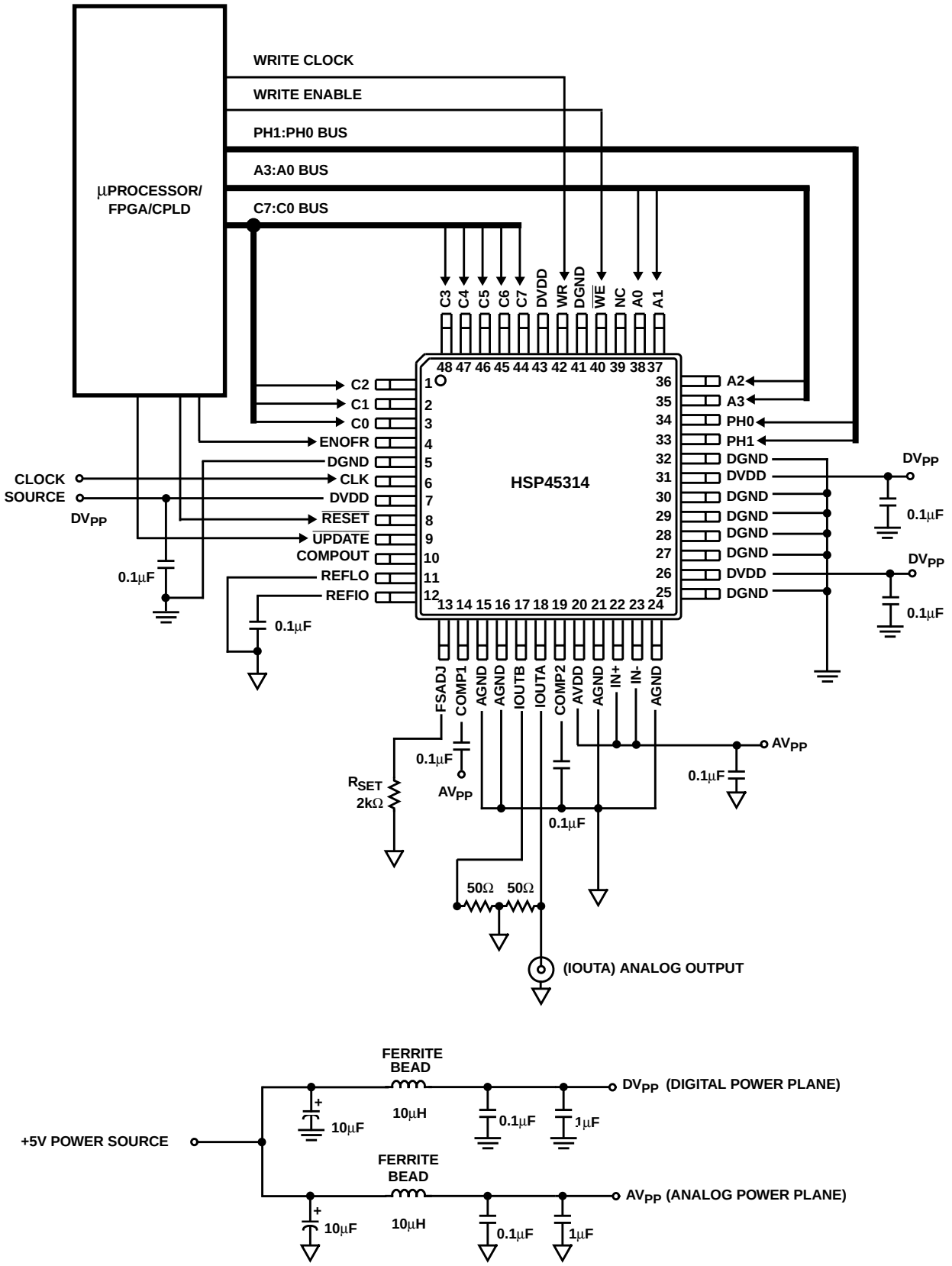
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HSP45314VI	-40 to 85	48 LQFP	Q48.7X7A

Pinout

48-PIN LQFP (Q48.7X7A
TOP VIEW



Typical Application Circuit (Sinewave Generation)



Functional Description

The HSP45314 is an NCO with an integrated 14-bit DAC designed to run in excess of 125MSPS. The NCO is a 16-bit output design, which is rounded to 14 bits for input to the DAC. The frequency control is the sum of a 48-bit center frequency word and a 48-bit offset frequency word. The two components are added modulo 48 bits with the alignment shown in Table 1. Each of the two terms can be zeroed independently (via the microprocessor interface for the center frequency and via the ENOFR pin for the offset frequency term).

Frequency Generation

The output frequency of the part is determined by the summation of two registers:

$f_{OUT} = f_{CLK} \times ((CF + OF) \bmod (2^{48}))/ (2^{48})$,

where CF is the Center Frequency register and OF is the Offset Frequency register.

With a 125MSPS clock rate, the center frequency can be programmed to

$(125 \times 10^6)/(2^{48}) = 0.4$ μHz resolution.

The addition of the frequency control words can be interpreted as two's complement if convenient. For example, if the center frequency is set to 4000...00h and the offset frequency set to C000..00h, the programmed center frequency would be $f_{CLK}/4$ and the programmed offset frequency $-f_{CLK}/4$. The sum would be 10000..00h, but because only the lower 48 bits are retained, the effective frequency would be 0. In reality, frequencies above 8000...00h alias below $f_{CLK}/2$ (the output of the part is real), so the MSB is only provided as a convenience for two's complement calculations.

The frequency control of the NCO is the change in phase per clock period or $d\phi/dt$. This is integrated by the phase accumulator to obtain frequency. The most significant 24 bits of phase are then mapped to 16 bits of amplitude in a sine look-up table function. The range of $d\phi/dt$ is 0 to 1 with 1 equaling 360 degrees or (2 x pi) per clock period. The phase accumulator output is also 0 to 1 with 1 equaling 360 degrees. The operations are modulo 48 bits because the MSB (bit 47) aligns with the most significant address bit of the sine ROM and the ROM contains one cycle of a sinusoid. The MSB is weighted at 180 degrees. Full scale is 360 degrees minus 1 LSB and the phase then rolls over to 0 degrees for the next cycle of the sinusoid.

Parallel Interface

The processor interface is an 8-bit parallel write only interface. The interface consists of 8 data bits (C7:C0), four address pins (A3:A0), a Write Strobe (WR), and a Write Enable ($\overline{WE}$). The interface is a master/slave type. The processor interface loads a set of master registers. The contents of the master set of registers is then transferred to a slave set of registers by asserting a pin ($\overline{UPDATE}$). This allows all of the bits of the frequency control to be updated simultaneously.

The rate which the user writes (WR) to these registers does not have to be the same rate as the DDS clock rate (the rate of the NCO and DAC; pin CLK). It is expected that most applications will have a slower register write rate than the DDS clock rate. It takes 6 WR cycles at the write rate plus another 11 CLK cycles at the DDS rate to write and obtain a new frequency, assuming that all registers are rewritten and the $\overline{UPDATE}$ pin is always active. If the $\overline{UPDATE}$ pin is not active until after the new word has been written, it takes 14 CLK cycles, rather than 11. For cases which require the output to be updated with all of the new frequency information present, it is necessary that the $\overline{UPDATE}$ be inactive until after all of the new frequency word has been written to the device. See the Timing Diagrams for more information. The parallel registers can be written to again immediately after the 11th or 14th CLK cycle, again depending the state of $\overline{UPDATE}$. If the application does not need 48 bits (all 6 registers) of frequency information, then the output frequency can be changed more quickly. For example, if only 32 bits of frequency information are needed and it is desired that the output be updated all at once, then it takes 4 WR cycles, then the assertion low of the $\overline{UPDATE}$ pin, plus another 14 CLK cycles at the DDS rate to write and update a new frequency.

The timing is the same whether writing to the center or offset frequency registers. For faster frequency update, consider the ENOFR (Enable Offset Frequency Register) option. Once the values have been written to the center and offset frequency registers, the user can enable and disable the offset frequency register, which is added to the center frequency value when enabled. The ENOFR pin has a latency of 14 CLK cycles, but simplifies the interface because the only pin that has to be toggled is the ENOFR pin.

TABLE 1. FREQUENCY CONTROL BIT ALIGNMENTS

Bits	4444 4444	3333 3333	3322 2222	2222 1111	1111 1100	0000 0000
Individual Bit Alignment	7654 3210	9876 5432	1098 7654	3210 9876	5432 1098	7654 3210
Phase Accumulator	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
Center Frequency	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
Offset Frequency	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx

Control Pins

There are three control pins provided for phase and frequency control. The PH0 and PH1 pins select phase offsets of 0, 90, 180, and 270 degrees and can be used for low speed, unfiltered BPSK or QPSK modulation. These pins can also be used for providing sine/cosine when using two HSP45314s together as quadrature local oscillators. The ENOFR pin enables or zeros the offset frequency word to the phase accumulator and can be used for FSK or MSK modulation. These control pins and the $\overline{\text{UPDATE}}$ pin are passed through special cells to minimize the probability of meta-stability.

Reset

A $\overline{\text{RESET}}$ pin is available which resets all registers to their defaults. In order to reset the part, the user must take the $\overline{\text{RESET}}$ pin low, allow at least one CLK rising edge, and then take the $\overline{\text{RESET}}$ pin high again. The latency from the $\overline{\text{RESET}}$ pin going high until the output reflects the reset is 11 CLK cycles. See the register description table in the back of the datasheet for the default states of all bits in all addresses. After $\overline{\text{RESET}}$ goes high, one rising edge of CLK is required before the control registers can be written to again.

Comparator

A comparator is provided for square wave output generation. The user can take the DDS analog output, filter it, and then send it back into the comparator. A square wave will be generated at the comparator output (COMPOUT pin) at an amplitude level that is dependent on the digital power supply used (DV_{DD}). The comparator was designed to operate at speeds comparable to the DDS output frequency range (approximately 0-50MHz). It is not intended for low jitter applications. The comparator has a sleep mode that is activated by connecting both inputs (IN- and IN+) to the analog power supply plane. This will save approximately 4mA of current (as shown in the Typical Application Circuit). If the comparator is not used, leave the COMPOUT pin floating.

DAC Voltage Reference

The internal voltage reference for the DAC has a nominal value of +1.2V with a ±60ppm/^{o}C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (11) selects the reference. The internal reference can be selected if pin 11 is tied low (ground). If an external reference is desired, then pin 11 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 12. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

If the internal reference is used, V_{FSADJ} will equal approximately 1.2V (pin 13). If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT} (Full Scale) is:

I_{OUT}(Full Scale) = (V_{FSADJ}/R_{SET}) X 32.

Analog Output

IOUTA and IOUTB are complementary current outputs. They are generated by a 14-bit digital-to-analog converter (DAC) that is capable of running at the full 125MSPS rate. The DDS clock also clocks the DAC. The sum of the two output currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0V to 1.25V. R_{LOAD} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$V_{OUT} = I_{OUT}$ X R_{LOAD}.

These outputs can be used in a differential-to-single-ended arrangement. This is typically done to achieve better harmonic rejection. Because of a mismatch in IOUTA and IOUTB, the transformer does not improve the harmonic rejection. However, it can provide voltage gain without adding distortion. The SFDR measurements in this data sheet were performed with a 1:1 transformer on the output of the DDS (see Figure 1). With the center tap grounded, the output swing of pins 17 and 18 will be biased at zero volts. The loading as shown in Figure 1 will result in a 500mV_{PP} signal at the output of the transformer if the full scale output current of the DAC is set to 20mA.

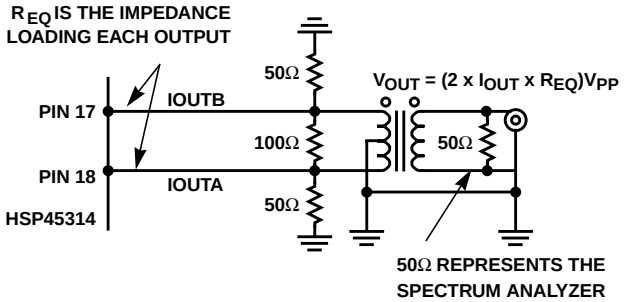


FIGURE 1.

V_{OUT} = 2 x I_{OUT} x R_{EQ}, where R_{EQ} is ~12.5Ω. Allowing the center tap to float will result in identical transformer output, however the output pins of the DAC will have positive DC offset, which could limit the voltage swing available due to the output voltage compliance range. The 50Ω load on the output of the transformer represents the load at the end of a

'transmission line', typically a spectrum analyzer, oscilloscope, or the next function in the signal chain. The necessity to have a 50Ω impedance looking back into the transformer is negated if the DDS is only driving a short trace. The output voltage compliance range does limit the impedance that is loading the DDS output.

Ground Plane Considerations

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane. Pins 11 through 24 are analog pins, while all of the others are digital.

Noise Reduction Considerations

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the power supply pins, AV_{DD} and DV_{DD}. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended.

Power Supplies

The DDS will provide the best SFDR (Spurious Free Dynamic Range) when using +5V analog and +5V digital power supply. The analog supply must be +5V (±10%). The digital supply can be either a +3.3V (±10%) or a +5V (±10%) supply, or anything in between. The DDS is rated to 125MSPS when using a +5V digital supply. The maximum clock is 100MSPS when using a +3.3V digital supply.

Improving SFDR

As was previously noted, using +5V power supplies provides the best SFDR. Under some clock and output frequency combinations, particularly when the f_{CLK}/f_{OUT} ratio is less than 4, the user can improve SFDR even further by connecting the COMP2 pin (19) of the DDS to the analog power supply. The digital supply must be +5V if this option is explored. Improvements as much as 6dBc in the SFDR-to-Nyquist measurement were seen in the lab.

FSK Modulation

BFSK (Binary Frequency Shift Keying) can be done by enabling and disabling the offset frequency (ENOFR pin). Once the offset frequency has been written once, it can be toggled with a latency of 14 CLK cycles.

M-ary FSK or GFSK can be done by continuously loading in new frequency words.

Quadrature Local Oscillators

Two HSP45314s can be used as sine/cosine generators for quadrature local oscillator applications. It is important to note that the Phase Accumulator feedback needs to be zeroed in both devices if it is desired that both DDSs restart with a known phase, which is determined by the use of the phase control pins, PH1 and PH0. To zero the phase accumulator, pull bit 5 of address 13 low and then high again at the same time in both devices.

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DGND . . . . . +5.5V
Analog Supply Voltage AV_{DD} to AGND . . . . . +5.5V
Grounds, AGND To DGND. . . . . -0.3V To +0.3V
Digital Input Voltages . . . . . DV_{DD} + 0.3V
Reference Input Voltage Range. . . . . AV_{DD} + 0.3V
Analog Output Current (I_{OUT}) 24mA

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}(^{O}C/W)
LQFP Package	68

Maximum Junction Temperature . . . . . .150^{O}C
Maximum Storage Temperature Range. . . . . -65^{O}C to 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{O}C

Operating Conditions

Temperature Range . . . . . -40^{O}C to 85^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD} = DV_{DD} = +5V (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25^{O}C for All Typical Values

PARAMETER	TEST CONDITIONS	HSP45314 T_A = -40^{O}C TO 85^{O}C			UNITS
		MIN	TYP	MAX	
DAC CHARACTERISTICS					
DAC Resolution		14	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line (Note 7)	-5	+2.5	+6	LSB
Differential Linearity Error, DNL	(Note 7)	-2	+1.5	+4	LSB
Offset Error, I_{OS}	(Note 7)	-0.025		+0.025	% FSR
Offset Drift Coefficient	(Note 7)	-	0.1	-	ppm FSR/^{O}C
Full Scale Gain Error	With Internal Reference (Notes 2, 7)	-10	±1	+10	% FSR
Full Scale Gain Drift	With Internal Reference (Note 7)	-	±50	-	ppm FSR/^{O}C
Full Scale Output Current	(Note 3)	2	-	20	mA
Output Voltage Compliance Range	(Note 3, 7)	-1.0	-	1.25	V
DAC DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	+5V DV_{DD}, +5V AV_{DD} (Note 3)	125	-	-	MSPS
Maximum Clock Rate, f_{CLK}	+3.3V DV_{DD}, +5V AV_{DD} (Note 3)	100	-	-	MSPS
Output Settling Time, (t_{SETT})	±0.05% (±8 LSB) (Note 7)	-	35	-	ns
Output Rise Time	Full Scale Step	-	2.5	-	ns
Output Fall Time	Full Scale Step	-	2.5	-	ns
Output Capacitance		-	25	-	pF
Output Noise	IOUTFS = 20mA	-	50	-	pA/$\sqrt{Hz}$
	IOUTFS = 2mA	-	30	-	pA/$\sqrt{Hz}$

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$ (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HSP45314 $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS					
Spurious Free Dynamic Range, SFDR Within a Window (Notes 4, 7)	f_{CLK} = 100MSPS, f_{OUT} = 20MHz, 5MHz Span	-	93	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5MHz, 8MHz Span	-	93	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5MHz, 8MHz Span	-	93	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist ($f_{CLK}/2$) (Notes 4, 7)	f_{CLK} = 125MSPS, f_{OUT} = 40.4MHz	-	40	-	dBc
	f_{CLK} = 125MSPS, f_{OUT} = 10.1MHz	57	63	-	dBc
	f_{CLK} = 125MSPS, f_{OUT} = 5.02MHz	-	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz	-	40	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 20.2MHz	-	49	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 5.04MHz	-	72	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 2.51MHz	-	73	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz	-	45	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.02MHz	-	68	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 2.51MHz	-	72	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 1.00MHz	-	71	-	dBc
	f_{CLK} = 25MSPS, f_{OUT} = 1.0MHz	-	72	-	dBc
DAC REFERENCE VOLTAGE					
Internal Reference Voltage, V_{FSADJ}	Pin 13 Voltage with Internal Reference	1.13	1.2	1.28	V
Internal Reference Voltage Drift		-	±60	-	ppm/^{o}C
Internal Reference Output Current Sink/Source Capability		-	±0.1	-	µA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 7)	-	1.4	-	MHz
DIGITAL INPUTS					
Input Logic High Voltage with 5V Digital Supply, V_{IH}	(Note 3)	3.5	5	-	V
Input Logic High Voltage with 3V Digital Supply, V_{IH}	(Note 3)	2.0	3	-	V
Input Logic Low Voltage with 5V Digital Supply, V_{IL}	(Note 3)	-	0	1.3	V
Input Logic Low Voltage with 3V Digital Supply, V_{IL}	(Note 3)	-	0	0.8	V
Input Logic Current, I_{IH}		-10	-	+10	µA
Input Logic Current, I_{IL}		-10	-	+10	µA
Digital Input Capacitance, C_{IN}		-	4	-	pF

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$ (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HSP45314 $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
TIMING CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	+5V DV_{DD}, +5V AV_{DD} (Note 3)	125	-	-	MSPS
Maximum Clock Rate, f_{CLK}	+3.3V DV_{DD}, +5V AV_{DD} (Note 3)	100	-	-	MSPS
CLK Pulse Width, t_{CW}	CLK (Note 3)	5	-	-	ns
Maximum Parallel Write Rate	Rate of WR	50	-	-	MSPS
WR Pulse Width, t_{WW}	(Note 3)	5	-	-	ns
Data Setup Time, t_{DS}	Between DATA and WR (Note 3)	10	-	-	ns
Data Hold Time, t_{DH}	Between DATA and WR (Note 3)	0	-	-	ns
Address Setup Time, t_{AS}	Between ADDR and WR (Note 3)	12	-	-	ns
Address Hold Time, t_{AH}	Between ADDR and WR (Note 3)	0	-	-	ns
$\overline{UPDATE}$ Pulse Width, t_{UW}	(Note 3)	5	-	-	ns
$\overline{UPDATE}$ Setup Time, t_{US}	Between $\overline{UPDATE}$ and CLK (Note 3)	2	-	-	ns
$\overline{UPDATE}$ Hold Time, t_{UH}	Between $\overline{UPDATE}$ and CLK (Note 3)	4	-	-	ns
$\overline{UPDATE}$ Latency, t_{UL}	After $\overline{UPDATE}$, before analog output change, if asserted after writing to the control registers	-	14	-	Clock Cycles
$\overline{UPDATE}$ Latency, t_{UL}	After $\overline{UPDATE}$, before analog output change, if asserted before writing to the control registers	-	11	-	Clock Cycles
Phase Pulse Width, t_{PW}	PH(1:0) (Note 3)	5	-	-	ns
Phase Setup Time, t_{PS}	Between PH(1:0) change and CLK (Note 3)	2	-	-	ns
Phase Hold Time, t_{PH}	Between PH(1:0) change and CLK (Note 3)	4	-	-	ns
Phase Latency, t_{PL}	Between PH(1:0) change and analog output change	-	12	-	Clock Cycles
ENOFR Pulse Width, t_{EW}	ENOFR (Note 3)	5	-	-	ns
ENOFR Setup Time, t_{ES}	Between ENOFR and CLK (Note 3)	2	-	-	ns
ENOFR Hold Time, t_{EH}	Between ENOFR and CLK (Note 3)	4	-	-	ns
ENOFR Latency, t_{EL}	After ENOFR, before analog output change	-	14	-	Clock Cycles
Write Enable Pulse Width, t_{WR}	$\overline{WE}$ (Note 3)	5	-	-	ns
Write Enable Setup Time, t_{WS}	Between $\overline{WE}$ and WR (Note 3)	2	-	-	ns
Write Enable Hold Time, t_{WH}	Between $\overline{WE}$ and WR (Note 3)	4	-	-	ns
$\overline{RESET}$ Pulse Width, t_{RW}	$\overline{RESET}$ (Note 3)	5	-	-	ns
$\overline{RESET}$ Setup Time, t_{RS}	Between $\overline{RESET}$ and CLK	-	2	-	ns
$\overline{RESET}$ Latency to Output, t_{RL}	After $\overline{RESET}$, before analog output reflects reset values	-	11	-	Clock Cycles
$\overline{RESET}$ Latency to Write, t_{RE}	After $\overline{RESET}$, before the control registers can be written to	-	1	-	Clock Cycles

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$ (unless otherwise noted), V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	HSP45314 $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
COMPARATOR CHARACTERISTICS					
Input Capacitance		-	4	-	pF
Input Resistance		-	>1	-	MΩ
Input Current		-	1	-	µA
Maximum Input Voltage Allowed	(Excluding comparator sleep mode)	-	4.0	3.75	V
Minimum Input Voltage, Peak-to-Peak	(Dependent on noise)	-	0.1	-	Vpp
Propagation Delay, High to Low	(Note 8)	-	6	-	ns
Propagation Delay, Low to High	(Note 8)	-	5	-	ns
Output Rise Time	(Note 8)	-	1.5	-	ns
Output Fall Time	(Note 8)	-	1.3	-	ns
Output High Voltage, V_{OH}	I_{OH} = -4mA	2.6	-	-	V
Output Low Voltage, V_{OL}	I_{OL} = +4mA	-	-	0.4	V
Maximum Output Toggle Rate	High Z Load (~1MΩ)	-	100	-	MHz
POWER SUPPLY CHARACTERISTICS					
AV_{DD} (Analog) Power Supply		4.5	5.0	5.5	V
DV_{DD} (Digital) Power Supply		3.0	3.3	5.5	V
Analog Supply Current (I_{AVDD})	5V, IOUTFS = 20mA (Note 10)	-	25	30	mA
	5V, IOUTFS = 2mA	-	7	-	mA
Digital Supply Current (I_{DVDD})	5V (Notes 5, 10)	-	90	100	mA
	3.3V (Notes 6, 9)	-	50	55	mA
Power Dissipation	AV_{DD} = 5V, DV_{DD} = 3.3V, IOUTFS = 20mA (Notes 6, 9)	-	290	363	mW
	AV_{DD} = 5V, DV_{DD} = 5V, IOUTFS = 20mA (Notes 5, 10)	-	625	715	mW
Power Supply Rejection	Single 5V Supply (Note 7)	-0.2	-	+0.2	% FSR/V

NOTES:

2. Gain Error for the DAC is measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA); ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential transformer coupled output and no external filtering.
5. Measured with the clock at 125MSPS and the output frequency at 10MHz.
6. Measured with the clock at 100MSPS and the output frequency at 10MHz.
7. See “Definition of Specifications”.
8. 50MHz, High Z Load (~1MΩ), 15pF capacitance, (IN- = 0.5Vpp), (IN+ = $0.25V_{DC}$).
9. For maximum value, 5.5V AV_{DD} and 3.6V DV_{DD} are used.
10. For maximum value, 5.5V AV_{DD} and 5.5V DV_{DD} are used.

Definition of Specifications

Differential Non-Linearity, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1LSB. A DNL specification of 1LSB or less guarantees monotonicity.

Integral Non-Linearity, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Full Scale Gain Drift, is measured by setting the DAC inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (Full Scale Range) per ^{O}C.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the DAC output current and the full scale adjust current (through R_{SET}).

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per ^{O}C.

Offset Drift, is measured by setting the DAC inputs to all logic low (all 0s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (Full Scale Range) per degree ^{O}C.

Offset Error, is measured by setting the DAC inputs to all logic low (all 0s) and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Output Settling Time, is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. The measurement is done by switching quarter scale. Termination impedance was 25Ω due to the parallel resistance of the 50Ω loading on the output and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed at either IOUTA or IOUTB does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The supply's nominal +5V is varied ±10% and the change in the DAC full scale output current is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs to the DAC set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Timing Diagrams

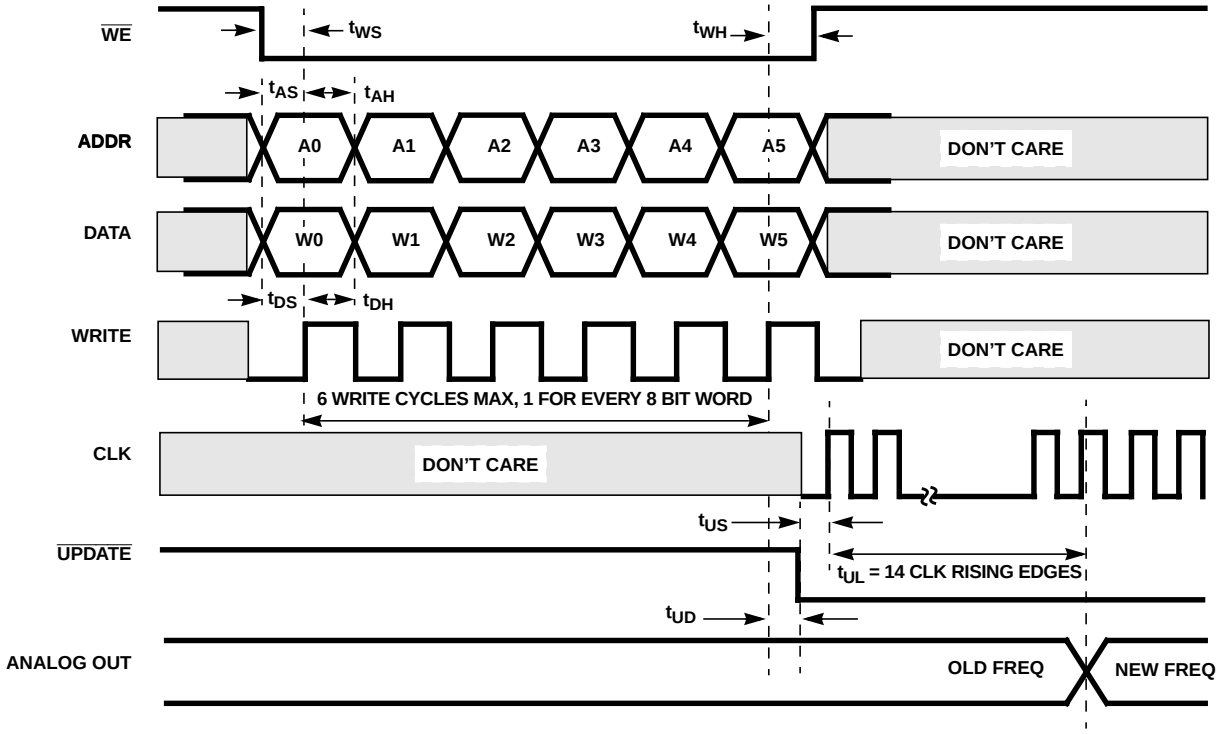


FIGURE 2. PARALLEL-LOAD METHOD 1, $\overline{\text{UPDATE}}$ ACTIVE AFTER LOADING REGISTERS ($\overline{\text{RESET}}$ = HIGH)

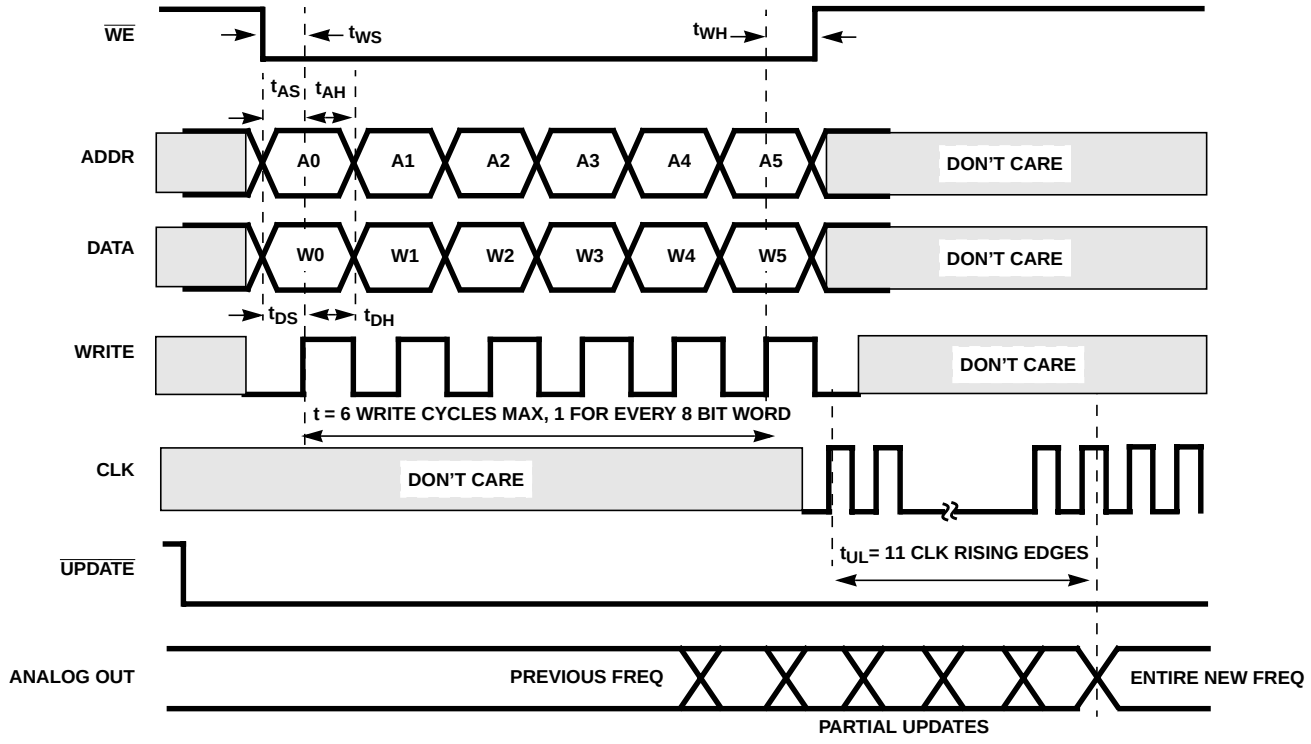


FIGURE 3. PARALLEL-LOAD METHOD 2, $\overline{\text{UPDATE}}$ ACTIVE WHILE LOADING REGISTERS ($\overline{\text{RESET}}$ = HIGH)

Timing Diagrams (Continued)

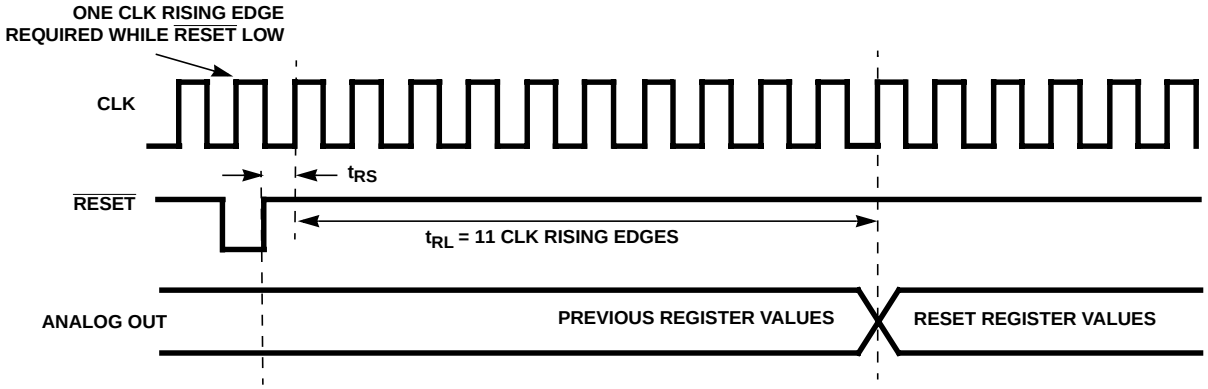


FIGURE 4. $\overline{\text{RESET}}$ TIMING AND LATENCY

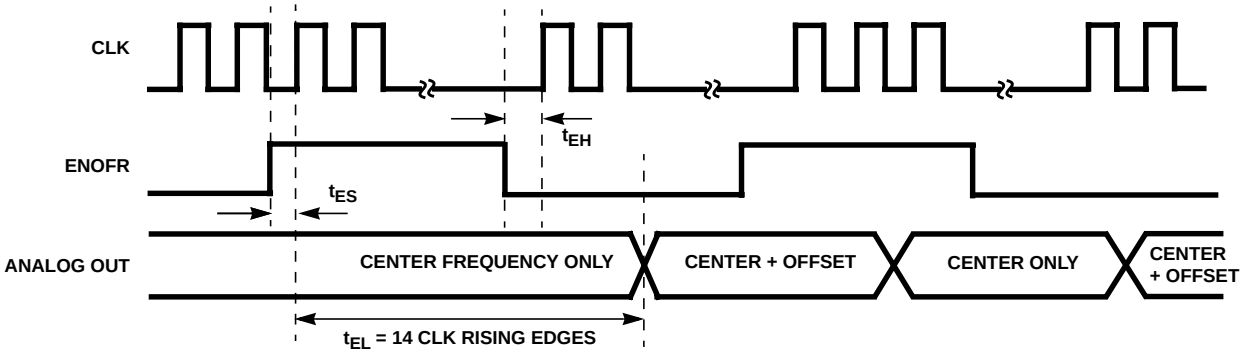


FIGURE 5. ENOFR (ENABLE OFFSET FREQUENCY REGISTER) TIMING AND LATENCY ($\overline{\text{RESET}}$ = HIGH)

Pin Description

PIN NO.	PIN NAME	TYPE	PIN DESCRIPTION
44-48, 1-3	C(7:0)	Input	8-bit Processor Input Data Bus. C7 is the MSB. Data is written to the control register selected on A(3:0) on the rising edge of WR when $\overline{\text{WE}}$ is active.
42	WR	Input	Write Clock For The Processor Interface. Parallel data is clocked into the chip on the rising edge of WR.
40	WE	Input	Write Enable. Active low. $\overline{\text{WE}}$ must be active when writing data to the chip.
35-38	A(3:0)	Input	Processor Interface Address Bus. These pins select the destination register for data on the C(7:0) bus. A3 is the MSB.
6	CLK	Clock	NCO and DAC Clock. The phase accumulator and DAC output update on the rising edge of this clock. CLK can be asynchronous to the WR clock.
8	RESET	Input	Reset. Active Low. Resets control registers to their default states (see register description table) and zeroes the feedback in the phase accumulator. $\overline{\text{UPDATE}}$ must be low for Reset to occur.
30	DGND	(Input)	Connect to DGND. Future serial clock input.
27	DGND	(Input)	Connect to DGND. Future serial data input.
32	DGND	(Input)	Connect to DGND. Future serial sync input.
9	UPDATE	Input	Active Low. Updates the active control registers only. It has no effect on the ENOFR or PH(1:0) pins. This pin is provided for updating an entire frequency word at once rather than byte by byte.

Pin Description (Continued)

PIN NO.	PIN NAME	TYPE	PIN DESCRIPTION
33, 34	PH(1:0)	Input	Phase Offset Bits. The phase of the output is shifted. If not used, these pins should be grounded. 00 – 0 degrees reference 01 – 90 degrees shift 10 – 180 degrees shift 11 – 270 degrees shift
4	ENOFR	Input	Enable Offset Frequency. Active High. When high, the offset frequency bus is enabled to the phase accumulator. When low, the offset frequency bus is zeroed. This pin does not affect the contents of the offset frequency registers. If not used, the pin should be grounded.
10	COMPOUT	Output	Comparator Output.
11	REFLO	Input	Connect to analog ground to enable the DAC's internal 1.2V reference or connect to AV_{DD} to disable the internal reference.
12	REFIO	Input	Reference voltage input for the DAC if internal reference is disabled. Recommend the use of a 0.1µF cap to ground from the REFIO pin when a DC reference voltage is used.
13	FSADJ		Full Scale Current Adjust for the DAC. Use a resistor to ground (R_{SET}) to adjust the full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}, where V_{FSADJ} equals the reference voltage.
14	COMP1		Noise reduction for the DAC. Connect a 0.1µF cap to AV_{DD} plane.
19	COMP2		Noise reduction for the DAC. Connect a 0.1µF cap to AGND plane.
18	IOUTA	Output	DAC Current Output.
17	IOUTB	Output	DAC Complementary Current Output.
20	AV_{DD}	Power	Analog Supply Voltage.
15, 16, 21, 24	AGND	Gnd	Analog Ground.
7, 26, 31, 43	DV_{DD}	Power	Digital Supply Voltage.
5, 25, 28, 29, 41	DGND	Gnd	Digital Ground.
22, 23	IN+, IN-	Input	Comparator Inputs. To power down the comparator, connect both of these pins to the analog power supply. This will conserve ~4mA of current.
39	NC	NC	No Connect.

Control Register Description

ADDRESS	BITS	DESCRIPTION	RESET STATE
0	7:0	Center frequency bits CF(7:0) (Least Significant Byte).	00 h
1	7:0	Center frequency bits CF(15:8).	00 h
2	7:0	Center frequency bits CF(23:16).	00 h
3	7:0	Center frequency bits CF(31:24).	00 h
4	7:0	Center frequency bits CF(39:32).	00 h
5	7:0	Center frequency bits CF(47:40) (MSByte). (Reset gives $f_{CLK}/4$ output).	40 h
6	7:0	Offset frequency bits OF(7:0) (LSByte).	00 h
7	7:0	Offset frequency bits OF(15:8).	00 h
8	7:0	Offset frequency bits OF(23:16).	00 h
9	7:0	Offset frequency bits OF(31:24).	00 h
10	7:0	Offset frequency bits OF(39:32).	00 h
11	7:0	Offset frequency bits OF(47:40) (MSByte).	00 h

Control Register Description (Continued)

ADDRESS	BITS	DESCRIPTION	RESET STATE
12	7:1	Bits 7 through 1 are Intersil reserved for future serial input control. Do Not Change.	00 h
	0	Center Frequency Enable. 1 = enable, 0 = center frequency disabled. This bit can be used to zero the center frequency (CF(47:0)) to the phase accumulator. This does not zero the processor interface registers - just the data path from the registers to the phase accumulator.	1 b
13	7:0	NCO control word.	F8 h
	7	Intersil reserved. Do Not Change.	1 b
	6	Intersil Reserved. Do Not Change. Future Serial output frequency register enable.	1 b
	5	Phase accumulator feedback. 0 = accumulator feedback disabled, 1 = accumulator enabled.	1 b
	4:0	Intersil reserved. Do Not Change.	11000 b
14	7:0	User should write 30 h to address 14 after $\overline{\text{RESET}}$.	10 h
	5:4	NCO-to-DAC setup and hold time control. Set to 11b.	01 b

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