

IN74HC221A

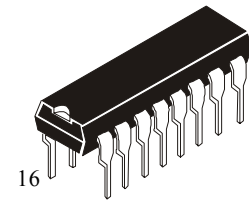
DUAL MONOSTABLE MULTIVIBRATOR

The IN74HC221A is identical in pinout to the LS/ALS221. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

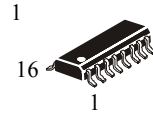
There are two trigger inputs, \overline{A} INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals

The device may also be triggered by using the \overline{RESET} input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor R_{EXT} and capacitor C_{EXT} . Taking RESET low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



N SUFFIX
PLASTIC

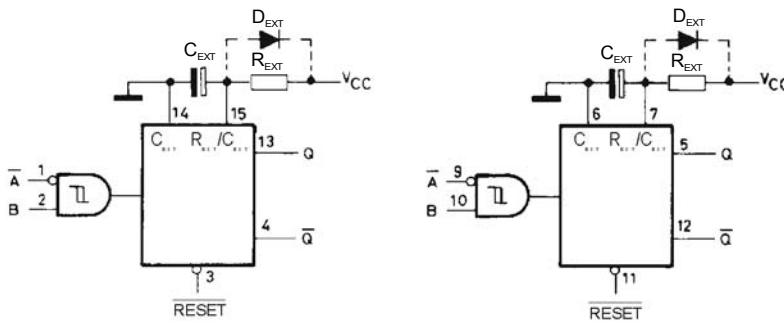


D SUFFIX
SOIC

ORDERING INFORMATION

IN74HC221AN Plastic
IN74HC221AD SOIC
IZ74HC221AZ Chip
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT

$\overline{1A}$	1	16	V_{CC}
1B	2	15	$1R_{EXT}/C_{EXT}$
$\overline{1RESET}$	3	14	$1C_{EXT}$
$\overline{1Q}$	4	13	$1Q$
2Q	5	12	$\overline{2Q}$
$2C_{EXT}$	6	11	$\overline{2RESET}$
$2R_{EXT}/C_{EXT}$	7	10	2B
GND	8	9	$\overline{2A}$

FUNCTION TABLE

Inputs			Outputs		Note
\overline{A}	B	\overline{RESET}	Q	\overline{Q}	
	H	H			Output Enable
X	L	H	L*	H*	Inhibit
H	X	H	L*	H*	Inhibit
L		H			Output Enable
L	H				Output Enable
X	X	L	L	H	Inhibit

X = don't care

* - except for monostable period

Note

(1) C_{EXT} , R_{EXT} , D_{EXT} are external components.

(2) D_{EXT} is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off C_x is discharged mainly through an internal parasitic diode. If C_x is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA.

IN74HC221A

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to $V_{CC} + 1.5$	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
I_{IN}	DC Input Current, per Pin \overline{A} , B, \overline{RESET} C_{EXT} , R_{EXT}	± 20 ± 30	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0*	6.0	V	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V	
T_A	Operating Temperature, All Package Types	-55	+125	°C	
t_r, t_f	Input Rise and Fall Time - \overline{RESET} (Figure 2)	$V_{CC} = 2.0$ V $V_{CC} = 4.5$ V $V_{CC} = 6.0$ V	0 0 0	1000 500 400	ns
	\overline{A} or B	-	No Limit		
R_X	External Timing Resistor	$V_{CC} < 4.5$ V	10	1000	k Ω
		$V_{CC} \geq 4.5$ V	2.0	1000	
C_X	External Timing Capacitor	0	No Limit	μ F	

*The IN74HC221 will function at 2.0 V but for optimum pulse width stability, V_{CC} should be above 3.0 V.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

IN74HC221A

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55°C to 25 °C	≤85 °C	≤125 °C	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} ≤ 0.1 V or V _{CC} =0.1 V I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.3 0.9 1.2	0.3 0.9 1.2	0.3 0.9 1.2	V
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} ≤ 0.1 V or V _{CC} =0.1 V I _{OUT} ≤ 20 μA	2.0 4.5 6.0	1.5 3.15 4.2	1.5 3.15 4.2	1.5 3.15 4.2	V
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5	0.26	0.33	0.4	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 5.2 mA	6.0	0.26	0.33	0.40	
V _{OH}	Minimum High- Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ -4.0 mA	4.5	3.98	3.84	3.70	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ -5.2 mA	6.0	5.48	5.34	5.2	
I _{IL}	Maximum Low- Level Output Current	V _{IL} =GND V _{IH} =V _{CC}	6.0	-0.1	-1.0	-1.0	μA
I _{IH}	Minimum High- Level Input Current	V _{IL} =GND V _{IH} =V _{CC}	6.0	0.1	1.0	1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package) Standby State	V _{IL} =GND V _{IH} =V _{CC} I _{OUT} =0 μA	6.0	8.0	80	160	μA
I _{CC1}	Maximum Supply Current (per Package) Active State	V _{IL} =GND	2.0	0.08	0.11	0.13	mA
		V _{IH} =V _{CC}	4.5	1.0	1.3	1.6	
		I _{OUT} =0 μA V _{IN} = 0.5 V _{CC}	6.0	2.0	2.6	3.2	

IN74HC221A

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Test Conditions	V _{CC} V	Guaranteed Limit			Unit
					-55°C to 25°C	≤85 °C	≤125 °C	
t _{PHL}	Maximum Propagation Delay	A, B - \bar{Q}	V _{IL} =0 V	2.0	180	225	270	ns
			V _{IH} =V _{CC}	4.5	36	45	54	
			t _{LH} =t _{HL} =6 ns	6.0	31	38	46	
		\overline{RESET} - Q	C _L =50 pF	2.0	180	225	270	
			C _{EXT} =0	4.5	36	45	54	
			R _{EXT} =5 kΩ	6.0	31	38	46	
		\overline{RESET} - \bar{Q}		2.0	195	245	295	
				4.5	39	49	59	
				6.0	33	42	50	
t _{PLH}	Maximum Propagation Delay	A, B - Q	V _{IL} =0 V	2.0	220	275	330	ns
			V _{IH} =V _{CC}	4.5	44	55	66	
			t _{LH} =t _{HL} =6 ns	6.0	37	47	56	
		\overline{RESET} - Q	C _L =50 pF	2.0	245	305	370	
			C _{EXT} =0	4.5	49	61	74	
			R _{EXT} =5 kΩ	6.0	42	52	63	
		\overline{RESET} - \bar{Q}		2.0	200	250	300	
				4.5	40	50	60	
				6.0	34	43	51	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)		V _{IL} =0 V V _{IH} =V _{CC} t _{LH} =t _{HL} =6 ns C _L =50 pF	2.0 4.5 6.0	75 16 14	95 20 17	110 22 20	ns
C _{IN}	Maximum Input Capacitance	A, B, \overline{RESET} C _x , R _x		-	10 20	10 20	10 20	pF
C _{PD}	Power Dissipation Capacitance (Per Multivibrator) P _D =C _{PD} V _{CC} ² f+I _{CC} V _{CC}			5.0	180*			pF
t _{rec}	Minimum Recovery Time, Inactive to A or B (Figure 2)		V _{IL} =0 V V _{IH} =V _{CC} t _{LH} =t _{HL} =6 ns C _L =50 pF	2.0 4.5 6.0	100 20 17	125 25 21	150 30 26	ns
t _w	Minimum Pulse Width	A, \overline{RESET}	V _{IL} =0 V	2.0	25	95	110	ns
			V _{IH} =V _{CC}	4.5	9	19	22	
			t _{LH} =t _{HL} =6 ns	6.0	7	16	19	
		B	C _L =50 pF	2.0	30	115	135	
			C _{EXT} =0	4.5	11	23	27	
			R _{EXT} =5 kΩ	6.0	9	20	23	
t _{wQ}	Minimum Pulse Width (Figure 4)		C _{EXT} = 0 pF	5.0	105*			ns
			R _{EXT} = 5 kΩ					
			C _{EXT} = 1 nF	2.0	0.80*			
			R _{EXT} = 10 kΩ	4.5	0.75*			
				6.0	0.70*			
			C _{EXT} = 1 μF	2.0	80*			
			R _{EXT} = 10 kΩ	4.5	75*			
				6.0	70*			

* T_A=25±10°C

IN74HC221A

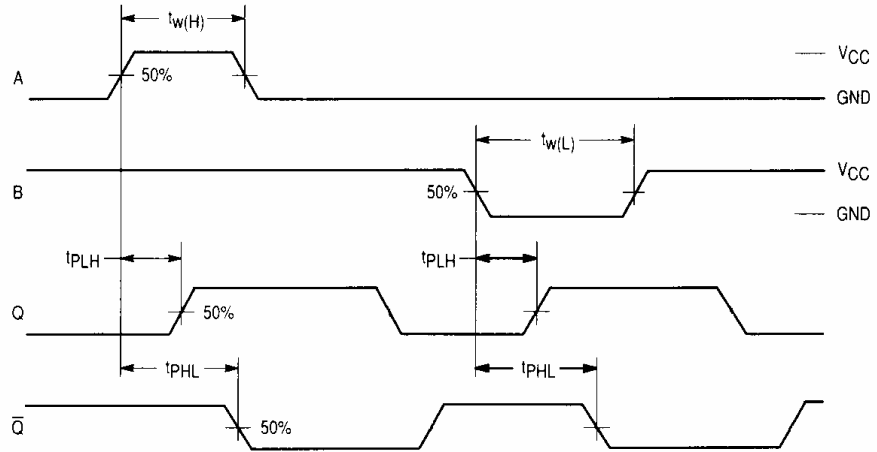


Figure 1. Switching Waveforms

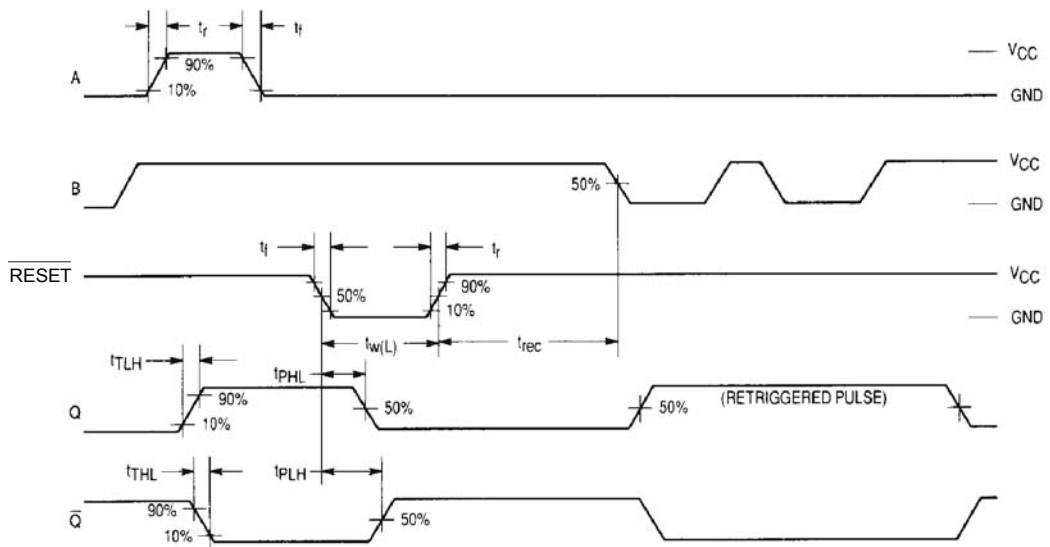
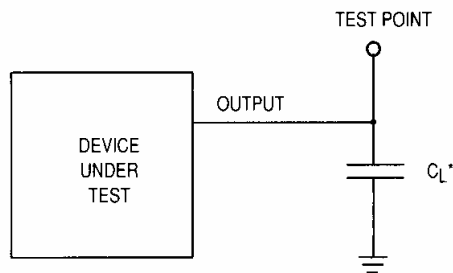


Figure 2. Switching Waveforms

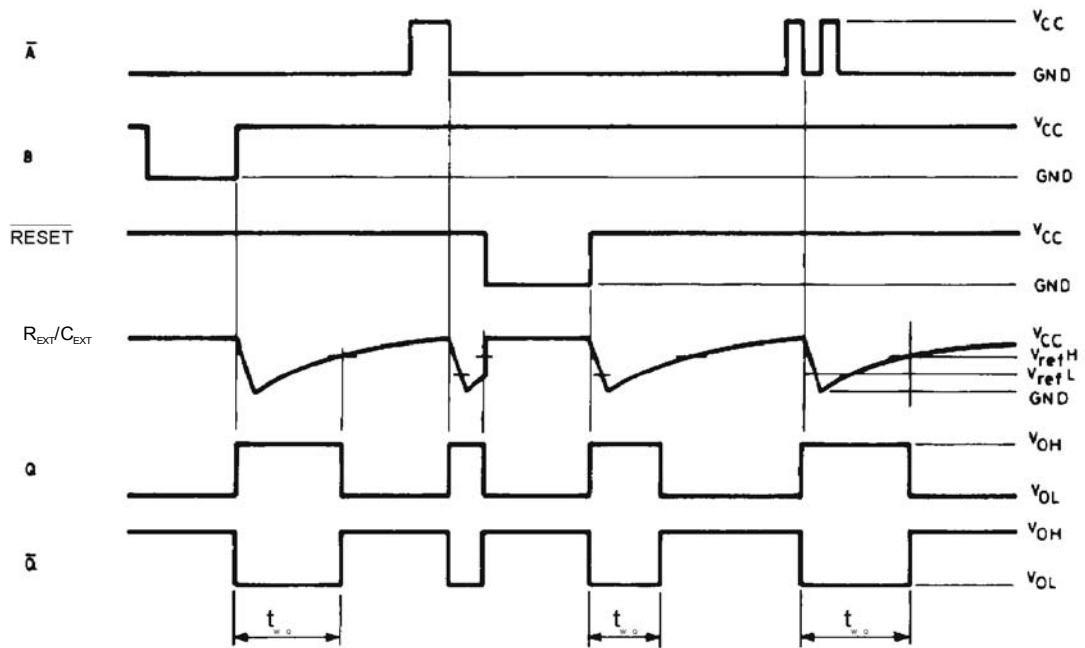


*Includes all probe and jig capacitance

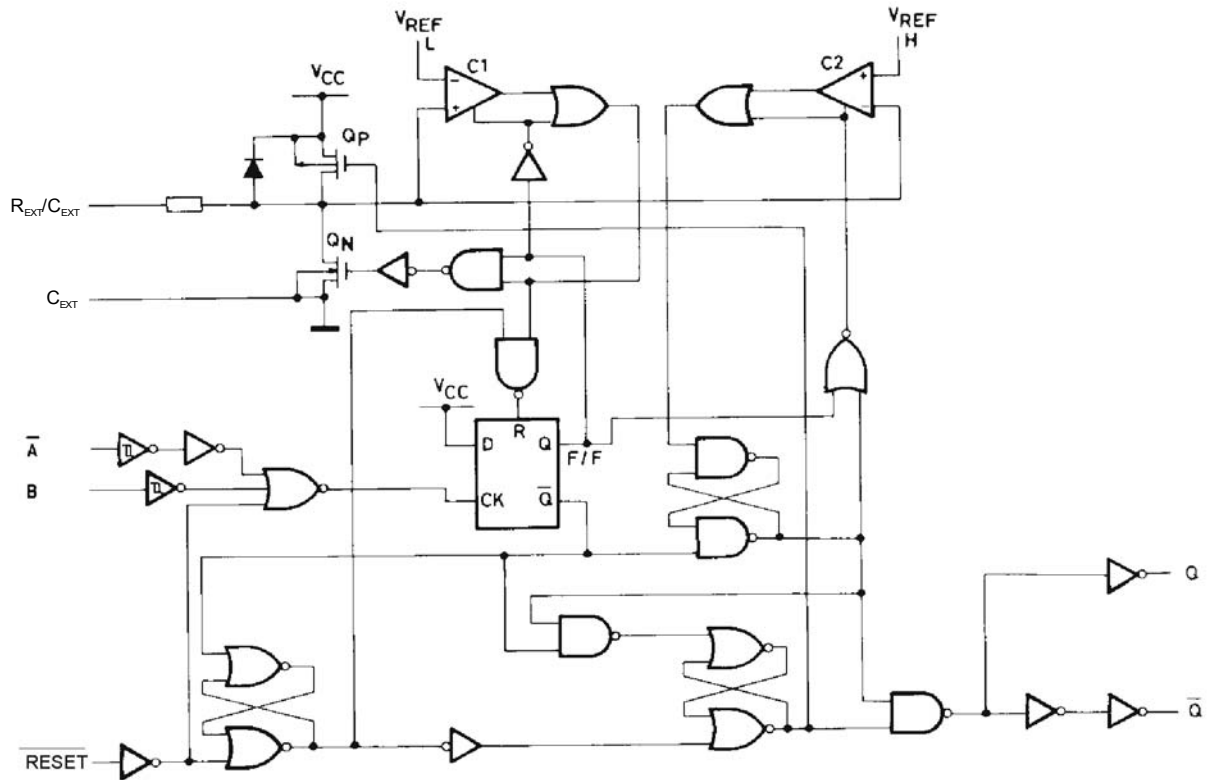
Figure 3. Test Circuit

IN74HC221A

TIMING DIAGRAM

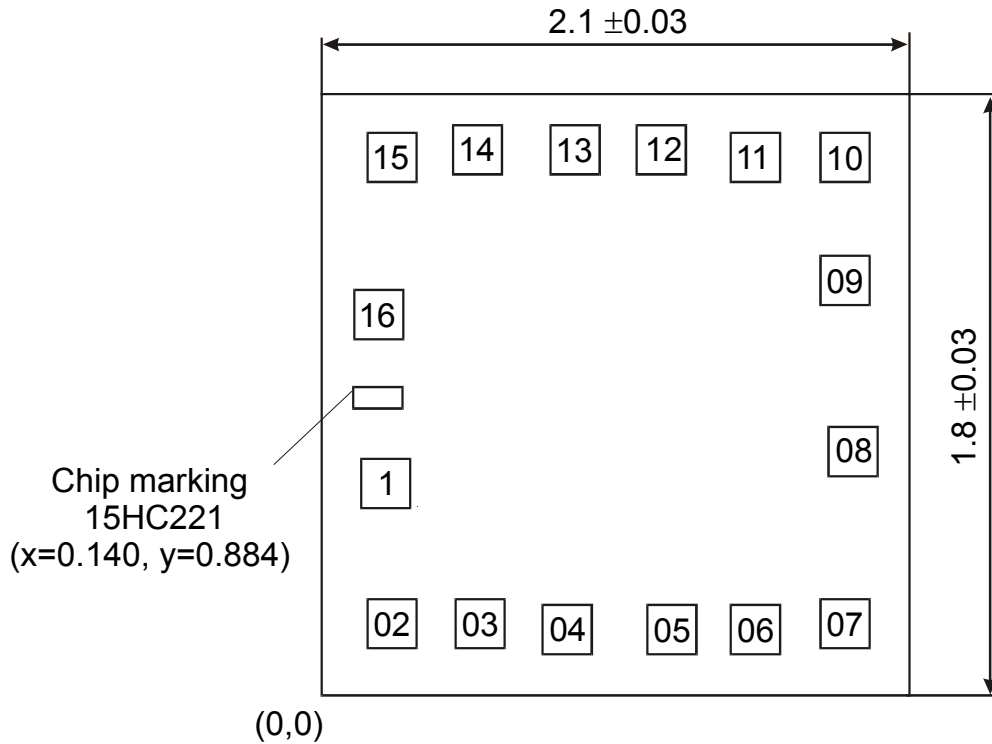


EXPANDED LOGIC DIAGRAM



IN74HC221A

CHIP PAD DIAGRAM IZ74HC221A



Pad size 0.106 x 0.106 mm (Pad size is given as per passivation layer)

Thickness of chip 0,46±0,02 mm

PAD LOCATION

Pad No	Symbol	X	Y
01	$\overline{1A}$	0.152	0.419
02	1B	0.157	0.132
03	$\overline{1RESET}$	0.458	0.134
04	$\overline{1Q}$	0.715	0.122
05	2Q	1.310	0.122
06	2C _{EXT}	1.585	0.122
07	2R _{EXT} /C _{EXT}	1.836	0.132
08	GND	1.847	0.690
09	2A	1.836	1.275
10	2B	1.837	1.562
11	$\overline{2RESET}$	1.536	1.560
12	2Q	1.278	1.572
13	1Q	0.684	1.572
14	1C _{EXT}	0.408	1.572
15	1R _{EXT} /C _{EXT}	0.158	1.562
16	V _{CC}	0.147	1.004