

# KH200

## Fast Settling, Wideband Operational Amplifier

### Features

- -3dB bandwidth of 95MHz
- 0.1% settling in 18ns
- 4000V/μs slew rate
- Low distortion, linear phase
- 3.6ns rise and fall times
- Direct replacement for CLC200

### Applications

- Fast, precision A to D, D to A conversion
- Baseband and video communications
- Radar, sonar, IF processors
- Laser drivers, photodiode preamps
- High-density buffering
- Graphic CRT composite video drive amp

### General Description

The KH200 operational amplifier achieves performance far superior to that of other high performance op amps. A current feedback design provides a bandwidth of DC-95MHz and an unprecedented settling time of 18nsec to 0.1%. And since thermal tail has been eliminated, the KH200 can be depended upon to settle fast and solidly maintain its level. Drive capability is also impressive at 24V<sub>pp</sub> and 100mA.

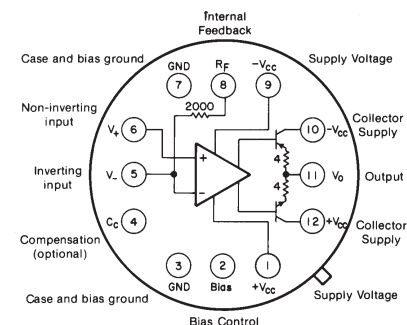
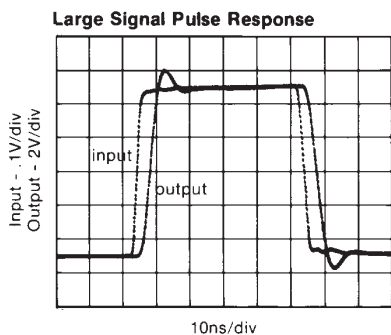
Using the KH200 is as easy as adding power supplies and a gain-setting resistor. The result is reliable, consistent performance because such characteristics as bandwidth and settling time are virtually independent of gain setting. Unlike conventional op amp designs where the optimum gain bandwidth product occurs at a high gain, minimum settling time at a gain of -1, maximum slew rate at a gain of +1, et cetera, the KH200 offers predictable response at gain settings from ±1 to ±50. This, coupled with consistent performance from unit to unit with no external compensation, makes the KH200 a real time and cost-saver in design and production situations alike.

Minimizing settling time was a design goal of the KH200. Settling time is one of the most demanding of all op amp requirements since it is affected by the op amp's bandwidth, gain flatness, and harmonic distortion. The result of this effort is an amplifier fast enough for the most demanding high speed D to A converters and "flash" A to D converters.

The superior slew rate and rise and fall times of the KH200 make it an ideal amplifier for a broad range of pulse, analog, and digital applications. Flat gain and phase response from DC to beyond 50MHz ensure distortion levels well below those of other op amps. A full power bandwidth of 20MHz eliminates the need for power buffers in many applications.

The KH200 is constructed using thin film resistor/bipolar transistor technology, and is available in the following versions:

KH200AI	-25°C to +85°C	12-pin TO-8 can
KH200AK	-55°C to +125°C	12-pin TO-8 can, features burn-in and hermetic testing
KH200AM	-55°C to +125°C	12-pin TO-8 can, environmentally screened and electronically tested to MIL-STD-883
KH200HXC	-55°C to +125°C	SMD#: 5962-8991001XC
KH200HXA	-55°C to +125°C	SMD#: 5962-8991001XA



Pin 8 provides access to a 2000 ohm feedback resistor. Pin 2 allows the user to reduce the amplifier supply current or to turn the amplifier off completely.

### Typical Performance

parameter	gain setting						units
	+2	+20	+50	-2	-20	-50	
-3dB bandwidth	150	95	75	100	95	90	MHz
rise time (20V)	—	4	5	4	4	4	ns
slew rate	4	4	4	4	4	4	V/ns
settling time (0.1%)	—	18	23	18	18	23	ns

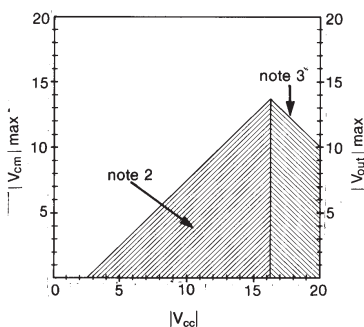
### KH200 Electrical Characteristics (A<sub>v</sub> = +20V, V<sub>CC</sub> = ±15V, R<sub>L</sub> = 200Ω, R<sub>f</sub> = 2000Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	MAX & MIN RATINGS <sup>1</sup>				UNITS	SYMBOL
Ambient Temperature	KH200A1	+25°C	-25°C	+25°C	+85°C			
Ambient Temperature	KH200AK/AM/HXC/HXA	+25°C	-55°C	+25°C	+125°C			
<b>FREQUENCY DOMAIN RESPONSE</b>								
+ -3dB bandwidth	V <sub>out</sub> < 2V <sub>pp</sub>	95	> 85	> 85	> 80	MHz	SSBW	
gain flatness at	V <sub>out</sub> < 2V <sub>pp</sub>							
+ peaking	0.1 to 25MHz	0	< 0.4	< 0.3	< 0.4	dB	GFPL	
+ peaking	>25MHz	0.2	< 0.8	< 0.6	< 1.0	dB	GFPH	
+ rolloff	at 50MHz	—	< 0.6	< 0.4	< 0.6	dB	GFR	
group delay	to 50MHz	4.2 ± 0.5	—	—	—	ns	GD	
linear phase deviation	to 50MHz	1	< 2	< 2	< 2	°	LPD	
reverse isolation	to 50MHz							
non-inverting		60	> 50	> 50	> 50	dB	RINI	
inverting		45	> 35	> 35	> 35	dB	RIIN	
<b>TIME DOMAIN RESPONSE</b>								
rise and fall time	2V step	3.6	< 4.1	< 4.1	< 4.4	ns	TRS	
	20V step	4	< 5	< 5	< 6	ns	TRL	
settling time to .02%	10V step <sup>4</sup>	25	—	—	—	ns	TSP	
to .1%	10V step <sup>4</sup>	18	< 25	< 25	< 25	ns	TS	
overshoot	10V step	5	< 12	< 10	< 10	%	OS	
slew rate (overdriven input)		4	> 3	> 3	> 3	V/ns	SR	
overload recovery								
<50ns pulse, 200% overdrive		25	—	—	—	ns	OR	
<b>DISTORTION AND NOISE RESPONSE</b>								
+ 2nd harmonic distortion	2V <sub>pp</sub> , 20MHz	-52	< -45	< -45	< -45	dBc	HD2	
+ 3rd harmonic distortion	2V <sub>pp</sub> , 20MHz	-58	< -50	< -50	< -50	dBc	HD3	
equivalent noise input								
noise floor	>100kHz	-156	< -150	< -150	< -150	dBm(1Hz)	SNF	
integrated noise	1kHz to 100MHz	35	< 70	< 70	< 70	μV	INV	
noise floor	>5MHz	-156	< -150	< -150	< -150	dBm(1Hz)	SNF	
integrated noise	5MHz to 100MHz	35	< 70	< 70	< 70	μV	INV	
<b>STATIC DC PERFORMANCE</b>								
*input offset voltage		10	< 25	< 25	< 25	mV	VIO	
average temperature coefficient		35	< 120	< 120	< 120	μV/°C	DVIO	
*input bias current	non-inverting	10	< 40	< 30	< 40	μA	IBN	
average temperature coefficient		20	< 125	< 125	< 125	nA/°C	DIBN	
*input bias current	inverting	20	< 70	< 50	< 70	μA	IBI	
average temperature coefficient		70	< 250	< 250	< 250	nA/°C	DIBI	
*power supply rejection ratio		55	> 45	> 45	> 45	dB	PSRR	
common mode rejection ratio		46	> 40	> 40	> 40	dB	CMRR	
*supply current	no load	29	< 36	< 34	< 36	mA	ICC	
<b>MISCELLANEOUS PERFORMANCE</b>								
non-inverting input	resistance	250	> 100	> 100	> 100	kΩ	RIN	
	capacitance	2.4	< 3	< 3	< 3	pF	CIN	
output impedance	at DC	—	< 0.1	< 0.1	< 0.1	Ω	RO	
	at 50MHz	1, 35	—	—	—	Ω, nH	ZO	
output voltage range	no load	±12	> ±11	> ±11	> ±11	V	VO	
internal feedback resistor	absolute tolerance	< 0.4	—	—	—	%	RFA	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Absolute Maximum Ratings

Common Mode and Output Voltage Limits



- supply voltage (V<sub>cc</sub>) ±20V
- output current ±100mA
- thermal resistance (θ<sub>ca</sub>) see thermal model
- junction temperature +175°C
- operating temperature AI: -25°C to +85°C
- AK, AM, HXC, HXA: -55°C to +125°C
- storage temperature -65°C to +150°C
- lead temperature (soldering 10s) +300°C

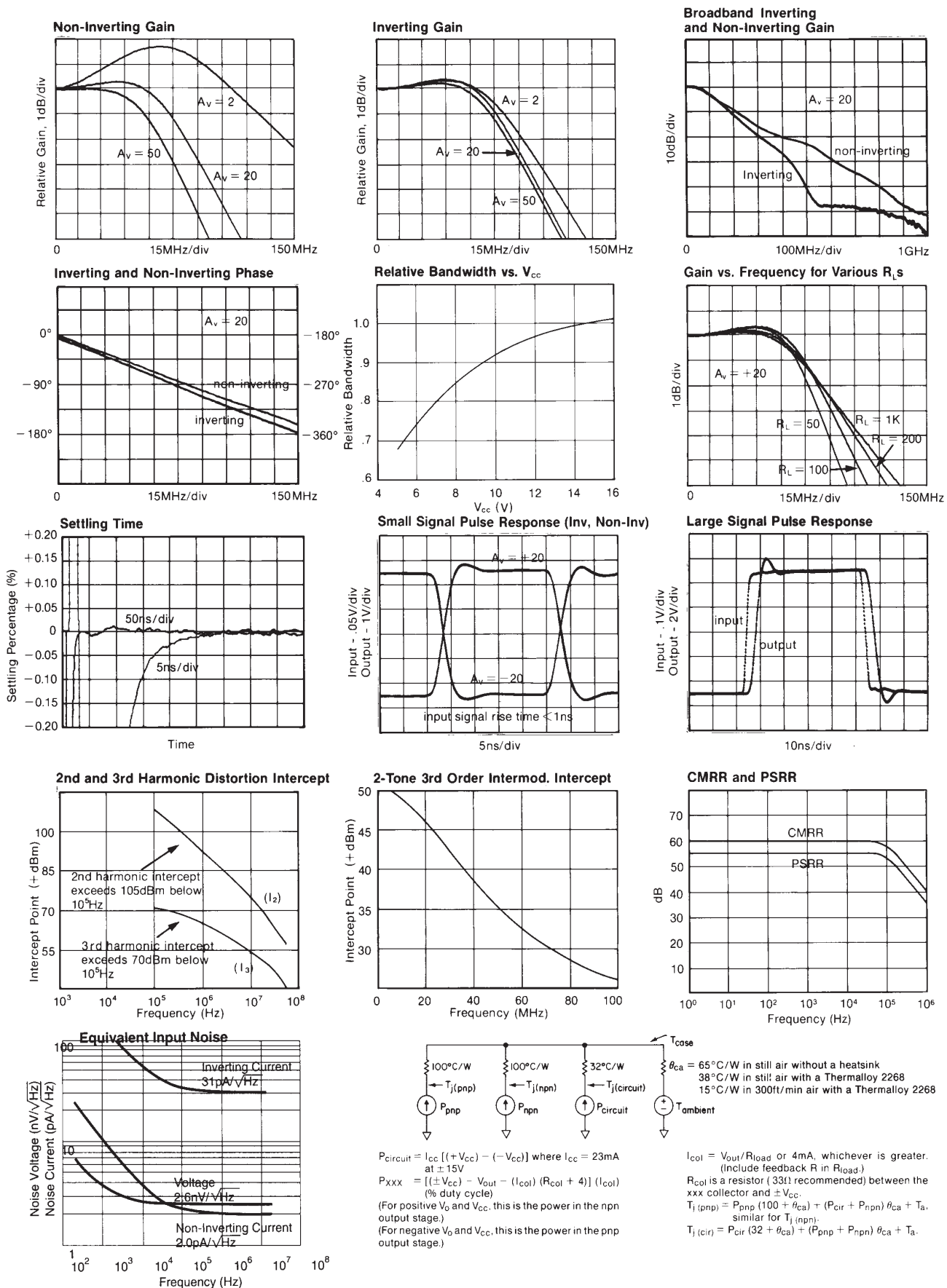
**note 1:** \* AI, AK, AM, HXC, HXA 100% tested at 25°C.  
 † AK, AM, HXC, HXA 100% tested at +25°C & sample tested at -55°C & +125°C.  
 ‡ AI sample tested at +25°C.

**note 2:** This rating protects against damage to the input stage caused by saturation of either the input or output stages. Under transient conditions not exceeding 1μs (duty cycle not exceeding 10%), maximum input voltage may be as large as twice the maximum. V<sub>cm</sub> should never exceed V<sub>cc</sub>. (V<sub>cm</sub> is the voltage at the non-inverting input, pin 6.)

**note 3:** This rating protects against exceeding transistor collector-emitter breakdown ratings. Recommended V<sub>cc</sub> is ±15V.

**note 4:** Settling time specifications require the use of an external feedback resistor (2000Ω).

# KH200 Performance Characteristics ( $A_v = +20^\circ\text{C}$ , $A_v = \pm 20$ , $V_{CC} = \pm 15\text{V}$ , $R_L = 200\Omega$ ; unless noted)



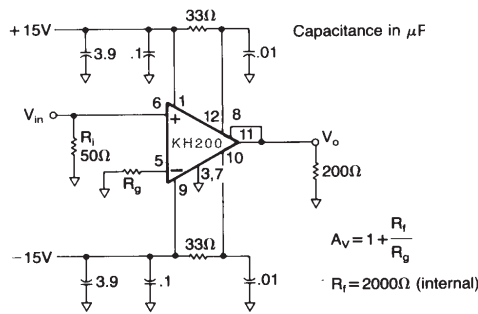


Figure 1: suggested non-inverting gain circuit

**Controlling Bandwidth and Passband Response**

As with any op amp, the ratio of the two feedback resistors  $R_f$  and  $R_g$  determines the gain of the KH200. Unlike conventional op amps, however, the closed loop pole-zero response of the KH200 is affected very little by the value of  $R_g$ .  $R_g$  scales the magnitude of the gain, but does not change the value of the feedback. This is possible due to a proprietary circuit topology.  $R_f$  does influence the feedback and so the KH200 has been internally compensated for optimum performance with  $R_f = 2000\Omega$ , but any value of  $R_f > 1k\Omega$  may be used with a single capacitor placed between pins 4 and 5 for compensation. See Table 1. As  $R_f$  decreases,  $C_c$  must increase to maintain flat gain. Slew rate will decrease slightly with increasing  $C_c$ , but other parameters such as bandwidth, settling time, and phase linearity will improve. Large values of  $R_f$  and  $C_c$  can be used together or separately to reduce the bandwidth. This may be desirable for reducing the bandwidth in applications not requiring the full frequency response available although this may cause the output noise to increase at low gains.

Table 1: Bandwidth versus  $R_f$  and  $C_c$

$R_f$ (k $\Omega$ )	$C_c$ (pF)	$f \pm 0.3dB$ (MHz)	$f - 3.0dB$ (MHz)
10.0	0	5	15
5.0	0	10	30
3.0	0	20	60
2.0	0	50	100
1.5	0.25	70	130
1.0	0.50	120	170

**Layout Considerations**

To assure optimum performance the user should follow good layout practices which minimize the unwanted coupling of signals between nodes. During initial breadboarding of the circuit, use direct point to point wiring, keeping the lead lengths to less than .25". The use of solid, unbroken ground plane is helpful. Avoid wire-wrap type pc boards and methods. Sockets with small, short pin receptacles may be used with minimal performance degradation although their use is not recommended.

During pc board layout, keep all traces short and direct. The resistive body of  $R_g$  should be as close as possible to pin 5 to minimize capacitance at that point. For the same reason, remove ground plane from the vicinity of pins 5 and 6. In other areas, use as much ground plane as possible on one side of the board. It is especially important to provide a ground return path for current from the load resistor to the power supply bypass capacitors. Ceramic capacitors of .01 to .1 $\mu$ F (with short leads) should be less than .15 inches from pins 1 and 9. Larger tantalum capacitors should be placed within one inch of these pins.  $V_{cc}$  connections to pins 10 and 12 can be made directly from pins 9 and 1, but better supply rejection and settling time are obtained if they are separately bypassed as in Figures 1 and 2. To prevent signal distortion caused by reflections from impedance mismatches, use terminated microstrip of coaxial cable when the signal must traverse more than a few inches.

Since the pc board forms such an important part of the circuit, much time can be saved if prototype boards of any high frequency sections are built and tested early in the design phase. Evaluation boards designed for either inverting or non-inverting gains are available.

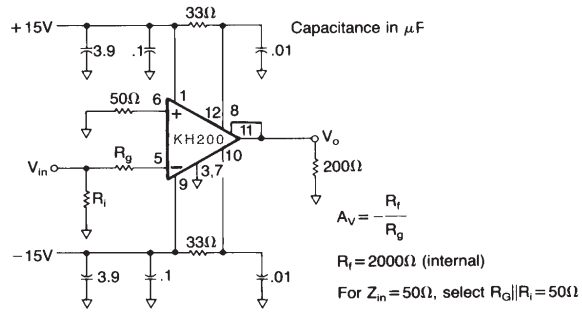


Figure 2: suggested inverting gain circuit

**Distortion and Amplification Fidelity**

The graphs of intercept point versus frequency on the preceding page make it easy to predict the distortion at any frequency, given the output voltage of the KH200. First, convert the output voltage ( $V_o$ ) to  $V_{RMS} = (V_{pp}/2\sqrt{2})$  and then to  $P = (10\log_{10}(20V_{RMS}^2))$  to get output power in dBm. At the frequency of interest, its 2nd harmonic will be  $S_2 = (I_2 - P)$  dB below the level of P. Its third harmonic will be  $S_3 = 2(I_3 - P)$  dB below P, as will the two-tone third order intermodulation products. These approximations are useful for  $P < -1$  dB compression levels.

Approximate noise figure can be determined for the KH200 using the Equivalent Input Noise graph on the preceding page. The following equation can be used to determine noise figure (F) in dB.

$$F = 10\log \left[ 1 + \frac{v_n^2 + \frac{i_n^2 R_F^2}{A_v^2}}{4kTR_s \Delta f} \right]$$

where  $v_n$  is the rms noise voltage and  $i_n$  is the rms noise current at the inverting node. Beyond the breakpoint of the curves (i.e., where they are flat), broadband noise figure equals spot noise figure, so  $\Delta f$  should equal one (1) and  $v_n$  and  $i_n$  should be read directly off the graph. Below the breakpoint, the noise must be integrated and  $\Delta f$  set to the appropriate bandwidth.

For linear operation of the KH200 at large output voltage swings (DC component not included) and at high frequencies, observe the (AC output voltage)  $\times$  (frequency) product specification of 400V  $\cdot$  MHz. Exceeding this rating will cause the signal to be greatly distorted as the amplifier bias control circuit reduces the current available for slewing to prevent damage. At frequencies and voltages within this range the excess slew rate and bandwidth available will ensure the highest possible degree of amplified signal fidelity.

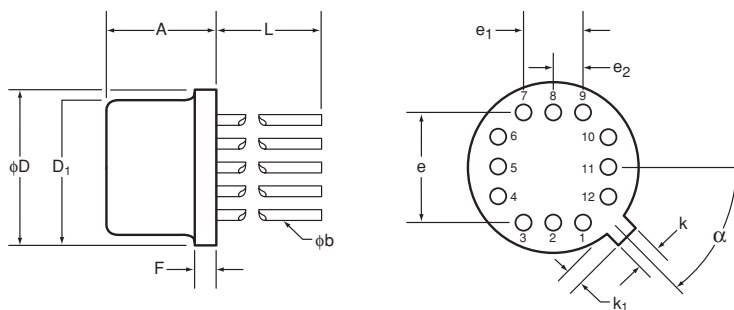
**Operation with Reduced Bias Current**

Placing a resistor between pins 1 and 2 will cause the KH200 bias current to be reduced. A value of 20K will cause only a slight reduction, 3K will almost halve the current, while less than 1K will reduce bias to about 5mA and the amplifier will be off. In this condition, the input signal will be greatly attenuated. In the reduced bias, on condition, bandwidth will be roughly proportional to the reduction in bias current. A mechanical or semiconductor switch can be used to turn the amplifier off. Any connection which would cause current to flow out of pin 2 will result in increased bias current and may lead to device destruction from overheating and excessive current.

**Thermal Considerations**

At high ambient temperatures or large internal power dissipations, heat sinking is required to maintain acceptable junction temperatures. Use the thermal model on the previous page to determine junction temperatures. Many styles of heat sinks are available for TO-8 packages; the Thermalloy 2240 and 2268 are good examples. Some heat sinks are the radial fin type which cover the pc board and may interfere with external components. An excellent solution to this problem is to use surface mounted resistors and capacitors. They have a very low profile and actually improve high frequency performance. For use of these heat sinks with conventional components, a .1" high spacer can be inserted under the TO-8 package to allow sufficient clearance.

### KH200 Package Dimensions



TO-8				
SYMBOL	INCHES		MILIMETERS	
	Minimum	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
$\phi b$	0.016	0.019	0.41	0.48
$\phi D$	0.595	0.605	15.11	15.37
$\phi D_1$	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e <sub>1</sub>	0.200 BSC		5.08 BSC	
e <sub>2</sub>	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k <sub>1</sub>	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
$\alpha$	45° BSC		45° BSC	

**NOTES:**

- Seal: cap weld
- Lead finish: gold per MIL-M-38510
- Package composition:
  - Package: metal
  - Lid: Type A per MIL-M-38510

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