

**KM28C64A/KM28C65A****CMOS EEPROM****8K x 8 Bit CMOS Electrically Erasable PROM****FEATURES**

- **Operating Temperature Range**
  - KM28C64A/65A: Commercial
  - KM28C64AI/65AI: Industrial
- **Simple Byte Write & Page Write**
  - Single TTL Level Write Signal
  - Internal Address and Data Latch
  - Automatic Internal Erase-Before-Write
  - Ready/Busy Output Pin (KM28C65A)
- **Fast Write Cycle Time**
  - 64-Byte Page Write Operation
  - 5ms Byte and Page Write Cycle Time
  - Complete Memory Rewrite: 0.7 seconds
- **Data-Polling and Toggle bit for End of Write Detection**
- **Single 5 volt Supply**
- **Fast Access Time: 120ns**
- **Power: 100 $\mu$ A—Standby (max.)**  
**40mA—Operating (max.)**
- **Hardware and Software Data Protection**
- **Reliable CMOS Floating-Gate Technology**
  - Endurance: 100,000 Cycle
  - Data Retention: 10 years
- **JEDEC Byte-wide Memory Pinout**

**GENERAL DESCRIPTION**

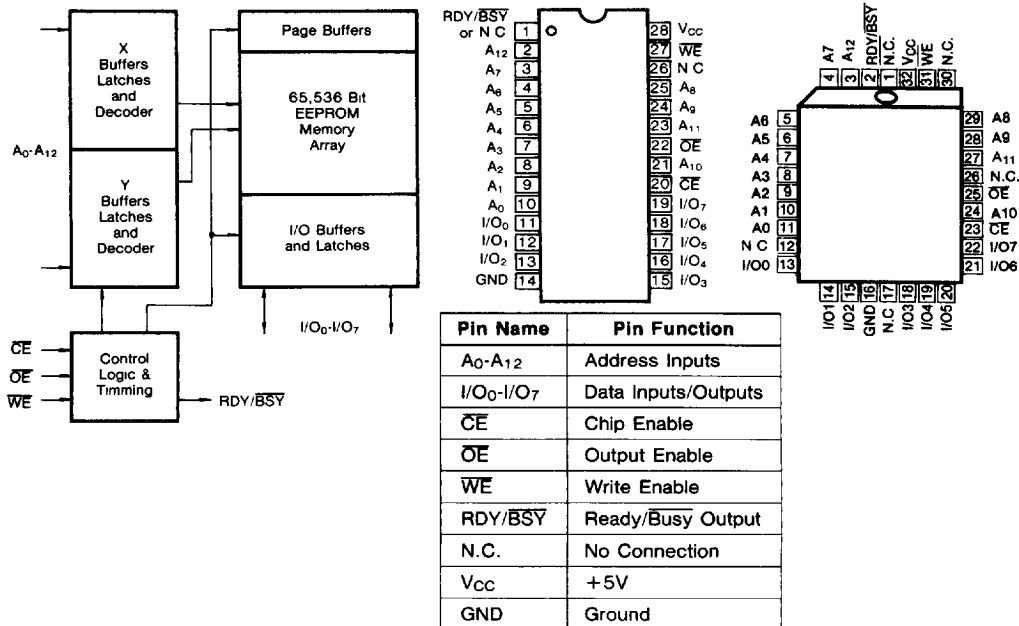
The KM28C64A/65A is a 8,192x8 bit Electrically Erasable Programmable Read Only Memory. It is fabricated with the floating-gate CMOS technology using Fowler-Nordheim tunneling for erasing and programming.

Writing data into the KM28C64A/65A is very simple. The internally self-timed writing cycle latches both address and data to provide a free system bus during the 5ms write period. A 64-byte page write enables an entire chip written in 0.7 seconds.

The KM28C64A/65A also features Data-polling and a Toggle bit schemes that signal the processor the early completion of a write cycle without requiring any external hardware. The KM28C65A features Read/Busy which is a hardware scheme to signal the status of the write operation and is especially useful in interrupt driven systems.

The KM28C64A/65A is designed for applications up to 100,000 write cycles per byte. Its on-chip Error Checking and Correction scheme improves the endurance to over 100,000 write cycles.

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**FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION**

## KM28C64A/KM28C65A

## CMOS EEPROM

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub>	-0.3 to +7.0	V
Temperature Under Bias	Com.	-10 to +125	°C
	Ind.	-65 to +150	°C
Storage Temperature	T <sub>stg</sub>	-65 to +150	°C
Short Circuit Output Current	I <sub>OS</sub>	5	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

KM28C64A/65A : Voltage reference to V<sub>SS</sub>, T<sub>A</sub>=0°C to +70°C

KM28C64AI/65AI : Voltage reference to V<sub>SS</sub>, T<sub>A</sub>=-40°C to +85°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V

## DC OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Operating Current	I <sub>CC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$ , $\overline{WE} = V_{IH}$ , all I/O's open (Note 1)	—	40	mA
Standby Current (TTL)	I <sub>SB1</sub>	$\overline{CE} = V_{IH}$ , all I/O's = open	—	1	mA
Standby Current (CMOS)	I <sub>SB2</sub>	$\overline{CE} = V_{CC} - 0.2$ , all I/O's = open	—	100	μA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0 to 5.5V	—	10	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>OUT</sub> = 0 to 5.5V	—	10	μA
Input High Voltage, all Inputs	V <sub>IH</sub>		2.0	V <sub>CC</sub> + 0.3	V
Input Low Voltage, all Inputs	V <sub>IL</sub>		-0.3	0.8	V
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> = -400μA	2.4	—	V
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA	—	0.4	V
Write Inhibit V <sub>CC</sub> Level	V <sub>WI</sub>		3.0	—	V

Note 1: All address toggling from V<sub>IL</sub> to V<sub>IH</sub> at 8.4MHz.

CAPACITANCE (T<sub>A</sub>=25°C, f=1.0 MHz)

Item	Symbol	Conditions	Min	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>IL</sub> =0V	—	10	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	—	6	pF

Note: Capacitance is periodically sampled and not 100% tested.



**KM28C64A/KM28C65A****CMOS EEPROM****MODE SELECTION**

CE	OE	WE	Mode	I/O	Power
L	L	H	Read	D <sub>OUT</sub>	Active
L	H	L	Write	D <sub>IN</sub>	Active
L	L	H	Data Polling	I/O <sub>7</sub> = $\overline{D}_7$	Active
			Toggle Bit	I/O <sub>6</sub>	Active
H	X	X	Standby and Write Inhibit	High-Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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**AC CHARACTERISTICS**KM28C64A/65A : T<sub>A</sub>=0°C to +70°C V<sub>CC</sub>=5V±10%, unless otherwise notedKM28C64AI/65AI: T<sub>A</sub>=-40°C to +85°C V<sub>CC</sub>=5V±10%, unless otherwise noted**TEST CONDITIONS**

Parameter	Value
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	20 ns
Input and Output Timing measurement Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C <sub>L</sub> =100pF

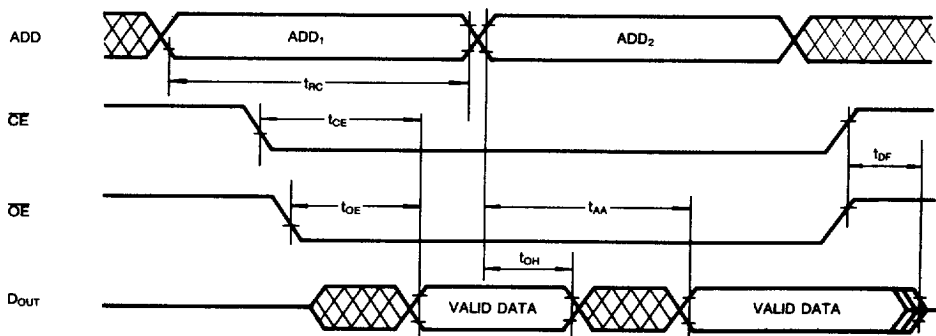
**READ CYCLE**

Parameter	Symbol	KM28C64A-12		KM28C64A-15		KM28C64A-20		KM28C64A-25		Unit
		KM28C65A-12		KM28C65A-15		KM28C65A-20		KM28C65A-25		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	120		150		200		250		ns
Chip Enable Access Time	t <sub>CE</sub>		120		150		200		250	ns
Address Access Time	t <sub>AA</sub>		120		150		200		250	ns
Output Enable Access Time	t <sub>OE</sub>		60		80		100		120	ns
Output or Chip Disable to Output High-Z	t <sub>DF</sub>	0	50	0	50	0	50	0	50	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		0		ns

**KM28C64A/KM28C65A****CMOS EEPROM****WRITE CYCLE**

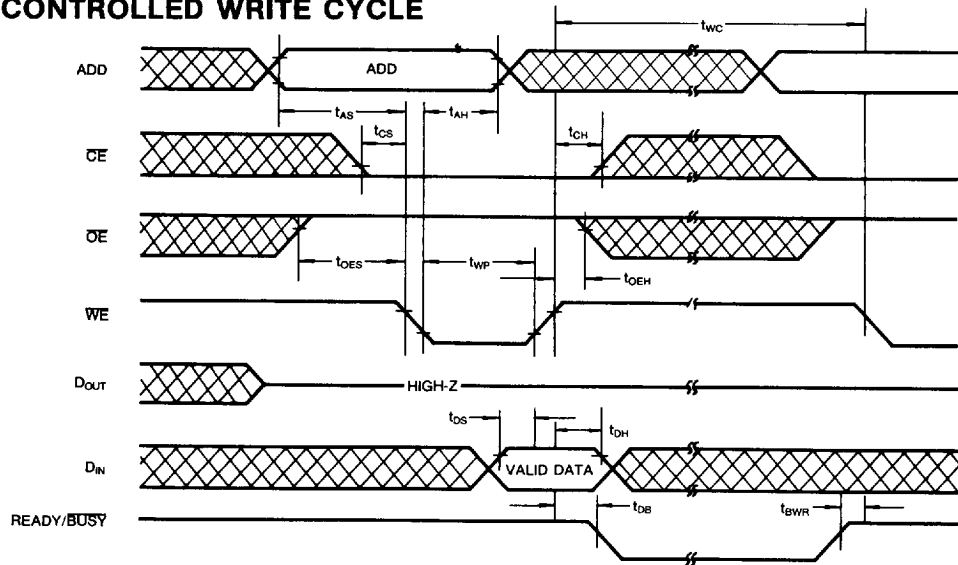
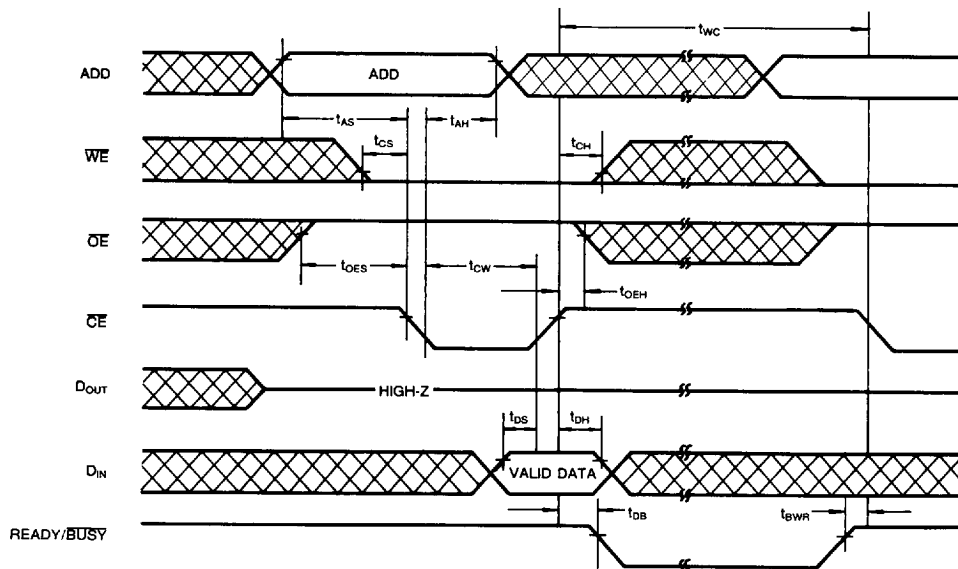
Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t <sub>WC</sub>		5	ms
Address Set-Up Time	t <sub>AS</sub>	0		ns
Address Hold Time	t <sub>AH</sub>	80		ns
Write Set-Up Time	t <sub>CS</sub>	0		ns
Write Hold Time	t <sub>CH</sub>	0		ns
CE Pulse Width	t <sub>CW</sub>	100		ns
Output Enable Set-Up Time	t <sub>OES</sub>	10		ns
Output Enable Hold Time	t <sub>OEH</sub>	10		ns
WE Pulse Width	t <sub>WP</sub>	100		ns
Data Set-Up Time	t <sub>DS</sub>	50		ns
Data Hold Time	t <sub>DH</sub>	0		ns
Time to Device Busy	t <sub>DB</sub>		100	ns
Busy to Write Recovery Time	t <sub>BWR</sub>	50		ns
Byte Load Cycle Time	t <sub>BLC</sub>	0.2	150	μs
Last Byte Loaded to Data Polling	t <sub>LP</sub>		200	ns

Note: The timer for t<sub>BLC</sub> is reset at a falling edge of WE and restarts at rising edge of WE.

**TIMING DIAGRAM****READ CYCLE (WE=V<sub>IH</sub>)**

## KM28C64A/KM28C65A

## CMOS EEPROM

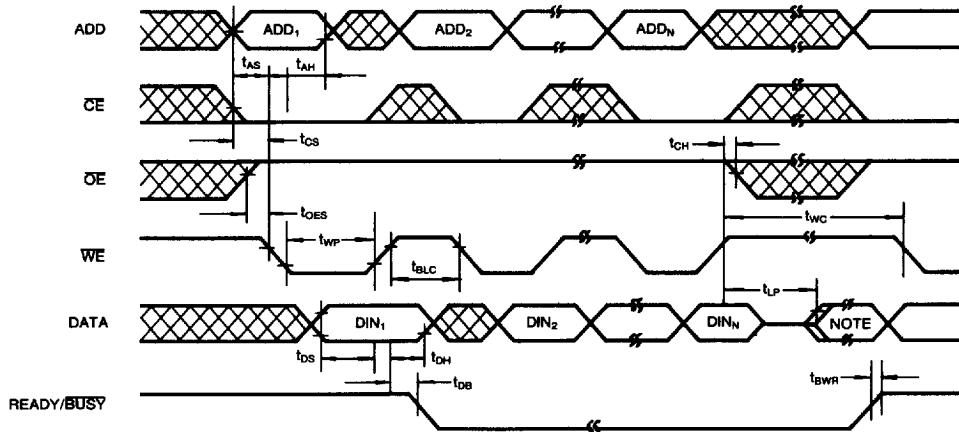
**TIMING DIAGRAM (Continued)**  
**WE CONTROLLED WRITE CYCLE**

**CE CONTROLLED WRITE CYCLE**


## KM28C64A/KM28C65A

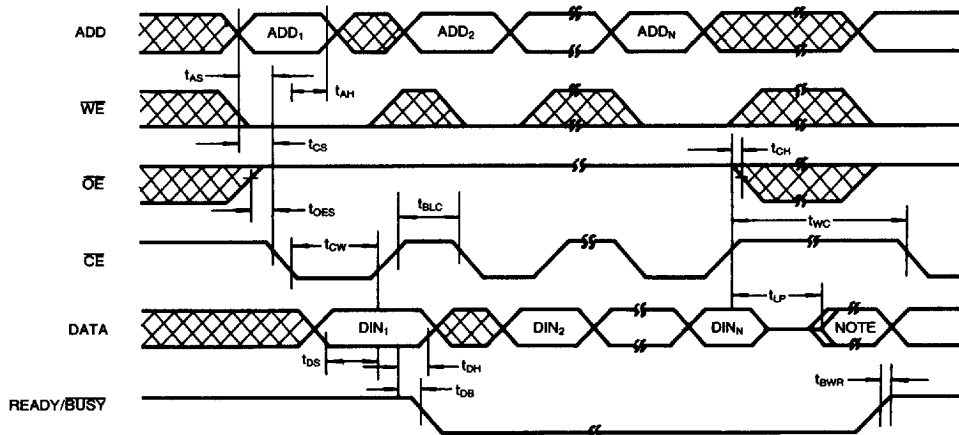
## CMOS EEPROM

## TIMING DIAGRAMS (Continued)

## PAGE MODE WRITE (WE CONTROLLED WRITE CYCLE)



## PAGE MODE WRITE (CE CONTROLLED WRITE CYCLE)



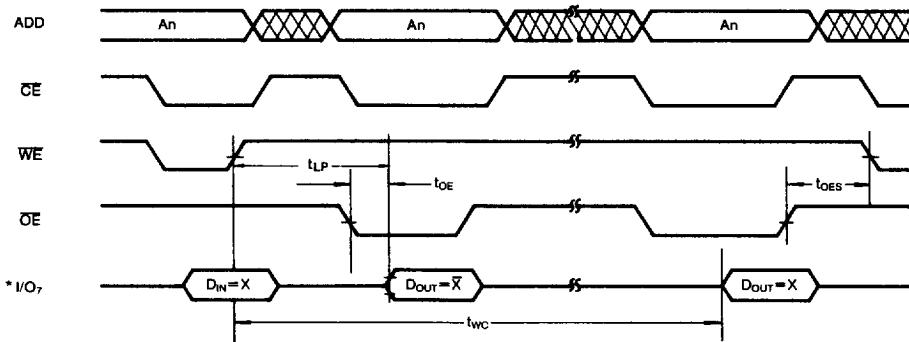
\* NOTE: I/O<sub>7</sub> output  $\overline{DIN}_N$  when the chip is read.  
I/O<sub>6</sub> is toggling between "1" and "0" when the chip is successively read.

**KM28C64A/KM28C65A**

**CMOS EEPROM**

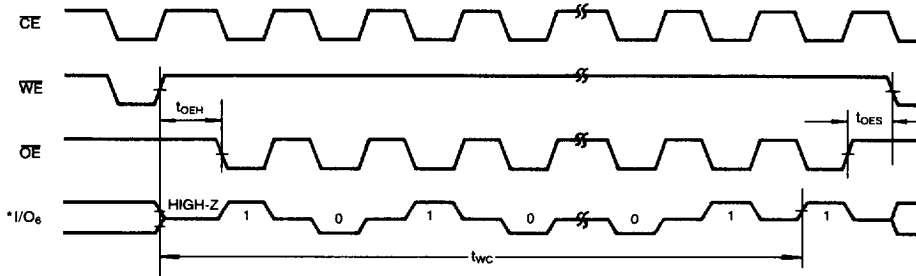
**TIMING DIAGRAMS** (Continued)

**DATA POLLING CYCLE**



\* During the write cycle, I/O<sub>7</sub> will produce an inverted data of the last I/O<sub>7</sub> data, loaded into the EEPROM

**TOGGLE BIT CYCLE**



\* During the write cycle, I/O<sub>6</sub> will toggle between "1" and "0".

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**KM28C64A/KM28C65A****CMOS EEPROM****DEVICE OPERATION****READ**

Reading data from the KM28C64A/65A is similar to reading data from a SRAM. A read cycle occurs when  $\overline{WE}$  is high and  $\overline{CE}$  and  $\overline{OE}$  are low. If either  $\overline{CE}$  or  $\overline{OE}$  goes high the read cycle is terminated. This two line control eliminates bus contention in a system environment. The DATA I/O pins are in the high impedance state whenever  $\overline{OE}$  or  $\overline{CE}$  is high.

**WRITE**

Writing data into the KM28C64A/65A is easy. Only a single 5V supply and TTL level signals are required. The on-chip data latches, address latches, high voltage generator, and fully self-timed control logic make writing as easy as writing to a SRAM.

\*\*\*\* BYTE WRITE MODE \*\*\*\*

The byte write mode of the KM28C64A/65A is only a part of the page write mode. A single byte data loading followed by a  $t_{BLC}$  time-out and by a nonvolatile write cycle will complete a byte mode write.

\*\*\*\* PAGE WRITE MODE \*\*\*\*

The KM28C64A/65A allows up to 64 bytes to be written in a single page write cycle. A page write cycle consists of a data loading period, in which from 1 to 64 bytes of data are loaded into the KM28C64A/65A internal registers and a nonvolatile write period, in which the loaded data in the registers are written to the EEPROM cells of the selected page.

Data is loaded into the KM28C64A/65A by sequentially pulsing  $\overline{WE}$  with  $\overline{CE}$  low and  $\overline{OE}$  high. For each addressed location in the page, address is latched on the falling edge of the  $\overline{WE}$  and data is latched on the rising edge of the  $\overline{WE}$ . The data can be loaded in any "Y" address ( $A_0-A_6$ ) order (i.e. data need not be loaded into consecutive locations in memory in anypage) and can be renewed in a data loading period.

Since the timer for the data loading ( $t_{BLC}$ ) is reset at the falling edge of  $\overline{WE}$  and starts at every rising edge of  $\overline{WE}$ , the only requirement on  $\overline{WE}$  to continue loading the data is that the interval between  $\overline{WE}$  pulses does not exceed the maximum  $t_{BLC}$  (150 $\mu$ s). If  $\overline{OE}$  goes low during the data loading period, further attempt to load the data will be ignored because the external  $\overline{WE}$  signal is blocked by  $\overline{OE}$  signal internally. Consequently, the  $t_{BLC}$  timer is not reset by the external  $\overline{WE}$  pulse if  $\overline{OE}$  is low. The nonvolatile write starts if  $\overline{WE}$  stays high for at least  $t_{BLC}$  maximum (150 $\mu$ s) after the last  $\overline{WE}$  low to high transition. The page address for the nonvolatile write is the "X" ad-

dress (A6-A12) latched on the last  $\overline{WE}$ . The nonvolatile write period consists of an erase cycle and a program cycle. During the erase cycle, the existing data of the locations being addressed are erased. The new data latched at the register are written into the location during the program cycle. Note that only the addressed location in a page are rewritten during a page write cycle.

The KM28C64A/65A also supports  $\overline{CE}$  controlled write cycle. That means  $\overline{CE}$  can be used to latch address and data as well as  $\overline{WE}$ .

**STANDBY**

Power consumption is reduced to less than 100 $\mu$ A by deselecting the device with a high input on  $\overline{CE}$ . Whenever  $\overline{CE}$  is high, the device is in the standby mode and I/O<sub>0</sub>-I/O<sub>7</sub> are in the high impedance state, regardless of the state of  $\overline{OE}$  or  $\overline{WE}$ .

**DATA PROTECTION**

Features have been designed into the KM28C64A/65A to prevent unwanted write cycles during power supply transitions and system noise periods.

The KM28C64A/65A has a protection feature against  $\overline{WE}$  noises; a  $\overline{WE}$  noise the width shorter than 20ns (typ.) will not start any unwanted write cycle. Write cycles are also inhibited when  $V_{CC}$  is less than  $V_{WI}=3.0$  volts, the write inhibits  $V_{CC}$  level. During power-up, the KM28C64A/65A automatically prevents any write operation for a period of 5ms (typ.) after  $V_{CC}$  reaches the  $V_{WI}$  level. This will provide the system with sufficient time to bring  $\overline{WE}$  and  $\overline{CE}$  to a high level before a write can occur. Read cycles can be executed during this initialization period. Holding either  $\overline{OE}$  low or  $\overline{WE}$  high or  $\overline{CE}$  high during power-on and power-off will inhibit inadvertent writes.

\*\*\*\* SOFTWARE DATA PROTECTION \*\*\*\*

The KM28C64A/65A has the JEDEC standard software data protection scheme for enhanced protection of stored data. The scheme does not affect normal write operation if it is not enabled through a SDP enable software algorithm, followed by a write or page write operation. Once the protection mode is enabled, the KM28C64A/65A will not write any data if the SDP enable software algorithm is not proceeded. The data protection function can be disabled by execution a SDP disable software algorithm. Power transitions will not reset the SDP feature. All the data and address timings for the SDP enable and disable are identical to those of a page write cycle.





**KM28C64A/KM28C65A****CMOS EEPROM****DEVICE OPERATION** (Continued)**WRITE COMPLETION INDICATORS****\*\*\* DATA POLLING \*\*\***

The KM28C64A/65A features  $\overline{\text{DATA}}$ -Polling at I/O<sub>7</sub> to detect the completion of a write cycle using a simple read and compare operation. Such a scheme does not require any external hardware. During the write period, any attempt to read of the last byte the EEPROM will produce, at I/O<sub>7</sub>, an inverted value of the last I/O<sub>7</sub> data loaded to the EEPROM. True data will be produced at all I/O's once the write cycle has been completed

**\*\*\* TOGGLE BIT \*\*\***

The KM28C64A/65A also provides toggle bit at I/O<sub>6</sub> to determine the end of a write cycle. During the write cycle, subsequent attempts to read the EEPROM will toggle I/O<sub>6</sub> between "1" and "0". Once the write cycle is complete, the toggling will stop and valid data will be read.

**\*\*\* READY/ $\overline{\text{BUSY}}$  \*\*\***

The KM28C65A has a Ready/ $\overline{\text{BUSY}}$  output on pin 1 that indicates when the write cycle is complete. The pin is

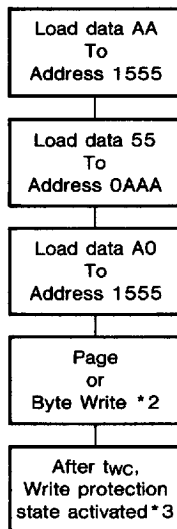
normally high except when a write cycle is in progress, in which case the pin is low. The Ready/ $\overline{\text{BUSY}}$  output is configured as an open-drain driver thereby allowing two or more Ready/ $\overline{\text{BUSY}}$  output to be OR-tied. This pin requires an appropriate pull-up resistor for proper operation. The pull-up resistor value may be calculated as follows.

$$R_P = \frac{V_{CC}(\text{max}) - V_{OL}(\text{max})}{I_{OL} + \sum I_L} = \frac{5.1V}{2.1\text{mA} + \sum I_L}$$

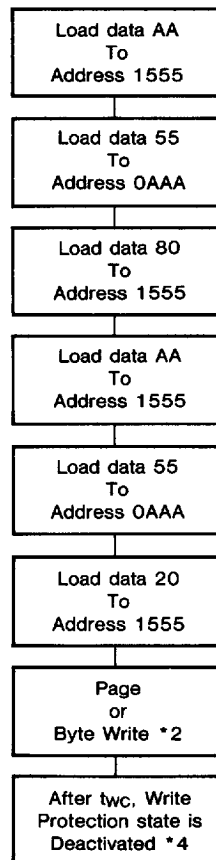
where  $\sum I_L$  is the sum of the input currents of all devices tied to the Ready/ $\overline{\text{BUSY}}$  pin.

**ENDURANCE AND DATA RETENTION**

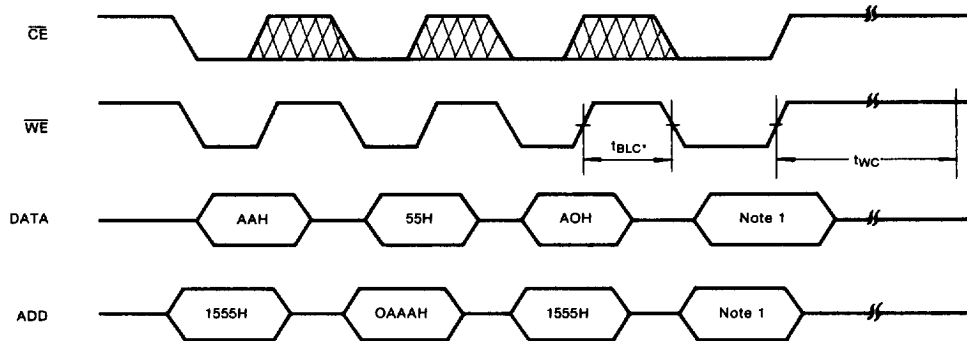
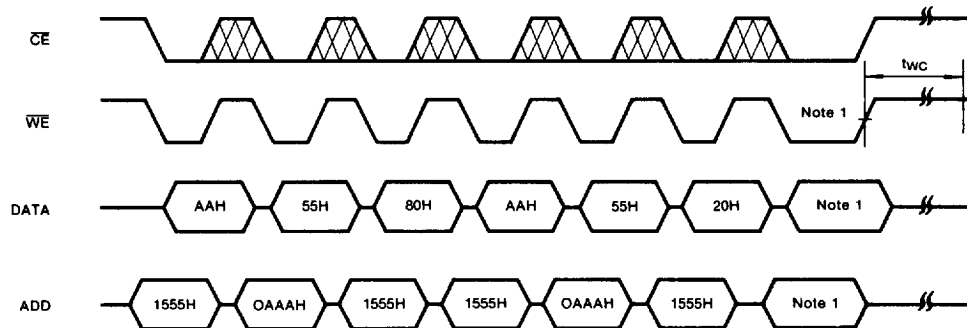
KM28C64A/65A is designed for applications requiring up to 100,000 write cycles per EEPROM byte and ten years of data retention. This means that each byte may be reliably written 100,000 times without degrading device operation. The device also features an on-chip Error Checking and Correction scheme that can detect and correct any single bit failure in a byte, and hence, significant improvements in the endurance and data retention characteristics are achieved.

**KM28C64A/KM28C65A****CMOS EEPROM****SOFTWARE DATA PROTECTION ALGORITHM\*1****SDP Enable Sequence**

\* Write mode enabled

**SDP Disable Sequence**

- Note: 1. Data Format: I/O<sub>7</sub>-I/O<sub>0</sub> (HEX)  
Address Format: A<sub>12</sub>-A<sub>0</sub> (HEX)
2. 1 to 64 byte of data may be loaded in random order.
  3. Write protection state will be activated after t<sub>WC</sub> even if no data is written.
  4. Write protection state will be deactivated after.

**KM28C64A/KM28C65A****CMOS EEPROM****TIMING DIAGRAM OF SOFTWARE DATA PROTECTION****SDP ENABLE TIMING SEQUENCE****SDP DISABLE TIMING SEQUENCE**

\*  $t_{BLC}$  max.

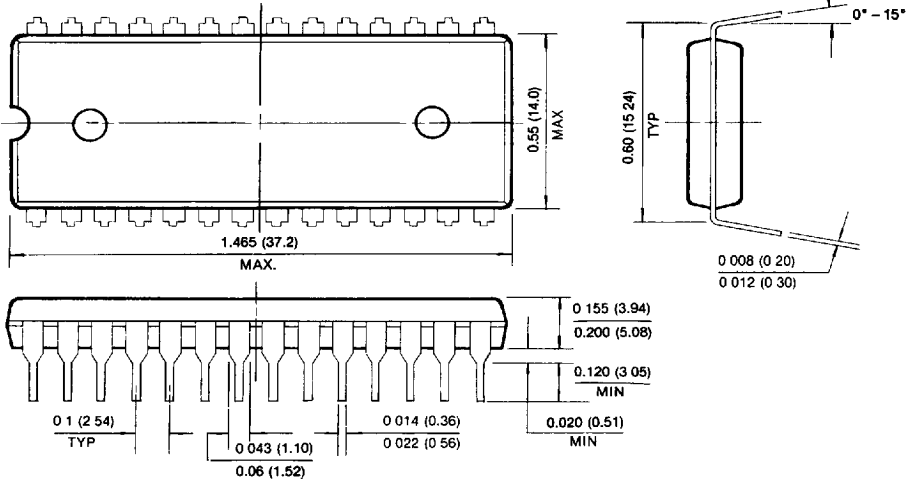
Note 1: 1 to 64 byte of data maybe loaded in random order.

# KM28C64A/KM28C65A

# CMOS EEPROM

## PACKAGE DIMENSIONS (Continued) 28 LEAD PLASTIC DUAL IN LINE PACKAGE

Units: Inches (millimeters)



## 32 PIN PLASTIC LEADED CHIP CARRIER

