National Semiconductor

July 2006

LP3929
High Speed Bi-Directional Level Shifter and Ultra Low-Dropout CMOS Voltage Regulator and Line Protection

General Description

The LP3929 is designed for portable and wireless applications requiring level translation and power supply generation in a compact footprint.

The device level translates 1.8 V LVCMOS on the host (A) side to 2.85 V LVCMOS levels on the card (B) side for a miniSD / SD 4-bit bi-directional data bus.

Independent direct control of the CMD, Data0 and Data1-3 paths support mini SD state machine requirements. A shutdown pin is provided for the level shifters and regulator. The f_CLK_A is a feedback clock to the host which can be used to overcome level shifter bus delay.

The built-in low-dropout voltage regulator is ideal for mobile phone and battery powered wireless applications. It provides up to 200 mA from a 3.05 V to 5.5 V input. It is stable with small 1.0 µF ±30% ceramic and high quality tantalum output capacitors, requiring smallest possible PC board area.

The card (B port) side channels have integration of ASIP (Application Specific Integrated Passives) - on chip integrated pull-up, pull-down, series resistors and capacitors for EMC filtering. It is designed to tolerate IEC61000-4-2 level 4 ESD: ±15 kV air discharge, ±8 kV direct contact.

Key Specifications

Level Shifter:

- 6-signal Level Shifter (5 bi-directional and 1 uni-direction)
- 3 ns (typ) propagation delay
- Channel-to-channel skew < 1 ns (max)

Low-Dropout Regulator:

- 3.05 V to 5.5 V input range
- 2.85 V at 200 mA
- Fast Turn-On time: 30 µs (typ)
- 110 mV (max) dropout with 200 mA load
- Thermal shutdown at 160˚C (typ)

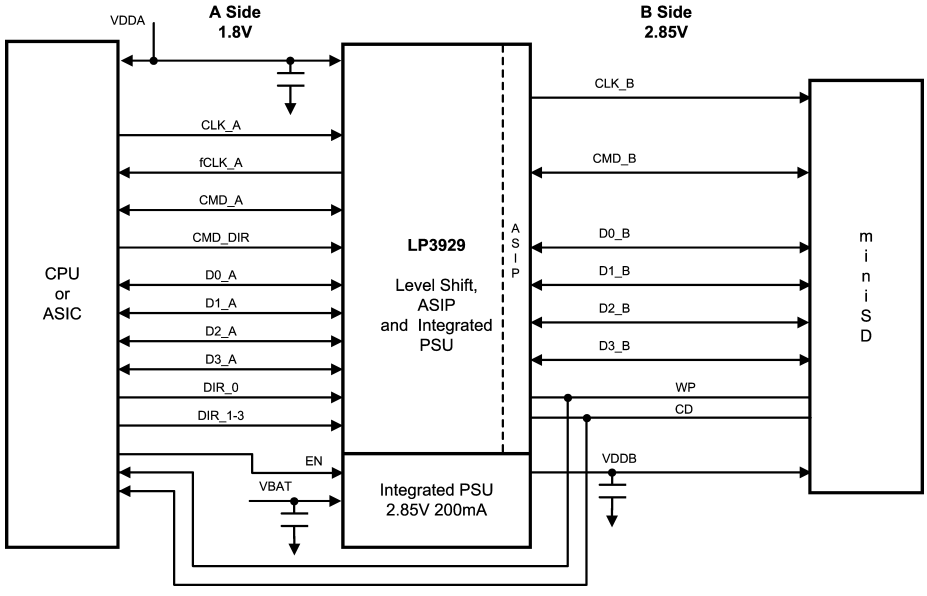
Protection Block (B Side):

- Robust IEC ESD Protection: ±15 kV Air Gap, ±8 kV Direct Contact
- ASIP / EMI Filtering

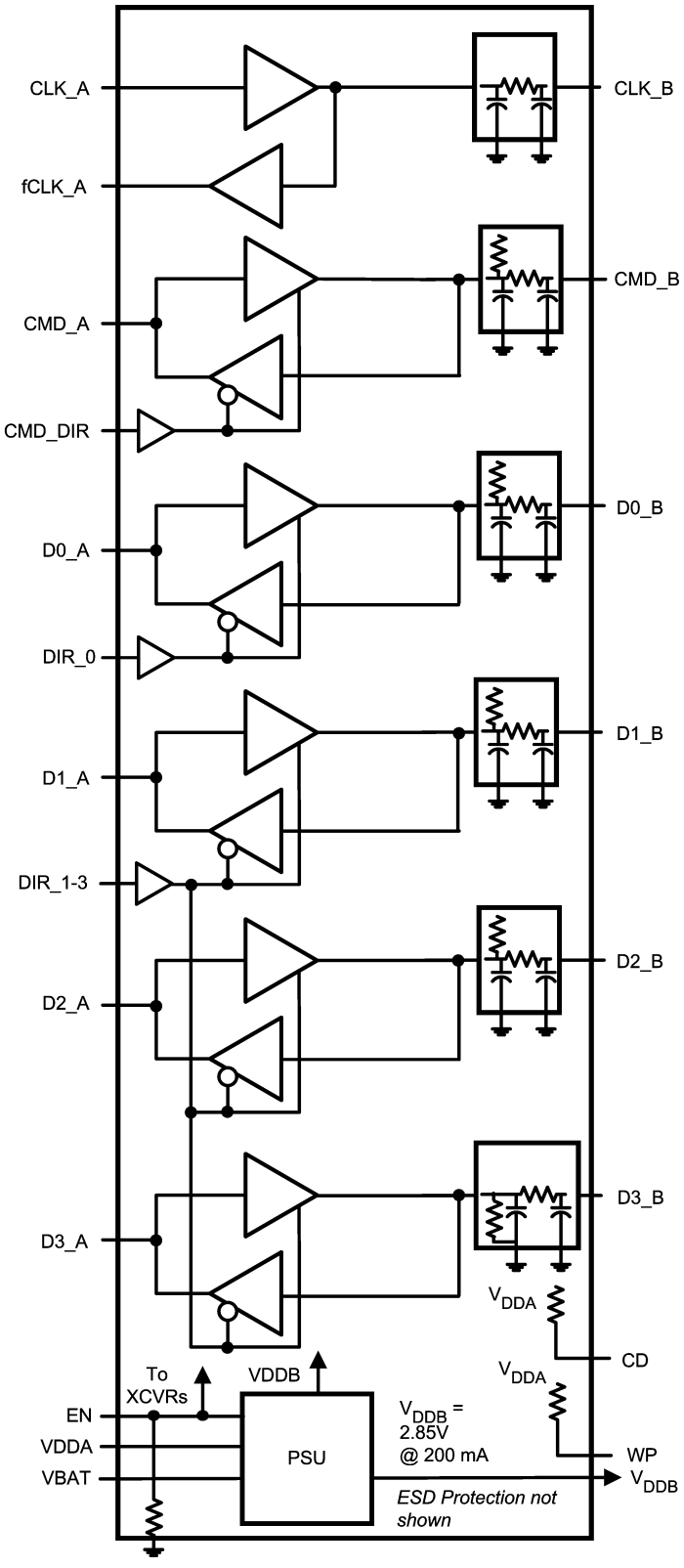
Features

- Ultra small micro SMD 24 bump package
- 6-signal level translation 1.8 V to 2.85 V
- LDO stable with ceramic and high quality tantalum capacitors

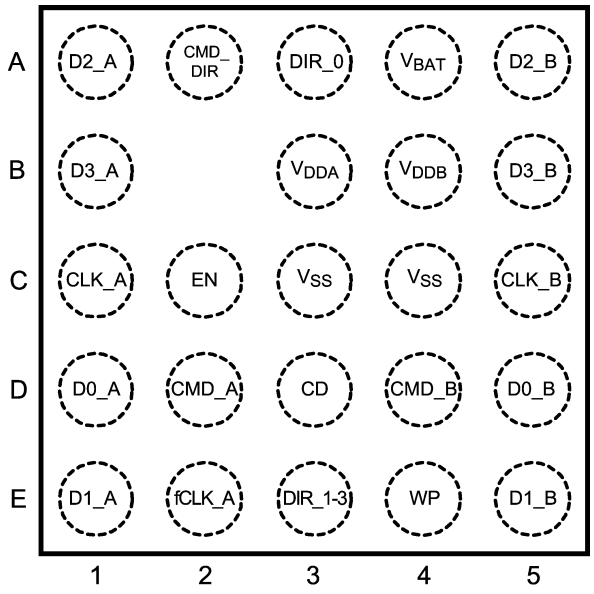
Typical Application Circuit



Block Diagram



Package Outline and Connection Diagrams



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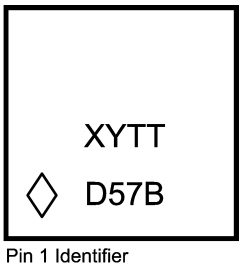
Top View - Bump Underneath
24 Bump micro SMD Package
See NSC Package Number TME24AAA



Pin 1 Identifier

20186812

Note: The actual physical placement of the package marking will vary from part to part. The package marking "XY" will designate the date code. The "TT" is a NSC internal code for die traceability; engineering sample parts will be marked as "ES". Both will vary considerably. The pin 1 marking identifier is the location of corner bump A1.

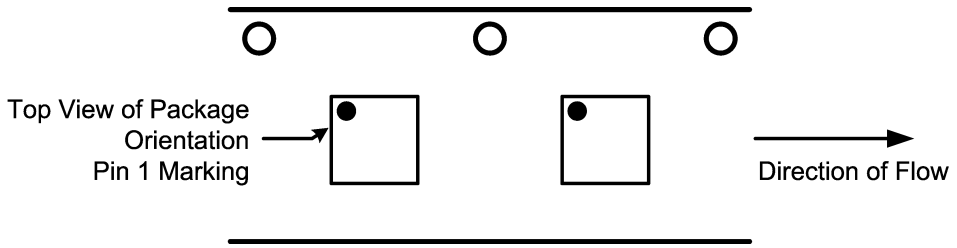
Top View - TME24 Device Marking

Ordering Information

For 24 Bump micro SMD Package

Output Voltage	Grade	LP3929 Supplied As 250 Units, Tape & Reel	LP3929 Supplied As 3000 Units, Tape & Reel
2.85 V	STD	LP3929TME-AACQ	LP3929TMEX-AACQ

Tape and Reel Information



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Top View: Tape and Reel Information

Pin Descriptions

Pin Name	micro SMD Bump Identifier	Port / Direction	Type	Function
D0_A	D1	Host / Bidirectional	Push-Pull	1.8 V I/O Channel (Note 14)
D1_A	E1	Host / Bidirectional	Push-Pull	1.8 V I/O Channel (Note 14)
D2_A	A1	Host / Bidirectional	Push-Pull	1.8 V I/O Channel (Note 14)
D3_A	B1	Host / Bidirectional	Push-Pull	1.8 V I/O Channel (Note 14)
CMD_A	D2	Host / Bidirectional	Push-Pull	1.8 V I/O Channel (Note 14)
CLK_A	C1	Host / Input	High Z	1.8 V Input CLK Channel (Note 14)
fCLK_A	E2	Host / Output	Push-Pull	1.8 V Output CLK Channel
DIR_0	A3	Host / Input	High Z	1.8 V Input Direction Control D0 Channel: V_{DDA} = A → B Direction (Write), V_{SS} = B → A Direction (Read)
DIR_1-3	E3	Host / Input	High Z	1.8 V Input Direction Control D1-D3 Channel: V_{DDA} = A → B Direction (Write), V_{SS} = B → A Direction (Read)
CMD_DIR	A2	Host / Input	High Z	1.8 V Input Direction Control CMD Channel: V_{DDA} = A → B Direction (Write), V_{SS} = B → A Direction (Read)
EN	C2	Host / Input	High Z	Device Enable with high impedance pull-down resistor (200 kΩ): V_{DDA} = Device Active (on), V_{SS} = Device Disabled (off)
D0_B	D5	Card / Bidirectional	Push-Pull	2.85 V I/O Channel with high impedance pull-up to V_{DDB} (70 kΩ)
D1_B	E5	Card / Bidirectional	Push-Pull	2.85 V I/O Channel with high impedance pull-up to V_{DDB} (70 kΩ)
D2_B	A5	Card / Bidirectional	Push-Pull	2.85 V I/O Channel with high impedance pull-up to V_{DDB} (70 kΩ)
D3_B	B5	Card / Bidirectional	Push-Pull	2.85 V I/O Channel with high impedance pull-down to V_{SS} (470 kΩ)
CMD_B	D4	Card / Bidirectional	Push-Pull	2.85 V I/O Channel with high impedance pull-up to V_{DDB} (15 kΩ)
CLK_B	C5	Card / Output	Push-Pull	2.85 V Output CLK Channel
V_{BAT}	A4	Host / Input	Power	3.05 V to 5.5 V
V_{DDA}	B3	Host / Input	Power	1.71 V to 1.92 V, 1.8 V (typ)
V_{DDB}	B4	Card / Output	Power	2.85 V (LDO output)
V_{SS}	C3			Ground
V_{SS}	C4			Ground
WP	E4	Host / Card Input	Pull-up	Pull-up to V_{DDA} (100 kΩ)
CD	D3	Host / Card Input	Pull-up	Pull-up to V_{DDA} (100 kΩ)

Pin Descriptions (Continued)

TABLE 1. Operation Modes

Inputs				Mode
EN	**CMD_DIR**	**DIR_0**	**DIR_1-3**	
L	X	X	X	Level shifter / LDO = off (Shutdown Mode)
H	L	L	L	All channels (D0-D3 and CMD): B → A Direction
H	L	L	H	A → B Direction: D1-D3, B → A Direction: CMD and D0
H	L	H	L	A → B Direction: D0, B → A Direction: CMD and D1-D3
H	L	H	H	A → B Direction: D0-D3, B → A Direction: CMD
H	H	L	L	A → B Direction: CMD, B → A Direction: D0-D3
H	H	L	H	A → B Direction: CMD and D1-D3, B → A Direction: D0
H	H	H	L	A → B Direction: CMD and D0, B → A Direction: D1-D3
H	H	H	H	All channels (D0-D3 and CMD): A → B Direction

H = V_{DDA}, L = V_{SS}

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{BAT})	−0.3V to +6.0V
Supply Voltage (V_{DDA})	−0.3V to +3.3V
LVCMOS A Port Input Voltage	−0.3V to V_{DDA} + 0.3V
LVCMOS A Port I/O Voltage	−0.3V to V_{DDA} + 0.3V
LVCMOS A Port I/O Voltage	−0.3V to V_{DDB} + 0.3V
Junction Temperature	150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature (Note 13)	235˚C
Pad Temperature (Note 13)	235˚C
Derate micro SMD Package above 25˚C	22.9 mW/˚C
Maximum Power Dissipation Capacity at 25˚C micro SMD	2.8 W
ESD Rating	
HBM, 1.5kΩ, 100pF	± 2kV
EIAJ, 0Ω, 200pF	± 200V
IEC61000-4-2, 330Ω, 150pF, Air Gap, B Side (Note 2)	± 15kV
IEC61000-4-2, 330Ω, 150pF, Direct Contact, B Side (Note 2)	± 8kV

Operating Conditions

V_{BAT} to V_{SS}	3.05V to 5.5V
V_{DDA} to V_{SS}	1.71V to 1.92V
Ambient Temperature	−30˚C to +85˚C

Electrical Characteristics

Unless otherwise specified: C_{VBAT} = 1 µF, I_{OUT} = 1 mA, C_{VDDB} = 1 µF, C_{VDDA} = 1 µF. Typical values and limits appearing in standard typeface apply for T_A = 25˚C. Limits appearing in **boldface type** apply over the entire ambient temperature range for operation, −30˚C to +85˚C. (Notes 3, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS A (Host) Port (V_{DDA} = 1.71V to 1.92V)							
V_{IH}	Input Voltage High Level			**0.65xV_{DDA}**		**1.92**	V
			V_{DDA} = 1.71V	**1.1115**		**1.92**	V
			V_{DDA} = 1.92V	**1.248**		**1.92**	V
V_{IL}	Input Voltage Low Level			**0**		**0.30xV_{DDA}**	V
			V_{DDA} = 1.71V	**0**		**0.513**	V
			V_{DDA} = 1.92V	**0**		**0.576**	V
I_{IH}	Input Current High Level	V_{IH} = V_{DDA}		**−1**	0	**+1**	µA
			EN = V_{SS}	**−1**	0	**+1**	µA
			EN = V_{DDA}	**−1**	0	**+10**	µA
I_{IL}	Input Current Low Level	V_{IL} = V_{SS}		**−1**	0	**+1**	µA
V_{OH}	Output Voltage High Level	I_{OH} = −4 mA		**1.26**	1.8	**V_{DDA}**	V
V_{OL}	Output Voltage Low Level	I_{OL} = 4 mA		**V_{SS}**	0	**0.45**	V
LVCMOS B (Card) Port (V_{DDB} = 2.85V)							
V_{IH}	Input Voltage High Level			**0.65xV_{DDB}**		**V_{DDB}**	V
V_{IL}	Input Voltage Low Level			**0**		**0.35xV_{DDB}**	V
I_{IH}	Input Current High Level	V_{IH} = V_{DDB}	D0_B to D2_B	**− 2**	0.2	**+ 2**	µA
			D3_B	**0**	6.5	**+ 13**	µA
			CMD_B	**− 5**	0.3	**+ 5**	µA
I_{IL}	Input Current Low Level	V_{IL} = V_{SS}	D0_B to D2_B	**− 80**	−40	**0**	µA
			D3_B	**− 1**	0.1	**+ 1**	µA
			CMD_B	**− 300**	− 200	**− 20**	µA
IOS +	Short Circuit Current	V_{OUTlow} = V_{DDB}			45		µA
IOS −		$V_{OUThigh}$ = V_{SS}			− 20		µA
V_{OH}	Output Voltage High Level	I_{OH} = − 2 mA		**0.75xV_{DDB}**			V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA				**0.25xV_{DDB}**	V

Electrical Characteristics

Unless otherwise specified: C_{VBAT} = 1 µF, I_{OUT} = 1 mA, C_{VDDB} = 1 µF, C_{VDDA} = 1 µF. Typical values and limits appearing in standard typeface apply for T_A = 25˚C. Limits appearing in **boldface type** apply over the entire ambient temperature range for operation, –30˚C to +85˚C. (Notes 3, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Supply Current							
I_{DD}	Supply Current	All Channels Static: A → B mode, LDO unloaded	V_{BAT}		4	**7**	mA
			V_{DDA}		95	**200**	µA
I_{DDZ}	Supply Current — Shutdown	EN = V_{SS}	V_{BAT}		0.1	**2**	µA
			V_{DDA}		0.2	**2**	µA
C_{OUT}	Output Capacitance (Note 15)	B (card) port			15	**20**	pF

Level Shifter AC Switching Characteristics

Unless otherwise specified: C_{VBAT} = 1 µF, I_{OUT} = 1 mA, C_{VDDB} = 1 µF, C_{VDDA} = 1 µF. Typical values and limits appearing in standard typeface apply for T_A = 25˚C. Limits appearing in **boldface type** apply over the entire ambient temperature range for operation, –30˚C to +85˚C. (Notes 3, 5, 15, 16)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay A to B or B to A	C_{LB} = 15 pF, C_{LA} = 20 pF, 50%-50%		3	**7**	ns
	Propagation Delay CLK_A to fCLK_A	C_{LA} = 20 pF, 50%-50%		5	**14**	ns
t_{PHL}	Propagation Delay A to B or B to A	C_{LB} = 15 pF, C_{LA} = 20 pF, 50%-50%		3	**7**	ns
	Propagation Delay CLK_A to fCLK_A	C_{LA} = 20 pF, 50%-50%		5	**14**	ns
t_{RISE}	Rise Time A Side Output *Figure 2*	C_{LA} = 20 pF, 20%-70%		1.1	**3**	ns
	Rise Time B Side Output with ASIP *Figure 2*	C_{LB} = 15 pF, 20%-70%		1.6	**3**	ns
t_{FALL}	Fall Time A Side Output *Figure 2*	C_{LA} = 20 pF, 20%-70%		1.0	**3**	ns
	Fall Time B Side Output with ASIP *Figure 2*	C_{LB} = 15 pF, 20%-70%		1.9	**3**	ns
t_{SKEW}	Skew between D0–D3, CLK and CMD outputs (either edge)			<0.5	**1.0**	ns
t_{EN}	Enable Time			30	**200**	µs
t_{DIS}	Disable Time			18	**50**	ns
t_{TA}	Level-Shifter Direction Switch Response (Turn Around) Time			13	**20**	ns

LDO Electrical Characteristics

Unless otherwise specified: C_{VBAT} = 1 µF, I_{OUT} = 1 mA, C_{VDDB} = 1 µF, C_{VDDA} = 1 µF. Typical values and limits appearing in standard typeface apply for T_A = 25˚C. Limits appearing in **boldface type** apply over the entire ambient temperature range for operation, –30˚C to +85˚C. (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OUT}	Output Voltage, V_{OUT} = V_{DDB}	I_{OUT} = 200mA, V_{BAT} = 3.05V to 5.5V	**2.76**	2.85	**2.93**	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1 mA	–2 **–3**		2 **3**	% of $V_{OUT(nom)}$
	Line Regulation Error (Note 6)	V_{BAT} = ($V_{OUT(nom)}$ + 0.5V) to 5.5V, I_{OUT} = 1 mA	**–0.15**		**0.15**	%/V
	Load Regulation Error (Note 7)	I_{OUT} = 1 mA to 200 mA	**–0.01**		**0.01**	%/mA
	Output AC Line Regulation	V_{BAT} = $V_{OUT(nom)}$ + 1V, I_{OUT} = 100 mA, C_{OUT} = 1.0 µF		1.5		mV_{PP}
PSRR	Power Supply Rejection Ratio (Note 15)	V_{BAT} = $V_{OUT(nom)}$ + 1V, f = 1 kHz, I_{OUT} = 50 mA		40		dB
		V_{BAT} = $V_{OUT(nom)}$ + 1V, f = 10 kHz, I_{OUT} = 50 mA		30		
ΔV_{DO}	Dropout Voltage (Note 8)	I_{OUT} = 1 mA		1		mV
		I_{OUT} = 50 mA		20		
		I_{OUT} = 100 mA		35		
		I_{OUT} = 200 mA		60	**110**	
I_{SC}	Short Circuit Current Limit	V_{BAT} = 5.5V, Output Grounded (Steady State)		750		mA
T_{ON}	Turn-On Time (Notes 9, 15)			30	**200**	µs
ρn (1/f)	Output Noise Density	f = 1 kHz, C_{OUT} = 1.0 µF		0.6		µV/√Hz
e_n	Output Noise Voltage	BW = 10 Hz to 100 kHz, C_{OUT} = 1.0 µF		45		µVrms
Output Capacitor	Output Filter Capacitance (Note 10)	V_{BAT} = 3.05V to 5.5V, I_{OUT} = 1mA to 200 mA	**0.7**	1.0	**22**	µF
	Output Filter Capacitance ESR (Note 11)	V_{BAT} = 3.05V to 5.5V, I_{OUT} = 1mA to 200mA	**5**		**500**	mΩ
Thermal Shutdown	Thermal Shutdown Temperature (Notes 12, 15)	V_{BAT} = 3.05V to 5.5V, I_{OUT} = 1mA to 200mA		160		˚C
	Thermal Shutdown Hysteresis (Note 15)			20		˚C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: IEC61000-4-2 level 4 ESD tolerance applies to VDDB, D0_B–D3_B, CMD_B, CLK_B, WP and CP pins only. Device is tested in application (common ground, bypass capacitors of 1.0 µF present on V_{BAT}, V_{DDA} and V_{DDB}).

Note 3: Typical values are given for V_{DDA} = 1.8V, V_{BAT} = 3.6V, T_A = 25˚C

Note 4: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are reference to ground unless otherwise specified.

Note 5: Input signal for test purpose is defined as: A side – 0V to 1.8V with 2ns rise time (20%-70%) and B side – 0V to 2.85V with 2ns rise time (20%-70%)

Note 6: The output voltage changes slightly with line voltage. An increase in the line voltage results in a slight increase in the output voltage and vice versa.

Note 7: The output voltage changes slightly with load current. An increase in the load current results in a slight decrease in the output voltage and vice versa.

Note 8: Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for input voltages below 2.7V.

Note 9: Turn-on time is that between when the enable input is high an the output voltage just reaching 95% of its nominal value.

Note 10: Range of capacitor value for which the device will remain stable. This electrical specification is guaranteed by design.

Note 11: Range of capacitor ESR values for which the device will remain stable. This electrical specification is guaranteed by design.

Note 12: The built-in thermal shut-down of the LDO is also used to put all A and B outputs in tri-state mode.

Note 13: Additional information on lead temperature and pad temperature can be found in National Semiconductor Application Note (AN-1112).

Note 14: Unused inputs must be terminated.

Note 15: This electrical specification is guaranteed by design.

Note 16: The SD/MMC card specification calls for a total of 30 pF capacitance. A load of 15 pF is internal to the LP3929, so the external load capacitance on the B side should comprise the remaining (15 pF or less).

Timing Diagrams

Timing Diagrams (Continued)

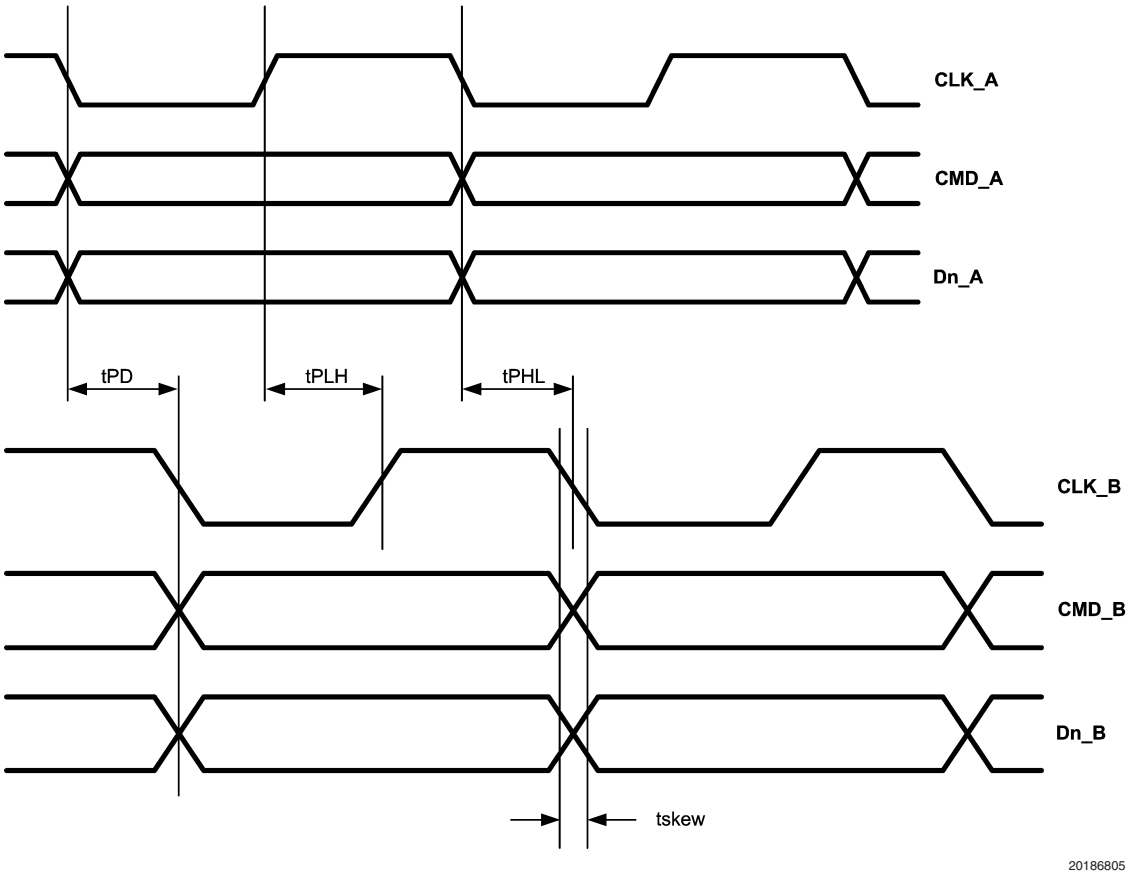


FIGURE 1. A to B Timing Diagram (propagation delay, skew)

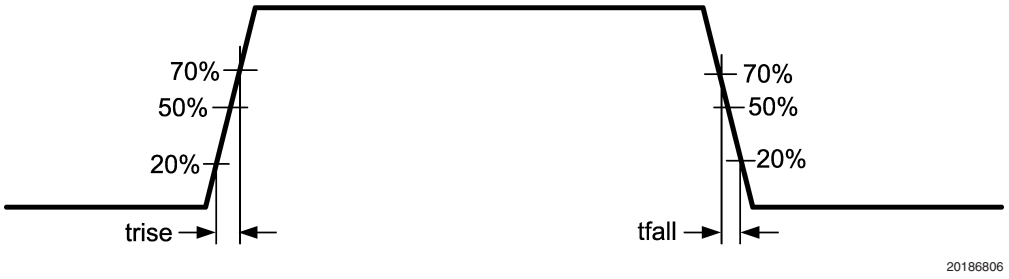


FIGURE 2. Output Transition Time (A and B Side)

Timing Diagrams (Continued)

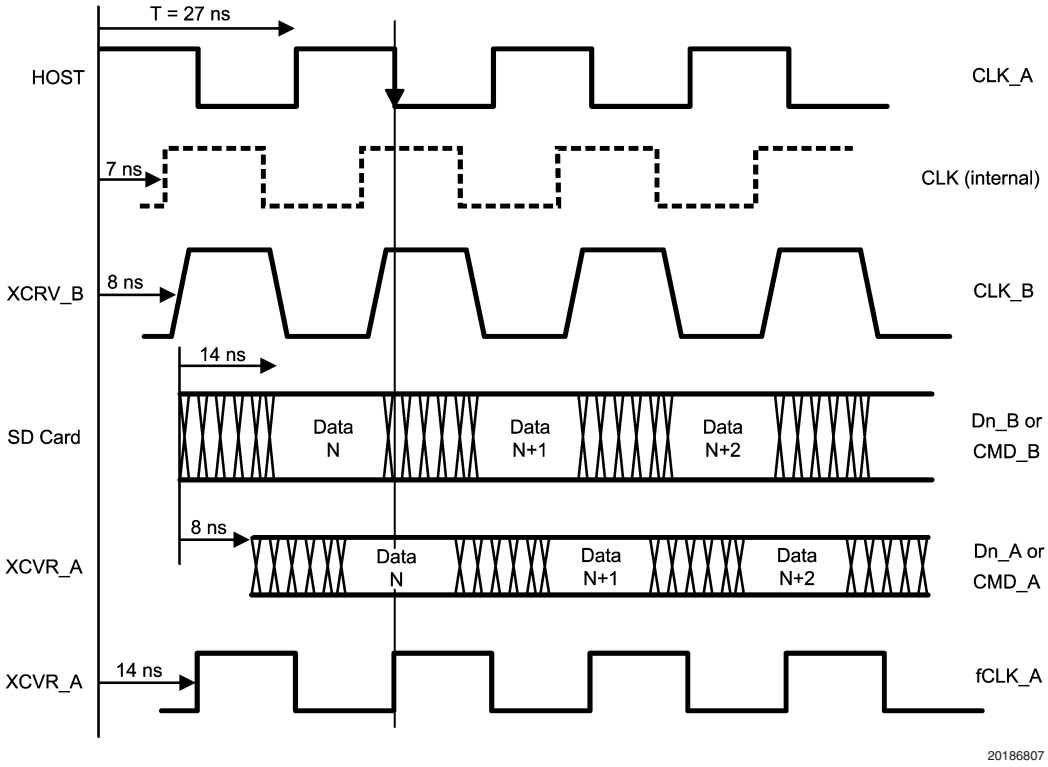
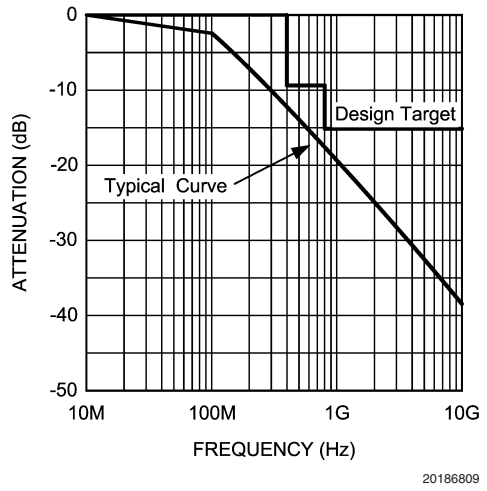


FIGURE 3. B to A Direction (37 MHz Example)

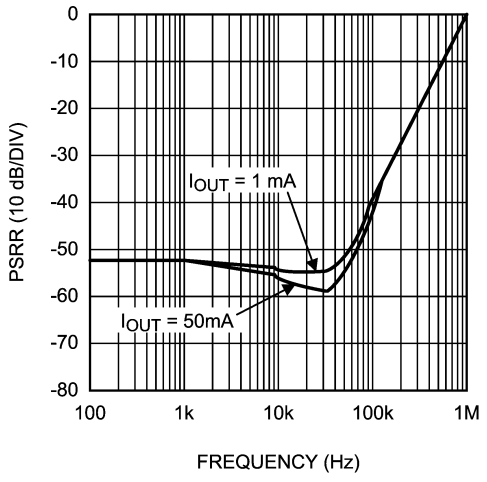
Typical Performance Characteristics

Unless otherwise specified: C_{VBAT} = 1 µF, C_{VDDA} = 1 µF, C_{VDDB} = 1 µF, V_{BAT} = 3.85 V, V_{DDA} = 1.8 V, T_A = 25˚C.

ASIP / EMI Filter Response



Power Supply Rejection Ration (V_{BAT} = 3.85V)



Application Information

EXTERNAL CAPACITORS

Like any low-dropout regulator, the LP3929 requires external capacitors for regulator stability. The LP3929 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitance of 1 µF is required between the LP3929 V_{BAT} pin and ground (the amount of the capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the V_{BAT} pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance, bias voltage and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be 1 µF over the entire operating conditions.

FAST ON-TIME

The LP3929 utilizes a speed up circuitry to ramp up the internal V_{REF} voltage to its final value to achieve a fast output turn on time.

CAPACITOR CHARACTERISTICS

The LP3929 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 1 µF to 4.7 µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability by the LP3929.

The ceramic capacitor's capacitance can vary with temperature.

Most large value ceramic capacitors (2.2 µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25˚C to 85˚C.

A better choice for temperature coefficient in ceramic capacitor is X7R, which holds the capacitance within ±15%.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25˚C down to –40˚C, so some guard band must be allowed.

OUTPUT CAPACITOR

The LP3929 is designed specifically to work with very small ceramic output capacitors, any ceramic capacitor (dielectric types Z5U, Y5V or X7R) in 1.0 µF to 2.2 µF range with 5 mΩ to 500 mΩ ESR range is suitable in the LP3929 application circuit.

It may also be possible to use tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see section Capacitor Characteristics).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR (Equivalent Series Resistance) value which is within a stable range.

The output capacitor should be placed as near as possible to the V_{DDB} pin.

NO-LOAD STABILITY

The LDO of the LP3929 will remain stable and in regulation with no external load connected to the LDO output V_{DDB}. This is especially important in CMOS RAM keep-alive applications.

MICRO SMD ASSEMBLY

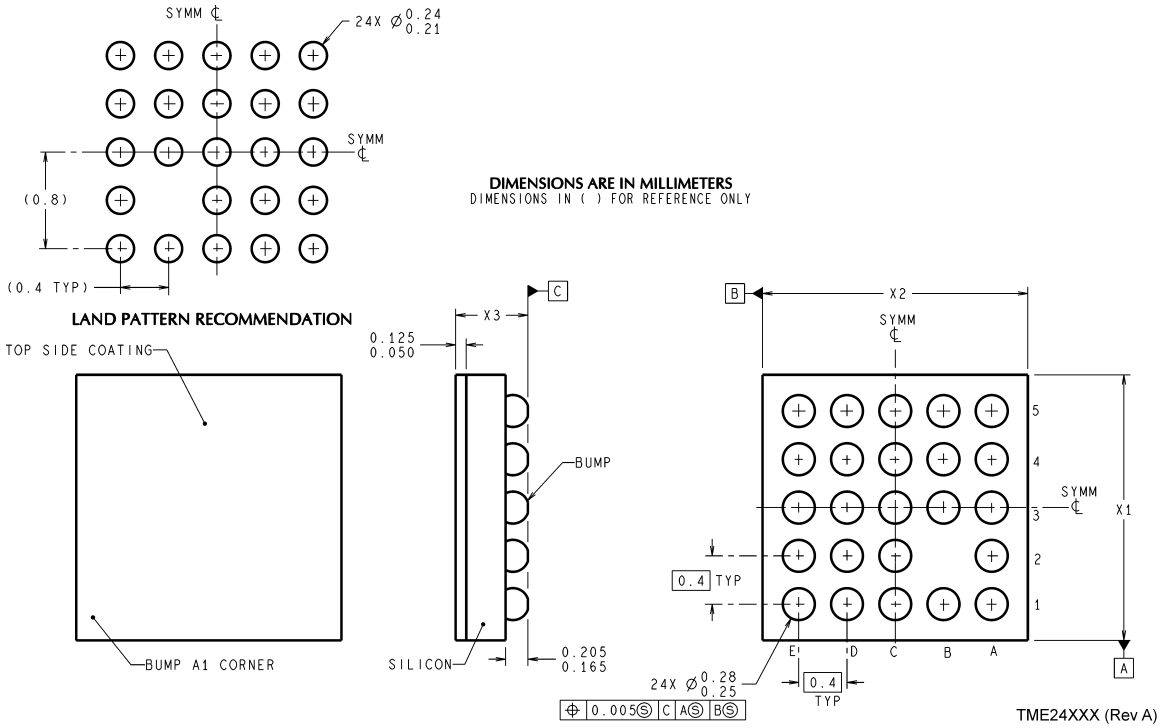
For assembly recommendations of micro SMD package please refer to National Semiconductor Application Note AN-1112.

MICRO SMD LIGHT SENSITIVITY

Exposing the micro SMD device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can effect electrical performance if brought near to the device.

The wavelengths which have most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance.

Physical Dimensions inches (millimeters) unless otherwise noted



micro SMD, 24 Bump
NS Package Number: TME24AAA
The dimensions for X1, X2 and X3 are as follows:
X1 = 2.015mm ± 30µm
X2 = 2.015mm ± 30µm
X3 = 0.600mm ± 75µm

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