Low Power 8th Order Pin Selectable Elliptic or Linear Phase Lowpass Filter

FEATURES

- 8th Order Pin Selectable Elliptic or Bessel Filter in a 14-Pin Package
- 4mA Supply Current with ±5V Supplies
- 64dB Attenuation at 1.44 f_{CUTOFF} (Elliptic Response)
- f_{CUTOFF} up to 30kHz (50:1 f_{CLK} to f_{CUTOFF} Ratio)
- 110µV_{RMS} Wideband Noise with ±5V Supplies
- Operates at Single 5V Supply with 1V_{RMS} Input Range
- Operates up to ±8V Supplies
- TTL/CMOS Compatible Clock Input
- No External Components

APPLICATIONS

- Anti-Aliasing Filters
- Battery-Operated Instruments
- Telecommunication Filters

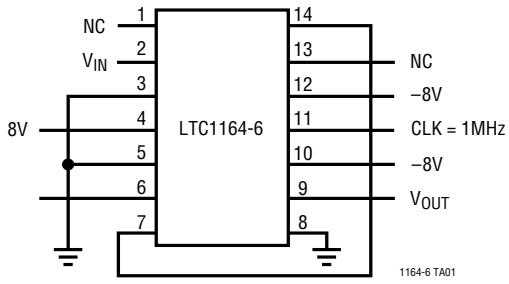
DESCRIPTION

The LTC1164-6 is a monolithic 8th order elliptic lowpass filter featuring clock-tunable cutoff frequency and low power supply current. Low power operation is achieved without compromising noise or distortion performance. At ±5V supplies the LTC1164-6 uses only 4mA supply current while keeping wideband noise below 110µV_{RMS}. With a single 5V supply, the LTC1164-6 can provide up to 10kHz cutoff frequency and 80dB signal-to-noise ratio while consuming only 2.5mA.

The LTC1164-6 provides an elliptic lowpass rolloff with stopband attenuation of 64dB at 1.44 f_{CUTOFF} and an f_{CLK}-to-f_{CUTOFF} ratio of 100:1 (pin 10 to V^-). For a ratio of 100:1, f_{CUTOFF} can be clock-tuned up to 10kHz. For a f_{CLK}-to-f_{CUTOFF} ratio of 50:1 (pin 10 to V^+), the LTC1164-6 provides an elliptic lowpass filter with f_{CUTOFF} frequencies up to 20kHz. When pin 10 is connected to ground, the LTC1164-6 approximates an 8th order linear phase response with 65dB attenuation at 4.5 f_{-3dB} and f_{CLK}/f_{-3dB} ratio of 160:1. The LTC1164-6 is pin compatible with the LTC1064-1.

TYPICAL APPLICATION

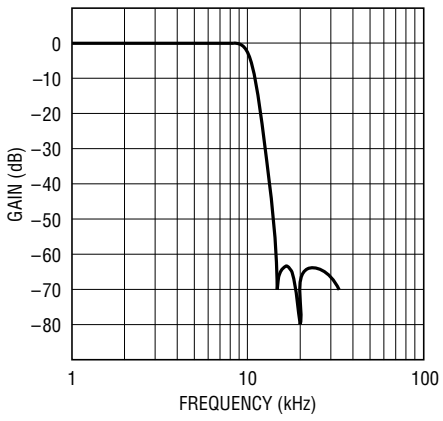
10kHz Anti-Aliasing Elliptic Filter



WIDEBAND NOISE = 115µV_{RMS}

NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

Frequency Response

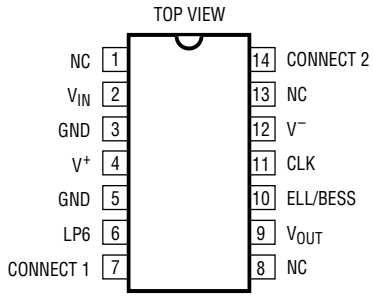


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V

Operating Temperature Range
LTC1164-6C ..... –40°C to 85°C
LTC1164-6M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



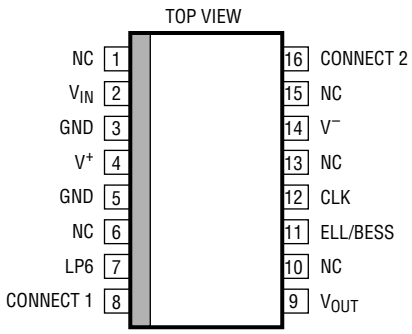
J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER

LTC1164-6CN
LTC1164-6CJ
LTC1164-6MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1164-6CS

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CLK} = 400kHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1μs) and all gain measurements are referenced to passband gain, unless otherwise specified. (f_{CLK}/f_{CUTOFF}) = 4kHz at 100:1 and 8kHz at 50:1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain 0.1Hz to 0.25 f_{CUTOFF} (Note 4)	f_{IN} = 1kHz, (f_{CLK}/f_C) = 100:1	●	–0.50	–0.15	0.25	dB
Passband Ripple with V_S = Single 5V	1Hz to 0.8 f_C (Table 2)			0.1 to –0.3		dB
Gain at 0.50 f_{CUTOFF} (Note 3)	f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1	●	–0.45	–0.10	0.10	dB
Gain at 0.90 f_{CUTOFF} (Note 3)	f_{IN} = 3.6kHz, (f_{CLK}/f_C) = 100:1	●	–0.75	–0.30	0.10	dB
Gain at 0.95 f_{CUTOFF} (Note 3)	f_{IN} = 3.8kHz, (f_{CLK}/f_C) = 100:1	●	–1.40	–0.70	–0.40	dB
Gain at f_{CUTOFF} (Note 3)	f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1	●	–3.50	–2.70	–2.30	dB
	f_{IN} = 8kHz, (f_{CLK}/f_C) = 50:1	●	–3.00	–2.10	–1.50	dB
Gain at 1.44 f_{CUTOFF} (Note 3)	f_{IN} = 5.76kHz, (f_{CLK}/f_C) = 100:1	●	–69	–64	–58	dB
Gain at 2.0 f_{CUTOFF} (Note 3)	f_{IN} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–69	–64	–58	dB
Gain with f_{CLK} = 20kHz	f_{IN} = 200Hz, (f_{CLK}/f_C) = 100:1		–3.50	–2.70	–2.30	dB
Gain with V_S = ±2.375V	f_{IN} = 400kHz, f_{IN} = 2kHz, (f_{CLK}/f_C) = 100:1		–0.50	–0.10	0.30	dB
	f_{IN} = 400kHz, f_{IN} = 4kHz, (f_{CLK}/f_C) = 100:1		–3.30	–2.50	–2.00	dB
Input Frequency Range (Tables 3, 4)	(f_{CLK}/f_C) = 100:1			0 – <f_{CLK}/2		kHz
	(f_{CLK}/f_C) = 50:1			0 – <f_{CLK}		kHz
Maximum f_{CLK} (Table 3)	V_S ≥ ±7.5V			1.5		MHz
	V_S ≤ ±5V			1.0		MHz
	V_S = Single 5V, AGND = 2V			1.0		MHz

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CLK} = 400kHz, TTL or CMOS level (maximum clock rise or fall time ≤ 1μs) and all gain measurements are referenced to passband gain, unless otherwise specified. (f_{CLK}/f_{CUTOFF}) = 4kHz at 100:1 and 8kHz at 50:1.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Feedthrough	Input at GND, f = f_{CLK}, Square Wave					
	V_S = ±7.5V, (f_{CLK}/f_C) = 100:1			500		μV_{RMS}
	V_S = ±5V, (f_{CLK}/f_C) = 50:1			200		μV_{RMS}
Wideband Noise	Input at GND, 1Hz ≤ f < f_{CLK}					
	V_S = ±7.5V			115 ± 5%		μV_{RMS}
	V_S = ±2.5V			100 ± 5%		μV_{RMS}
Input Impedance			30	40	70	kΩ
Output DC Voltage Swing	V_S = ±2.375V	●	±1.25	±1.50		V
	V_S = ±5V	●	±3.70	±4.10		V
	V_S = ±7.5V	●	±5.40	±5.90		V
Output DC Offset	V_S = ±5V, (f_{CLK}/f_C) = 100:1			±100	±160	mV
Output DC Offset TempCo	V_S = ±5V, (f_{CLK}/f_C) = 100:1			±100		μV/°C
Power Supply Current	V_S = ±2.375V, T_A > 25°C			2.5	4.0	mA
		●			4.5	mA
	V_S = ±5V, T_A > 25°C			4.5	7.0	mA
		●			8.0	mA
	V_S = ±7.5V, T_A > 25°C			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

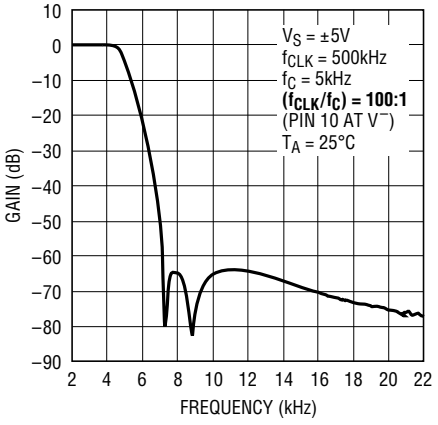
Note 2: Connecting any pin to voltages greater than V^+ or less than V^- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-6.

Note 3: All gains are measured relative to passband gain.

Note 4: The cutoff frequency of the filter is abbreviated as f_{CUTOFF} or f_C.

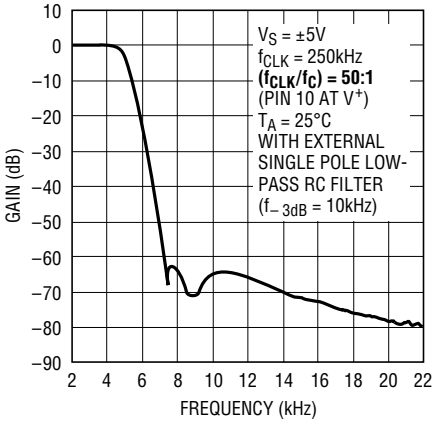
TYPICAL PERFORMANCE CHARACTERISTICS

Stopband Gain vs Frequency (Elliptic Response)



1164-6 G01

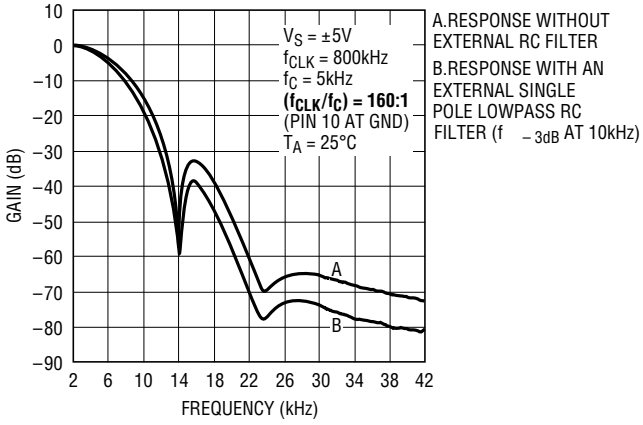
Stopband Gain vs Frequency (Elliptic Response)



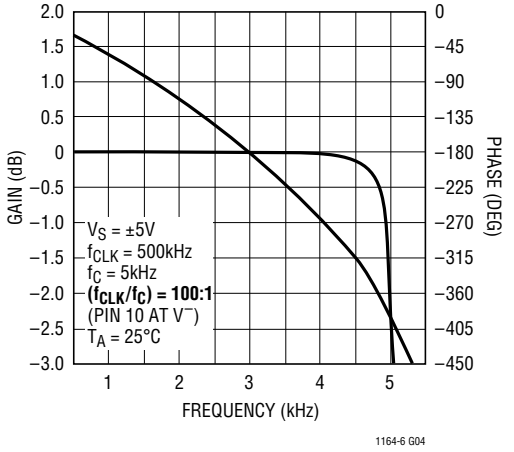
1164-6 G02

TYPICAL PERFORMANCE CHARACTERISTICS

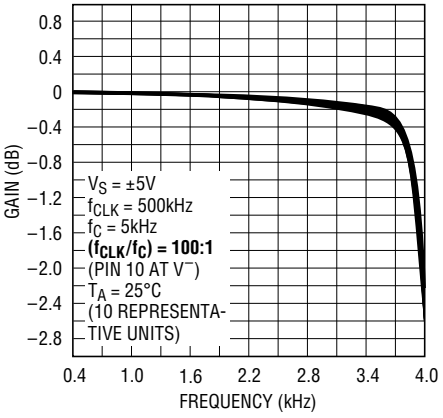
Stopband Gain vs Frequency (Linear Phase Response)



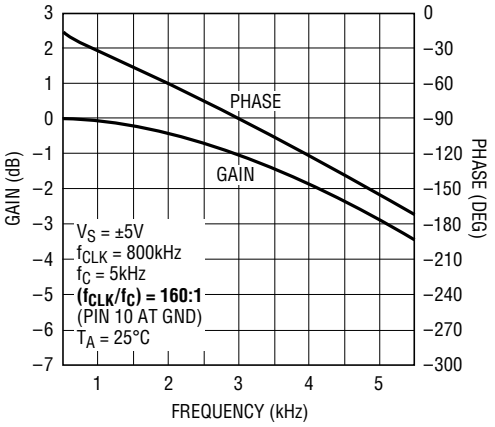
Passband Gain and Phase vs Frequency



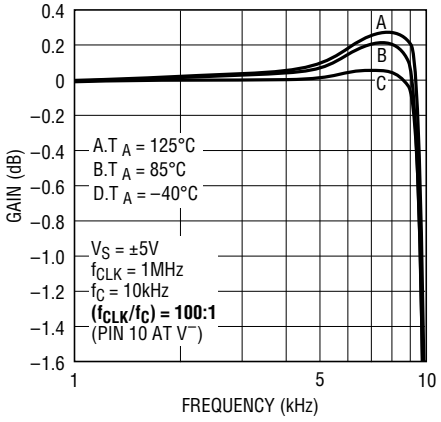
Passband Gain vs Frequency



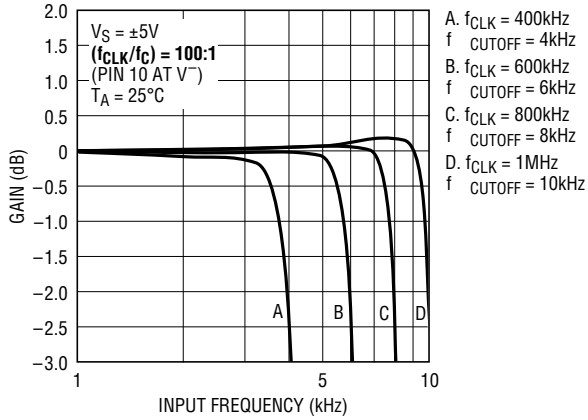
Passband Gain and Phase vs Frequency (Linear Phase Response)



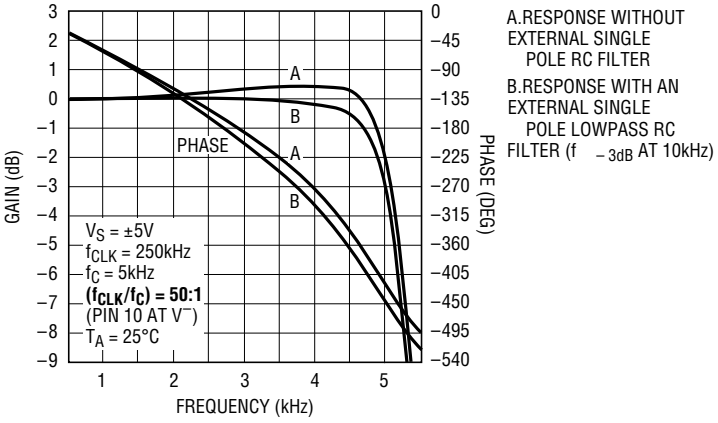
Maximum Passband over Temperature



Passband vs Frequency and f_{CLK}

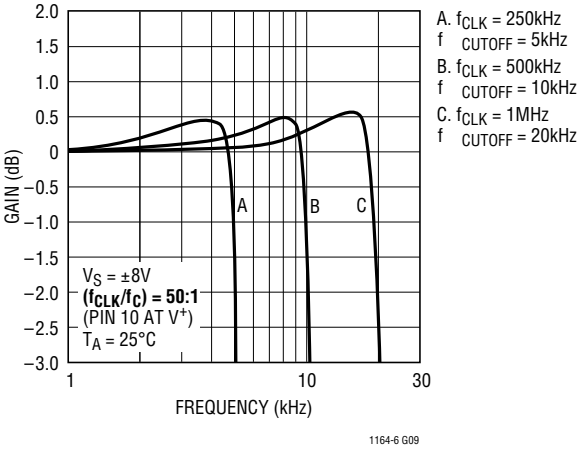


Passband Gain and Phase vs Frequency and f_{CLK}



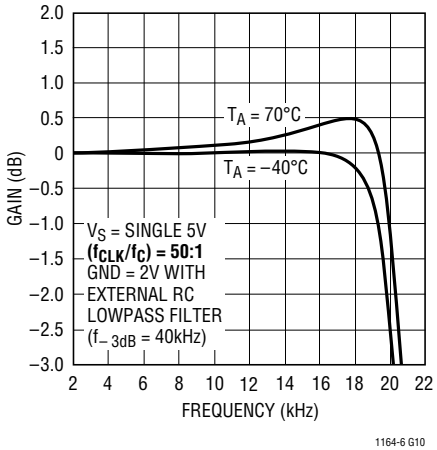
TYPICAL PERFORMANCE CHARACTERISTICS

Passband vs Frequency and f_{CLK}



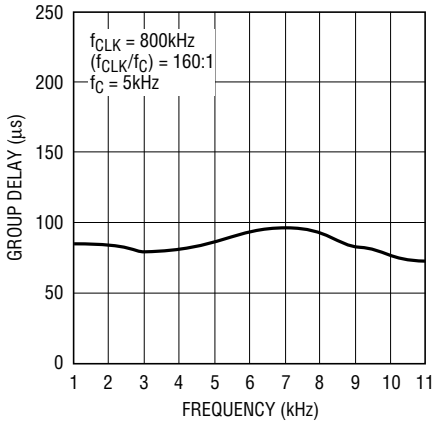
1164-6 G09

Maximum Passband over Temperature



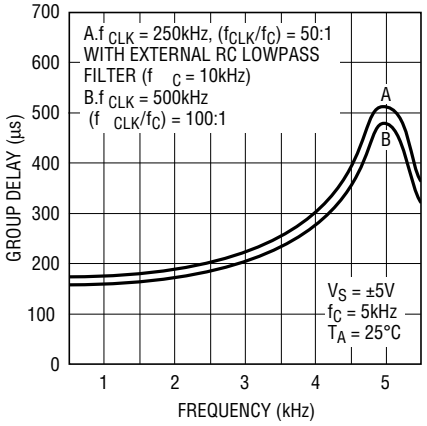
1164-6 G10

Group Delay vs Frequency (Linear Phase Response)



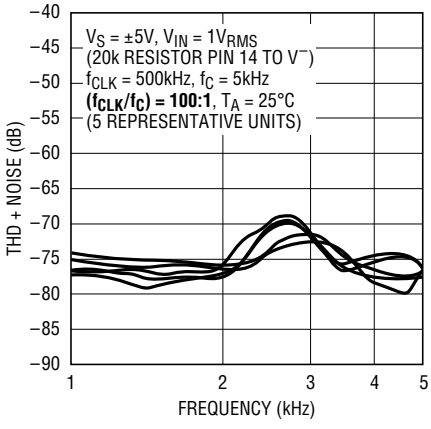
1164-6 G22

Group Delay vs Frequency (Elliptic Response)



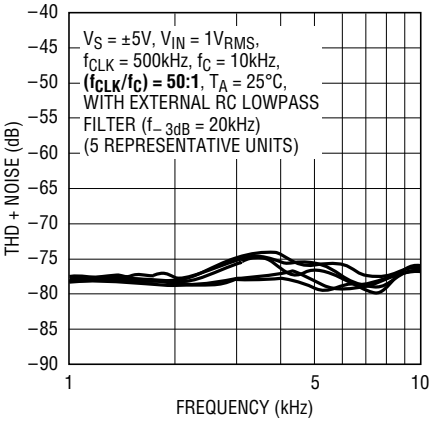
1164-6 G12

THD + Noise vs Frequency (Elliptic Response)



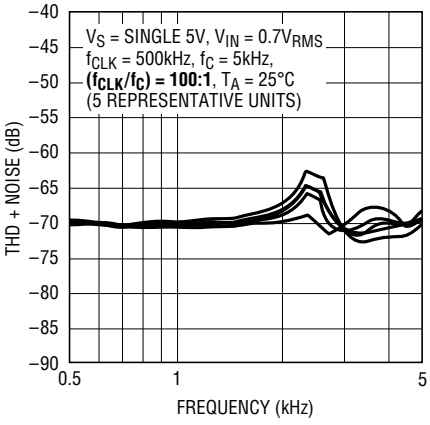
1164-6 G13

THD + Noise vs Frequency (Elliptic Response)



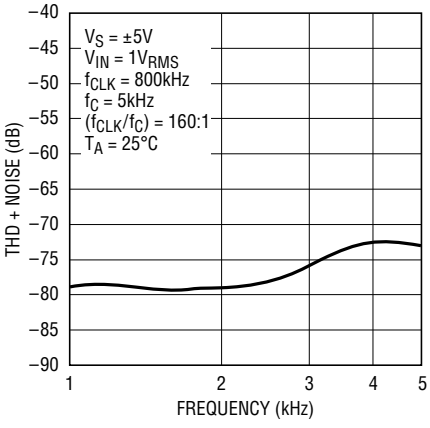
1164-6 G14

THD + Noise vs Frequency (Elliptic Response)



1164-6 G16

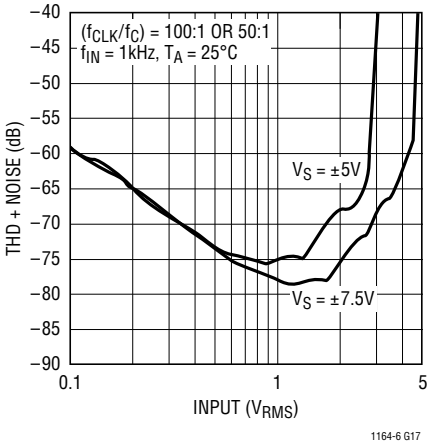
THD + Noise vs Frequency (Linear Phase Response)



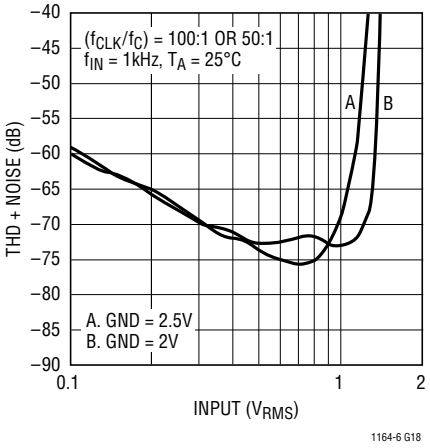
1164-6 G23

TYPICAL PERFORMANCE CHARACTERISTICS

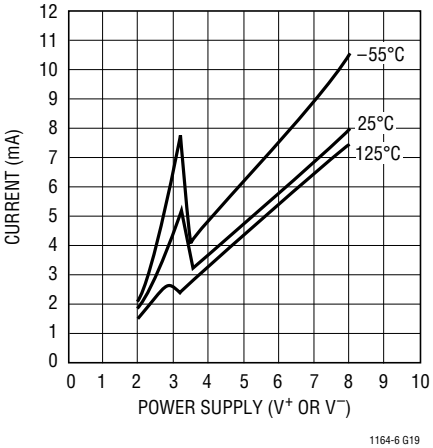
THD + Noise vs RMS Input (Elliptic Response)



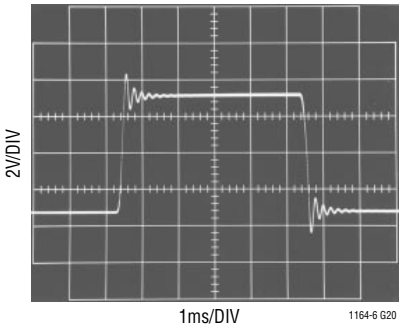
THD + Noise vs RMS Input for Single 5V (Elliptic Response)



Power Supply Current vs Power Supply Voltage

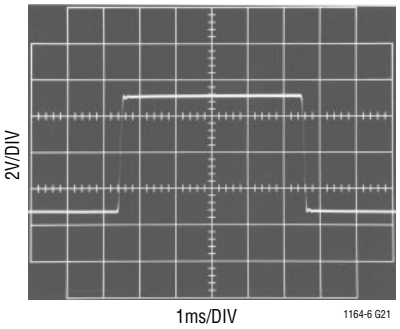


Transient Response



V_S = ±7.5V, V_{IN} = ±3V 100Hz SQUARE WAVE
f_{CLK} = 500kHz, (f_{CLK}/f_C) = 100:1, f_{CUTOFF} = 5kHz
ELLIPTIC RESPONSE

Transient Response



V_S = ±7.5V, V_{IN} = ±3V 100Hz SQUARE WAVE
f_{CLK} = 800kHz, (f_{CLK}/f_C) = 160:1, f_{CUTOFF} = 5kHz
LINEAR PHASE RESPONSE

PIN FUNCTIONS (14-Lead Dual-In-Line Package)

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/µs. When V^+ is applied before V^- and V^- could go above ground, a signal diode must be used to clamp V^-. Figures 1 and 2 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high

PIN FUNCTIONS (14-Lead Dual-In-Line Package)

level threshold value for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the right side of the IC package to avoid coupling into any input or output analog signal path. A 1k resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling, Figures 1 and 2.

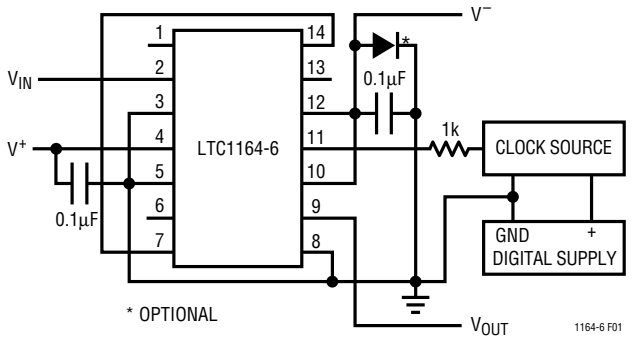


Figure 1. Dual Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

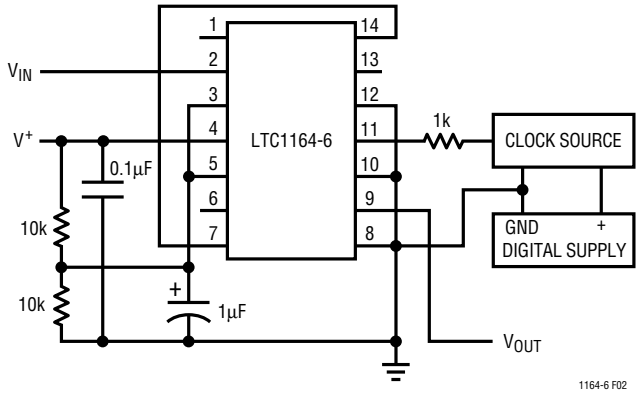


Figure 2. Single Supply Operation for f_{CLK}/f_{CUTOFF} = 100:1

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation pins 3 and 5 should be biased at 1/2 supply and they should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 2). For single 5V operation at the highest f_{CLK} of 1MHz, pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations (see Typical Performance Characteristics curves: Maximum Passband for Single 5V, 50:1; and THD + Noise vs RMS Input for Single 5V, 50:1).

Elliptic/Linear Phase Select Pin (10)

The DC level at this pin selects the desired filter response, elliptic or linear phase and determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 connected to V⁻ provides an elliptic lowpass filter with clock-to-f_{CUTOFF} ratio of 100:1. Pin 10 connected to analog ground provides a linear phase lowpass filter with a clock- to-f_{-3dB} ratio of 160:1 and a transient response overshoot of 1%. When pin 10 is connected to V^+ the clock-to-f_{CUTOFF} ratio is 50:1 and the filter response is elliptic. Bypassing pin 10 to analog ground reduces the output DC offsets. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source or sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 3,

PIN FUNCTIONS (14-Lead Dual-In-Line Package)

can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

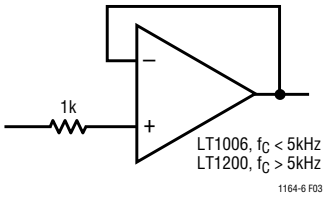


Figure 3. Buffer for Filter Output

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pin (1, 8, 13)

Pins 1, 8, and 13 are not connected to any internal circuit point on the device and should preferably be tied to analog ground.

APPLICATIONS INFORMATION

Passband Response

The passband response of the LTC1164-6 is optimized for a f_{CLK}/f_{CUTOFF} ratio of 100:1. Minimum passband ripple occurs from 1Hz to 80% of f_{CUTOFF}. Athough the passband of the LTC1164-6 is optimized for ratio f_{CLK}/f_{CUTOFF} of 100:1, if a ratio of 50:1 is desired, connect a single pole lowpass RC ($f_{-3dB} = 2\ f_{CUTOFF}$) at the output of the filter. The RC will make the passband gain response as flat as the 100:1 case. If the RC is omitted, and clock frequencies are below 500kHz the passband gain will peak by 0.4dB at 90% f_{CUTOFF}.

Table 2. Typical Passband Ripple with Single 5V Supply (f_{CLK}/f_C) = 100:1, GND = 2V, 30kHz, Fixed Single Pole, Lowpass RC Filter at Pin 9 (See Typical Applications)

PASSBAND FREQUENCY	PASSBAND GAIN (REFERENCED TO 0dB)			
	f_{CUTOFF} = 1kHz	f_{CUTOFF} = 10kHz		
% of f_{CUTOFF}	T_A = 25°C (dB)	T_A = 0°C (dB)	T_A = 25°C (dB)	T_A = 70°C (dB)
10	0.00	0.00	0.00	0.00
20	–0.02	0.00	0.01	0.01
30	–0.05	–0.01	–0.01	0.01
40	–0.10	–0.02	–0.02	0.02
50	–0.13	–0.03	–0.01	0.03
60	–0.15	–0.01	0.01	0.05
70	–0.18	–0.01	0.01	0.07
80	–0.25	–0.08	–0.05	0.02
90	–0.39	–0.23	–0.18	–0.05
f_{CUTOFF}	–2.68	–2.79	–2.74	–2.68

The gain peaking can approximate a $sin\ \chi/\chi$ correction for some applications. (See Typical Performance Characteristics curve, Passband vs Frequency and f_{CLK} at f_{CLK}/f_C = 50:1.)

When the LTC1164-6 operates with a single 5V supply and its cutoff frequency is clock-tuned to 10kHz, an output single pole RC filter can also help maintain outstanding passband flatness from 0°C to 70°C. Table 2 shows details.

Clock Feedthrough

Clock feedthrough is defined as, the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and, it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 3.

Table 3. Clock Feedthrough

V_S	50:1	100:1
±2.5V	$60\mu V_{RMS}$	$60\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$150\mu V_{RMS}$	$500\mu V_{RMS}$

Note: The clock feedthrough at ±2.5V supplies is imbedded in the wideband noise of the filter. (The clock signal is a square wave.)

APPLICATIONS INFORMATION

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transient.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and it cannot be reduced with post filtering. For instance, the LTC1164-6 wideband noise at ±2.5V supply is 100μV_{RMS}, 90μV_{RMS} of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LTC1164-6 optimizes AC performance versus power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown on Table 4.

Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-6 case, an input signal whose frequency is in the range of f_{CLK} ±4%, will be aliased back into the filter's passband. If, for instance, an LTC1164-6 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98.5kHz, 10mV_{RMS} input signal, a 1.5kHz, 10μV_{RMS} alias signal will appear at its output. When the LTC1164-6 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 5 shows details.

Table 4. Maximum V_{IN} vs V_S and f_{CLK}

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	1.5MHz	1V_{RMS} (f_{IN} > 35kHz)
	1MHz	3V_{RMS} (f_{IN} > 25kHz)
	≥1MHz	0.7V_{RMS} (f_{IN} > 250kHz)
±5V	1MHz	2.5V_{RMS} (f_{IN} > 25kHz)
	1MHz	0.5V_{RMS} (f_{IN} > 100kHz)
Single 5V	1MHz	0.7V_{RMS} (f_{IN} > 25kHz)
	1MHz	0.5V_{RMS} (f_{IN} > 100kHz)

Table 5. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = 1V_{RMS}) (kHz)	OUTPUT LEVEL (Relative to Input) (dB)	OUTPUT FREQUENCY (Aliased Frequency) (kHz)
f_{CLK}/f_C = 100:1, f_{CUTOFF} = 1kHz		
96 (or 104)	–75.0	4.0
97 (or 103)	–68.0	3.0
98 (or 102)	–65.0	2.0
98.5 (or 101.5)	–60.0	1.5
99 (or 101)	–3.2	1.0
99.5 (or 100.5)	–0.5	0.5
f_{CLK}/f_C = 50:1, f_{CUTOFF} = 2kHz		
192 (or 208)	–76.0	8.0
194 (or 206)	–68.0	6.0
196 (or 204)	–63.0	4.0
198 (or 202)	–3.4	2.0
199 (or 201)	–1.3	1.0
199.5(or 200.5)	–0.9	0.5

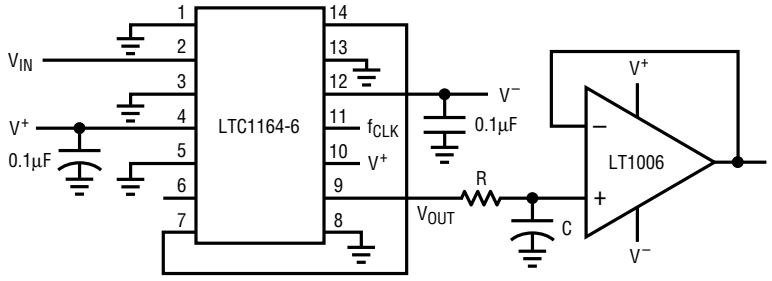
Table 6. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	0.50/f_C	0.34/f_C	0.80/f_C	0.5
LTC1164-5 Linear Phase	0.43/f_C	0.34/f_C	0.85/f_C	0
LTC1164-6 Linear Phase	0.43/f_C	0.34/f_C	1.15/f_C	1
LTC1264-7 Linear Phase	1.15/f_C	0.36/f_C	2.05/f_C	5
LTC1164-7 Linear Phase	1.20/f_C	0.39/f_C	2.20/f_C	5
LTC1064-7 Linear Phase	1.20/f_C	0.39/f_C	2.20/f_C	5
LTC1164-5 Butterworth	0.80/f_C	0.48/f_C	2.40/f_C	11
LTC1164-6 Elliptic	0.85/f_C	0.54/f_C	4.30/f_C	18
LTC1064-4 Elliptic	0.90/f_C	0.54/f_C	4.50/f_C	20
LTC1064-1 Elliptic	0.85/f_C	0.54/f_C	6.50/f_C	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

TYPICAL APPLICATIONS

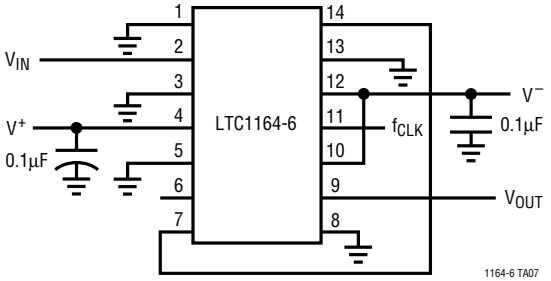
8th Order Elliptic Lowpass Filter
(f_{CLK}/f_C) = 50:1



NOTES:
1. OPTIONAL OUTPUT BUFFER
   $1/2\pi RC = 2 \times f_{CUTOFF}$.
2. PINS 1, 8, 13 CAN BE GROUNDED OR LEFT FLOATING.

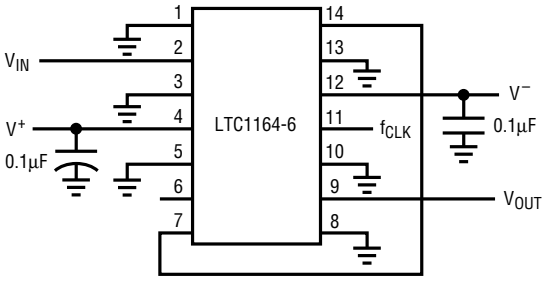
1164-6 TA06

8th Order Elliptic Lowpass Filter
(f_{CLK}/f_C) = 100:1



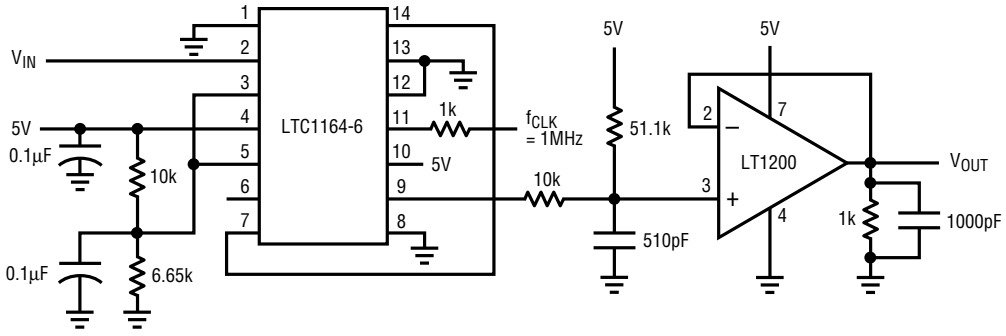
1164-6 TA07

8th Order Linear Phase Lowpass Filter
(f_{CLK}/f_C) = 160:1



1164-6 TA08

8th Order 20kHz Cutoff, Elliptic Filter Operating with a Single 5V Supply and Driving 1k, 1000pF Load

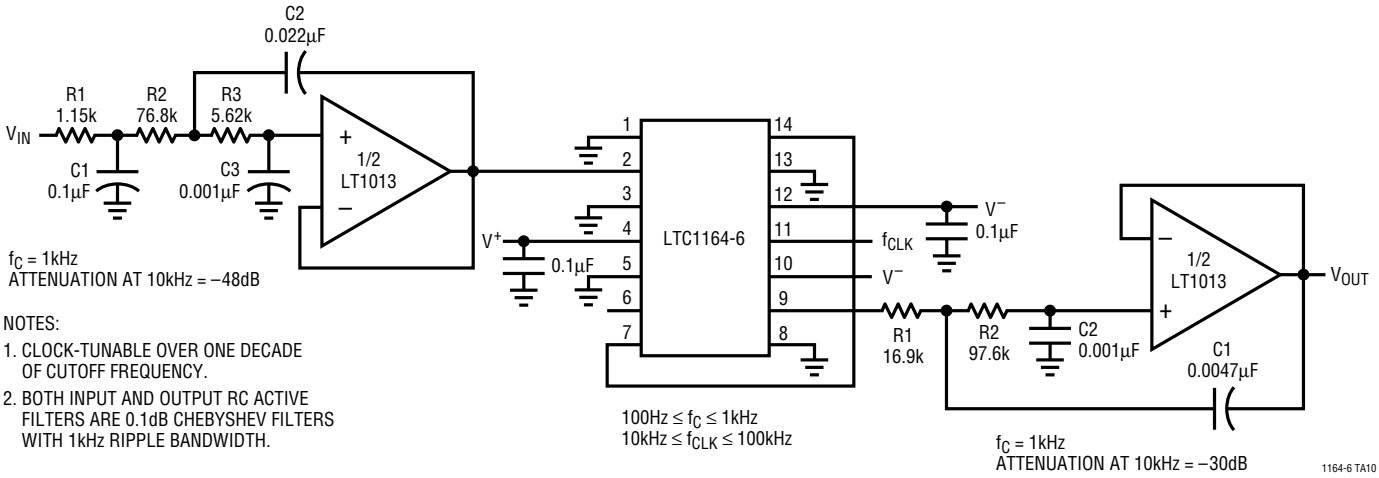


NOTES:
1. TOTAL SUPPLY CURRENT I_S = 4mA (EXCLUDING OUTPUT LOAD CURRENT).
2. FLAT PASSBAND UP TO 18kHz, f_{-3dB} = 20kHz.
3. THD + NOISE ≤ –70dB, $1V_{P-P} \leq V_{IN} \leq 3V_{P-P}$, f_{IN} = 1kHz.

1164-6 TA09

TYPICAL APPLICATIONS

8th Order Low Power, Clock-Tunable Elliptic Filter with Active RC Input Anti-Aliasing Filter and Output Smoothing Filter



f_C = 1kHz
ATTENUATION AT 10kHz = –48dB

NOTES:

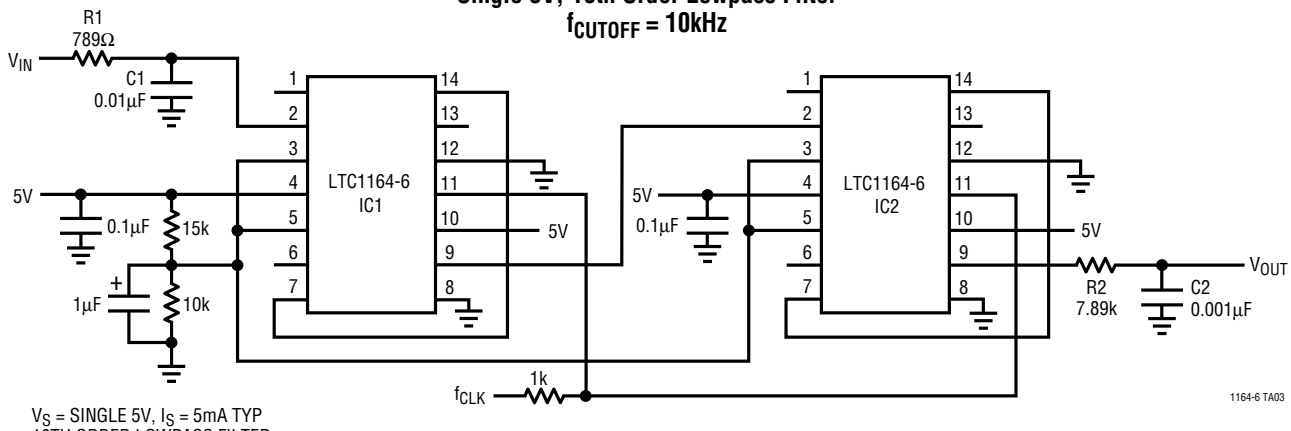
1. CLOCK-TUNABLE OVER ONE DECADE OF CUTOFF FREQUENCY.
2. BOTH INPUT AND OUTPUT RC ACTIVE FILTERS ARE 0.1dB CHEBYSHEV FILTERS WITH 1kHz RIPPLE BANDWIDTH.

100Hz ≤ f_C ≤ 1kHz
10kHz ≤ f_{CLK} ≤ 100kHz

f_C = 1kHz
ATTENUATION AT 10kHz = –30dB

1164-6 TA10

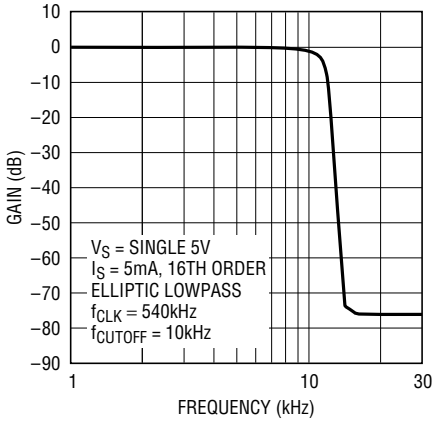
Single 5V, 16th Order Lowpass Filter
f_{CUTOFF} = 10kHz



1164-6 TA03

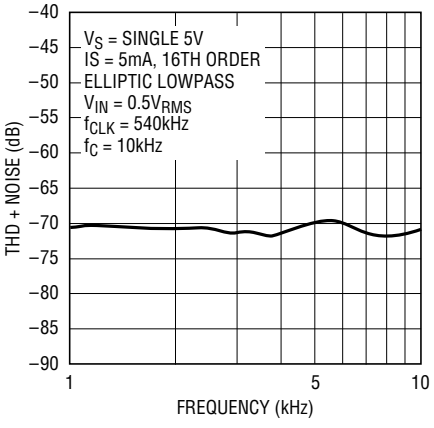
V_S = SINGLE 5V, I_S = 5mA TYP
16TH ORDER LOWPASS FILTER
FIXED f_{CUTOFF}, f_{CLK} = 540kHz
f_{CUTOFF} = 10kHz
(f_{CLK}/f_C) = 54:1
$1/2\pi R1C1 = 1/2\pi R2C2 = 2f_{CUTOFF}$

Gain vs Frequency



1164-6 TA04

THD + Noise vs Frequency

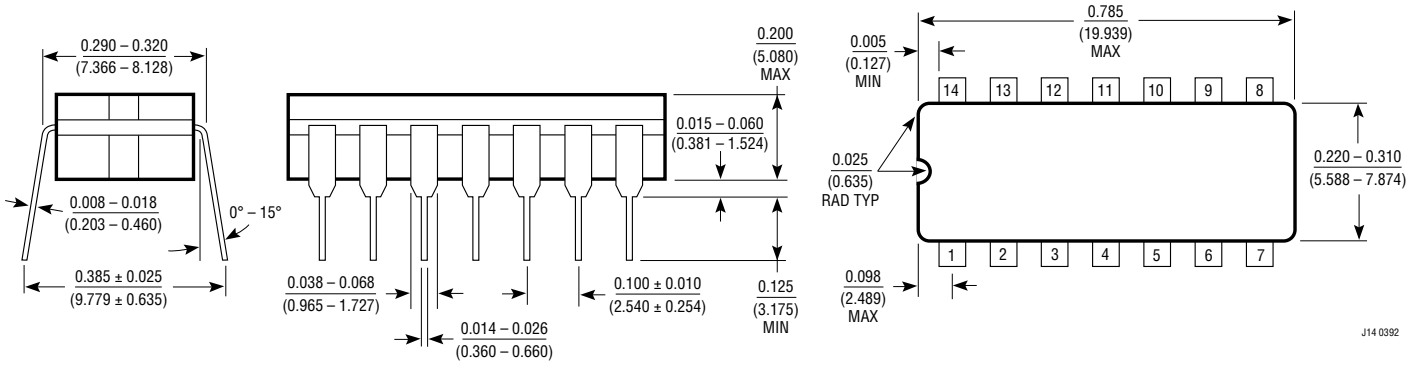


1164-6 TA05

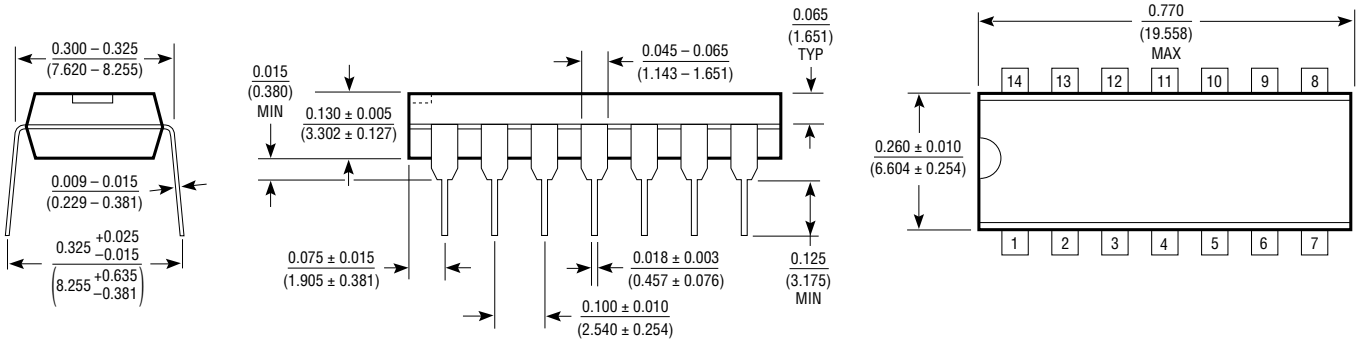
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

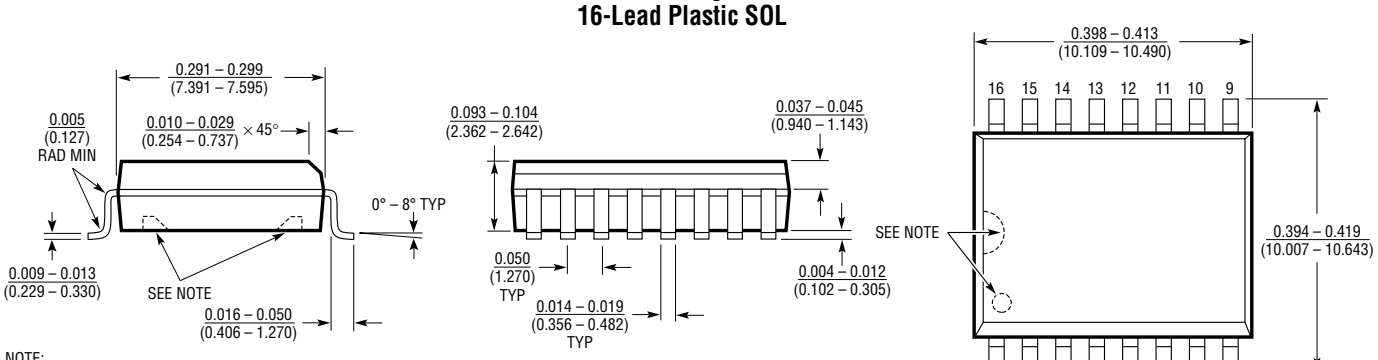
J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

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