G MICRO

PRELIMINARY

Notice: These are not a final specification. Some parametric limits are subject to change.

M33281GS-20

CMOS FLOATING-POINT PROCESSING UNIT (M32/FPU)

T-49-12-05

DESCRIPTION

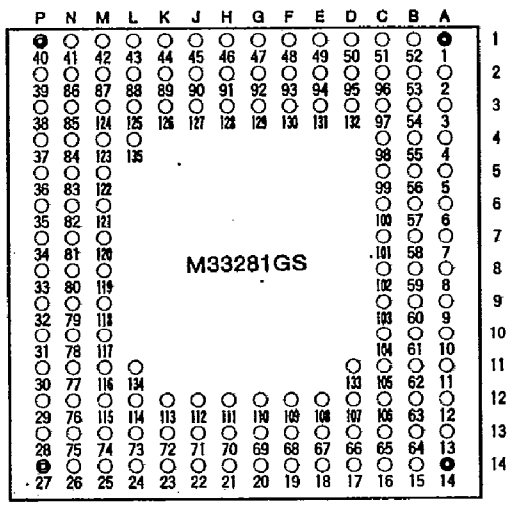
M33281GS-20 is a high-speed floating-point arithmetic LSI unit, and support the extended precision data format of IEEE standard.

The M33281GS-20 is designed to give maximum performance as a coprocessor for M32 family microprocessors (M33220GS-20, M33230GS-20). In addition to arithmetic operations and square roots, it has elementary function instructions, inner product instructions for fast matrix and vector calculations, area discrimination instructions for clipping discrimination, graphics oriented instructions and many more.

FEATURES

- Performance (20MHz operation with M33220GS-20)
  - Addition or subtraction 0.5μs
  - Multipulication 0.45μs
  - Division 1.5μs
- Elementary function calculation
- Graphics support
- Conforms to IEEE754
- Fast coprocessor interface
- Comprehensive system functions
- Softwave and system support
- Variety of instruction types
  - 31 arithmetic related
  - 21 control related
- 16 floating point operation registers (80-bit)

PIN CONFIGURATION (BOTTOM VIEW)



Outline 135S8X-A

- Peripheral device mode specifiable (for use when MPU lacks coprocessor interface)
- Package 135 pin PGA

APPLICATION

Scientific and technical calculations, engineering diagram processing

PIN ASSIGN

PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME	PIN CODE	PIN	NAME
A1	1	V_{SS}	B10	61	$\overline{CPDC}$	D12	107	D_{16}	H3	128	D_{10}	L14	24	V_{CC}	N9	79	V_{SS}
A2	2	A_{29}	B11	62	$\overline{BERR}$	D13	66	D_{19}	H12	111	V_{CC}	M1	42	V_{SS}	N10	78	V_{CC}
A3	3	$\overline{HACK}$	B12	63	$CPST_2$	D14	17	V_{CC}	H13	70	V_{SS}	M2	87	$FCPST_1$	N11	77	V_{CC}
A4	4	$\overline{BC_2}$	B13	64	V_{SS}	E1	49	V_{CC}	H14	21	V_{CC}	M3	124	LD	N12	76	V_{CC}
A5	5	R/$\overline{W}$	B14	15	V_{CC}	E2	94	D_3	J1	45	D_9	M4	123	$CPID_1$	N13	75	V_{SS}
A6	6	BAT_0	C1	51	V_{CC}	E3	131	D_0	J2	90	D_{11}	M5	122	$\overline{IRL}$	N14	26	V_{SS}
A7	7	V_{SS}	C2	96	V_{CC}	E12	108	D_{18}	J3	127	D_{13}	M6	121	V_{SS}	P1	40	V_{CC}
A8	8	NC	C3	97	A_{28}	E13	67	D_{21}	J12	112	D_{29}	M7	120	V_{SS}	P2	39	$\overline{RESET}$
A9	9	V_{SS}	C4	98	$\overline{BC_0}$	E14	18	D_{23}	J13	71	D_{27}	M8	119	V_{CC}	P3	38	$CPID_0$
A10	10	V_{SS}	C5	99	$\overline{BC_3}$	F1	48	D_6	J14	22	D_{26}	M9	118	V_{CC}	P4	37	V_{SS}
A11	11	V_{CC}	C6	100	V_{SS}	F2	93	D_4	K1	44	V_{SS}	M10	117	V_{CC}	P5	36	SIZ16
A12	12	V_{SS}	C7	101	BAT_2	F3	130	D_2	K2	89	D_{12}	M11	116	V_{CC}	P6	35	NC
A13	13	$CPST_0$	C8	102	V_{CC}	F12	109	D_{20}	K3	126	D_{15}	M12	115	V_{CC}	P7	34	V_{CC}
A14	14	V_{CC}	C9	103	V_{CC}	F13	68	V_{CC}	K12	113	D_{30}	M13	74	V_{CC}	P8	33	CLKf
B1	52	V_{SS}	C10	104	$\overline{RETRY}$	F14	19	V_{SS}	K13	72	D_{28}	M14	25	D_{31}	P9	32	V_{SS}
B2	53	V_{CC}	C11	105	$\overline{DC}$	G1	47	V_{SS}	K14	23	V_{SS}	N1	41	$FCPST_2$	P10	31	$\overline{FCPDC}$
B3	54	A_{27}	C12	106	$CPST_1$	G2	92	D_7	L1	43	V_{CC}	N2	86	V_{SS}	P11	30	V_{CC}
B4	55	$\overline{BC_1}$	C13	65	D_{17}	G3	129	D_5	L2	88	D_{14}	N3	85	UD	P12	29	V_{CC}
B5	56	$\overline{BS}$	C14	16	V_{SS}	G12	110	D_{22}	L3	125	V_{SS}	N4	84	$CPID_2$	P13	28	NC
B6	57	V_{CC}	D1	50	V_{SS}	G13	69	D_{24}	L4	135	V_{CC}	N5	83	V_{CC}	P14	27	V_{CC}
B7	58	BAT_1	D2	95	D_1	G14	20	D_{25}	L11	134	$FCPST_0$	N6	82	V_{CC}			
B8	59	V_{SS}	D3	132	V_{SS}	H1	46	D_8	L12	114	V_{SS}	N7	81	V_{SS}			
B9	60	$\overline{CDE}$	D11	133	V_{SS}	H2	91	D_{10}	L13	73	V_{SS}	N8	80	$\overline{CLKf}$			

Note. G_{MICRO}™ is a trademark of the G-MICRO group for the TRON specification microprocessors.

MITSUBISHI ELECTRIC

BLOCK DIAGRAM