PRELIMINARY

Notice ; This is not a final specification.
some parametric limits are subject to change.

MITSUBISHI SOUND PROCESSORS

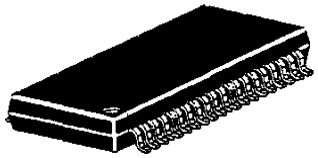
M65827FP

10-TIMES SPEED CD-DSP

FEATURES

•Normal speed to 8 times speed playback
•Multi speed selector
•Clock doubler
•Error correction(C1:2 error correction,C2:4 error correction)
•Channel control circuit (Bilingual / swap / (L+R)/2)
•Wide-band adjustment-free EFM-PLL
•CLV gain control
•Low power consumption and low radiation by 3.3V function of internal circuit

PACKAGE



Outline 42P2R

0.8mm Pitch 450mil SSOP
(8.4mm X 17.5mm X 2.0mm)

APPLICATION

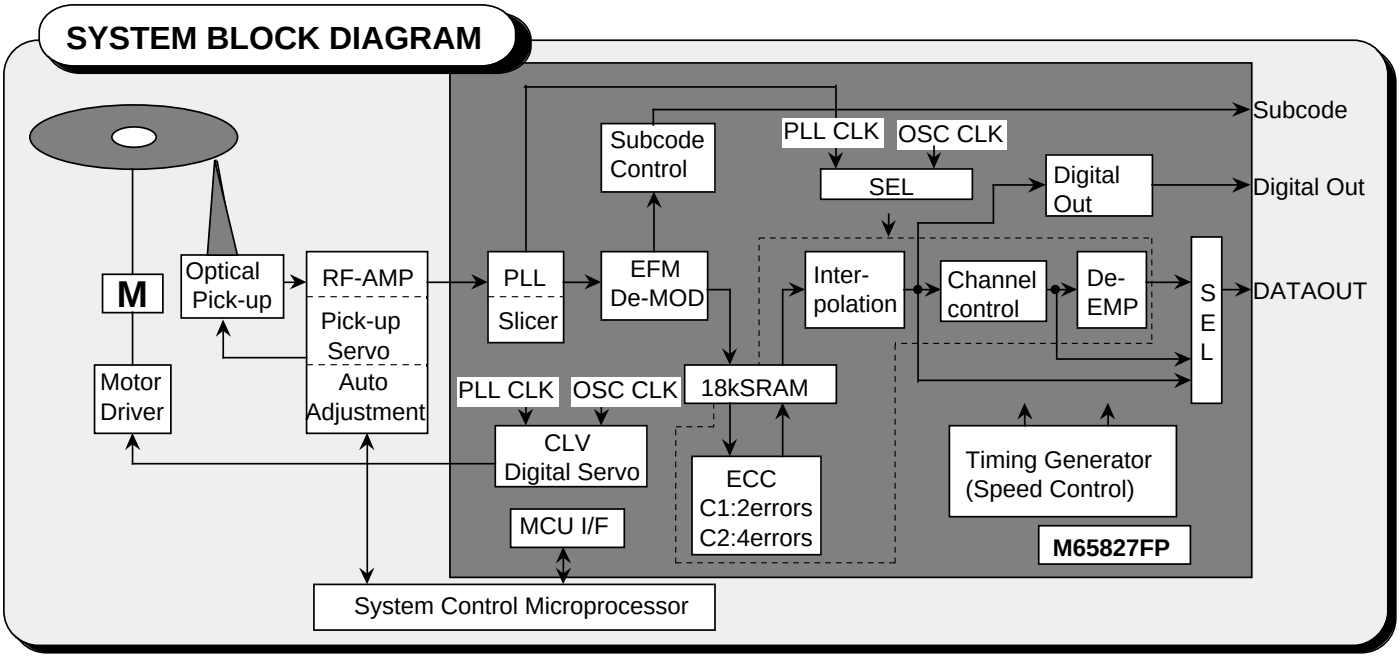
CD-ROM, CD-I, VIDEO-CD, etc.

RECOMMENDED OPERATING CONDITIONS

Supply voltage range ---------- 3.3V±10% (internal logic,analog circuits,oscillation circuit)
5.0V±10% (I/O buffer)

Rated voltage range ---------- 3.3V (internal logic,analog circuit)
5.0V (I/O buffer)

SYSTEM BLOCK DIAGRAM



BUILT IN FUNCTIONS

Block name	Description
Memory	•18 Kbit SRAM •±8 frames jitter margin
PLL	•Adjustment-free EFM-PLL •Wide-band lock range(1•8 times) •HF data slicer
EFM demodulation	•EFM demodulator •Frame synchronization detection / protection / interpolation •Frame synchronization monitor
Subcode control	•Subcode Q register •CRC checker •Subcode synchronous pattern detector (S0 and S1) •Emphasis flag detector and digital de-emphasis filter •Serial interface of subcode P~W (EIAJ CP-2401)
Error correction	•C1: 2 error correction, C2: 4 error correction (C1: 2 error correction, C2: 2 error correction selectable) •Unscramble / De-interleave •Error monitor
Interpolation	•Average and pre-hold interpolation (for CD-DA mode) •Interpolate prohibition (for CD-ROM mode)
DAC interface	•Mute control •Bilingual / swap / (L+R)/2 output •Lch / Rch independent attenuation control (256 steps) •Separate data output for CD-DA (DADT) and CD-ROM(ROMDT)
Digital output	•Based on EIAJ-1201 •C bit oscillation accuracy control •C bit source number control
Digital CLV servo	•PWM output •Low disc rotation detector •kick pulse control (256 steps) •Automatic brake control •CLV gain control
Oscillation circuit	•Master clock selector (Playback speed control) •Clock doubler •VCO clock selector
MCU interface	•CLV servo control / mute control / attenuating level control •Configuration control •Attenuator control •Channel control •Play back speed control •Analog switch control •Error monitor control •Track counter control •Interrupt mask •Kick timer control •Digital audio interface C bit control •Reset / sleep / clock disable control •Subcode Q interface

PIN DESCRIPTION TABLE

Name	No.	I/O	Description	Supply	Schmitt	Pull-Up
VDD•VSS						
DVDD5	1	—	Digital power supply (5V power supply for I/O buffer)	DVDD5		
DVDD3	2	—	Digital power supply (3.3V power supply for internal circuit)	DVDD3		
DVSS	42	—	Digital ground	—		
AVDD	14	—	Analog power supply (3.3V power supply for analog circuit)	AVDD		
AVSS	21	—	Analog ground	—		
Clock						
XI	41	I	Oscillator input	DVDD3		
XO	40	O	Oscillator output	DVDD3		
C423	38	O	Crystal half clock	DVDD5		
S846	34	O	Crystal / PLL system clock	DVDD5		
S423	35	O	Crystal / PLL half clock	DVDD5		
DXLPF	3	I/O	Clock doubler loop filter connect pin	DVDD3		
DXRC	12	O	Clock doubler frequency gain control pin	DVDD3		
PLL						
HFD	11	I	HF defect signal input	DVDD5	○	
IREF	13	I	Current reference	AVDD		
LPF	15	I/O	EFM-PLL loop filter connect pin	AVDD		
RC	16	O	EFM-PLL frequency gain control pin	AVDD		
HF	17	I	HF input	AVDD		
HPF1	18	O	High Pass Filter 1	AVDD		
HPF2	19	O	High Pass Filter 2	AVDD		
TLC	20	O	Data slicer charge pump output	AVDD		
Data output • Digital Audio Interface						
DADT	28	O	Audio data output	DVDD5		
ROMDT	31	O	CD-ROM data output	DVDD5		
LRCK	29	O	LR clock	DVDD5		
DSCK	30	O	Data shift clock	DVDD5		
DOTX	26	O	Digital audio interface output	DVDD5		

PIN DESCRIPTION TABLE (CONTINUED)

Name	No.	I/O	Description	Supply	Schmitt	Pull-Up
Subcode						
SBQS	5	O	Subcode Q interrupt signal	DVDD5		
SCAND	22	O	Subcode sync. signal output (S0 and S1)	DVDD5		
SBCO	23	O	Subcode data serial output	DVDD5		
EFFK	24	O	PLL frame clock output	DVDD5		
SCCK	25	I	Subcode data shift clock	DVDD5	◯	◯
CRCF	27	O	CRC flag output	DVDD5		
CLV						
PWM1	33	O	Spindle motor PWM output (-)	DVDD5		
PWM2	32	O	Spindle motor PWM output (+)	DVDD5		
Track counter						
TRIN	36	I	Track cross signal input	DVDD5	◯	
INT	37	O	Interrupting signal output	DVDD5		
MCU interface						
MCK	6	I	MCU shift clock input	DVDD5	◯	◯
R/W	7	I	MCU data read / write control	DVDD5	◯	◯
MSD	8	I/O	MCU data input / ouput	DVDD5		◯
MLA	9	I	MCU latch clock input	DVDD5	◯	◯
ALCR	10	I	Reset input	DVDD5	◯	
Monitor output						
EST	39	O	C1/C2 error flag output	DVDD5		
LOCK/DRD	4	O	Lock monitor output / Low disc rotation detect signal output / Frame synchronization status (SYCLK)	DVDD5		

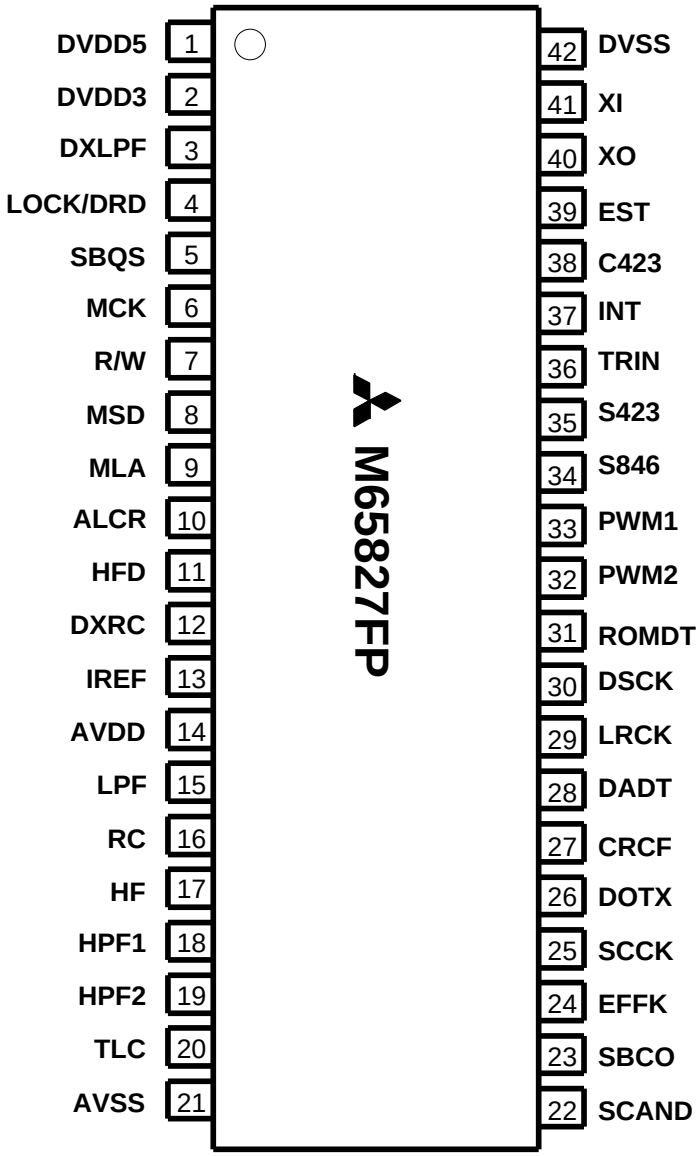
NUMERICAL PIN LIST

Name	No.	I/O	Description	Supply	Schmitt	Pull-Up
DVDD5	1	—	Digital power supply (5V power supply for I/O buffer)	DVDD5		
DVDD3	2	—	Digital power supply (3.3V power supply for internal circuits)	DVDD3		
DXLPF	3	I/O	Clock doubler loop filter connect pin	DVDD3		
LOCK/DRD	4	O	Lock monitor output / Low disc rotation detect signal output / Frame synchronization status(SYCLK)	DVDD5		
SBQS	5	O	Subcode interrupt signal output	DVDD5		
MCK	6	I	MCU shift clock input	DVDD5	○	○
R/W	7	I	MCU data read / write control	DVDD5	○	○
MSD	8	I/O	MCU data input / output	DVDD5		○
MLA	9	I	MCU latch clock input	DVDD5	○	○
ALCR	10	I	Reset input	DVDD5	○	
HFD	11	I	HF defect signal input	DVDD5	○	
DXRC	12	O	Clock doubler frequency gain control pin	DVDD3		
IREF	13	I	Current reference	AVDD		
AVDD	14	—	Analog power supply (3.3V power supply for analog circuits)	AVDD		
LPF	15	I/O	EFM-PLL loop filter connect pin	AVDD		
RC	16	O	EFM-PLL frequency gain control pin	AVDD		
HF	17	I	HF input	AVDD		
HPF1	18	O	High Pass Filter 1	AVDD		
HPF2	19	O	High Pass Filter 2	AVDD		
TLC	20	O	Data slice charge pump output	AVDD		
AVSS	21	—	Analog ground	——		
SCAND	22	O	Subcode syncronization status (S0 and S1)	DVDD5		
SBCO	23	O	Subcode data serial output	DVDD5		
EFFK	24	O	PLL frame clock output	DVDD5		
SCCK	25	I	Subcode readout clock	DVDD5	○	○
DOTX	26	O	Digital output	DVDD5		
CRCF	27	O	CRC flag output	DVDD5		

NUMERICAL PIN LIST (CONTINUED)

Name	No.	I/O	Description	Supply	Schmitt	Pull-Up
DADT	28	O	Audio data output	DVDD5		
LRCK	29	O	LR clock	DVDD5		
DSCK	30	O	Data shift clock	DVDD5		
ROMDT	31	O	CD-ROM data output	DVDD5		
PWM2	32	O	Spindle motor PWM output (+signal)	DVDD5		
PWM1	33	O	Spindle motor PWM output (-signal)	DVDD5		
S846	34	O	Crystal / PLL system clock	DVDD5		
S423	35	O	Crystal / PLL half clock	DVDD5		
TRIN	36	I	Track cross signal input	DVDD5	◯	
INT	37	O	Interrupt signal output	DVDD5		
C423	38	O	Crystal half clock	DVDD5		
EST	39	O	C2/C1 error output	DVDD5		
XO	40	O	Oscillator output	DVDD3		
XI	41	I	Oscillator input	DVDD3		
DVSS	42	—	Digital ground	—		

PIN CONFIGURATION



OUTLINE : 42P2R (Top view)

BLOCK DIAGRAM

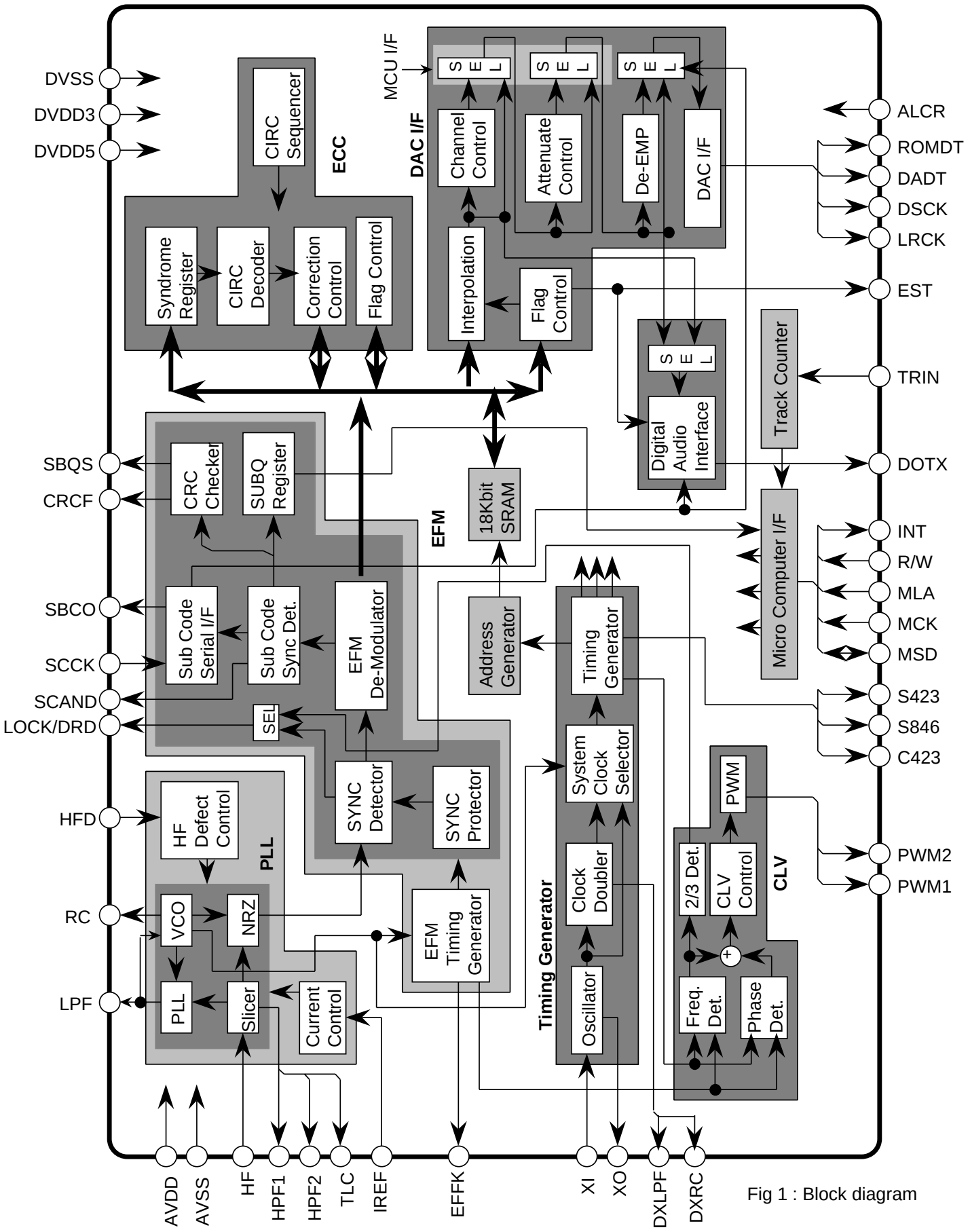


Fig 1 : Block diagram

ABSOLUTE MAXIMUM RATING

(Ta=25°C unless otherwise noted)

Symbol	Parameter	Condition	Limit	Unit
DVDD5-DVSS	Power supply voltage		-0.3 ~+7	V
DVDD3-DVSS	Power supply voltage		-0.3 ~+4.5	V
AVDD-AVSS	Power supply voltage		-0.3 ~+4.5	V
Vi	Input voltage		VSS-0.3≤Vi≤VDD+0.3	V
Vo	Output voltage		VSS≤Vo≤VDD	V
Pd	Power consumption		600	mW
Topr	Ambient temperature		-10 ~+70	°C
Tstg	Storage temperature		-40 ~+125	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Limit			Unit
			MIN	TYP	MAX	
DVDD5	5V digital power supply voltage		3.0	5.0	5.5	V
DVDD3	3.3V digital power supply voltage		3.0	3.3	3.6	V
AVDD	Analog supply voltage		3.0	3.3	3.6	V
V_{IH}	"H" output voltage		0.7DVDD		DVDD5	V
V_{IL}	"L" input voltage		DVSS		0.3DVDD	V
f_{OSC}	Oscillation frequency (X'tal)	Single speed		8.4672		MHz
		Double speed		16.9344		MHz
		Quad speed		33.8688		MHz
		6 times speed		50.8032		MHz
		8 times speed		67.7376		MHz
f_{VCO}	Oscillation frequency (VCO)	Single speed		8.6436		MHz
		Double speed		17.2872		MHz
		Quad speed		34.5744		MHz
		6 times speed		51.8616		MHz
		8 times speed		69.1488		MHz

ELECTRICAL CHARACTERISTICS

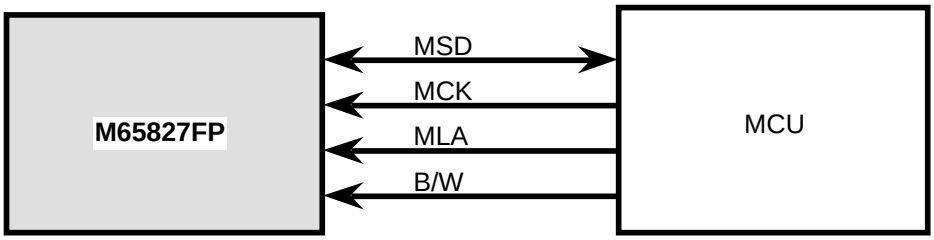
(Ta=25°C,DVDD5=5V, DVDD3=3.3V, AVDD=3.3V unless otherwise noted)

Symbol	Parameter	Condition		Limit			Unit
				MIN	TYP	MAX	
DVDD5	Operating voltage (5V, digital)	Ta=-10~+70°C		3.0	5.0	5.5	V
DVDD3	Operating voltage (3.3V, digital)	Ta=-10~+70°C	≤8X	3.0	3.3	3.6	V
			8X~10X	3.2	3.3	3.6	V
AVDD	Operating voltage (3.3V, analog)	Ta=-10~+70°C	≤8X	3.0	3.3	3.6	V
			8X~10X	3.2	3.3	3.6	V
| DD	Operating current	f osc=8.4672MHz f vco=8.6436MHz		—	20	50	mA
| OH	"H" output voltage	VDD=4.5V,| OH=-0.8mA		3.5	—	—	V
| OL	"L" output voltage	VDD=4.5V,| OL=0.8mA		—	—	0.4	V
| IH	"H" input current	VIH=4.5V		—	—	2	µA
| IL	"L" input current	VIL=0.5V		—	—	-2	µA
| OZH	Off condition "H" output current	VOH=4.5V		—	—	2	µA
| OZL	Off condition "L" output current	VOL=0.5V		—	—	-2	µA
f PLL1	VCO (EFFK) free run frequency (RIREF=110kΩ,RRC=91kΩ)	VLPF=1.0V		—	—	—	kHz
f PLL2		VLPF=1.5V		—	—	—	kHz
f PLL3		VLPF=3.0V		—	—	—	kHz
f DX1	Clock Doubler (S423) free run frequency (RIREF=110kΩ,RRC=91kΩ)	VLPF=1.0V		—	—	—	kHz
f DX2		VLPF=1.5V		—	—	—	kHz
f DX3		VLPF=3.0V		—	—	—	kHz
Rpu	Pull up resistance			25	50	100	kΩ

DETAILED DESCRIPTION

1. MCU interface

(1)Connection



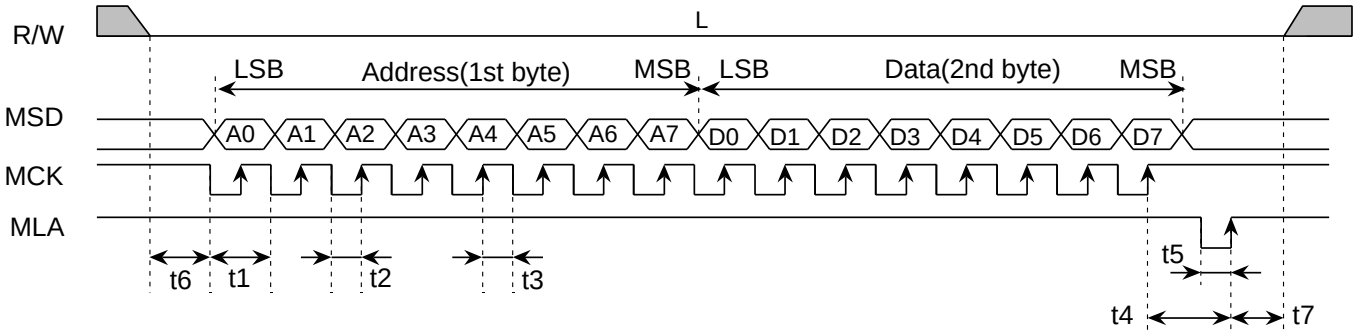
Pin No.	Signal name	Contents	I/O
8	MSD	MCU serial data input output pin	I/O
6	MCK	MCU shift clock input pin	I
9	MLA	MCU data latch clock input pin	I
7	R/W	Data read write control pin (H : Read, L : Write)	I

(2)Mode description

Address No.	Address								Data control
	A7	A6	A5	A4	A3	A2	A1	A0	
0	L	L	L	L	L	L	L	L	CLV servo, ATT, mute control
1	L	L	L	L	L	L	L	H	Configuration
2	L	L	L	L	L	L	H	L	Attenuation (Lch) control
3	L	L	L	L	L	L	H	H	Attenuation (Rch) control
4	L	L	L	L	L	H	L	L	Channel control
5	L	L	L	L	L	H	L	H	Playback speed control
6	L	L	L	L	L	H	H	L	Analog switch control
7	L	L	L	L	L	H	H	H	Monitor output select
8	L	L	L	L	H	L	L	L	Track counter (LSB)
9	L	L	L	L	H	L	L	H	Track counter (MSB)
A	L	L	L	L	H	L	H	L	Track counter interrupt value (LSB)
B	L	L	L	L	H	L	H	H	Track counter interrupt value (MSB)
C	L	L	L	L	H	H	L	L	Interrupt mask
D	L	L	L	L	H	H	L	H	Kick timer
E	L	L	L	L	H	H	H	L	Digital audio interface C bit control
F	L	L	L	L	H	H	H	H	Reset / Sleep / Clock disable control
80≥	H	X	X	X	X	X	X	X	Test Mode (For shipping test mode)

(3)Write timing

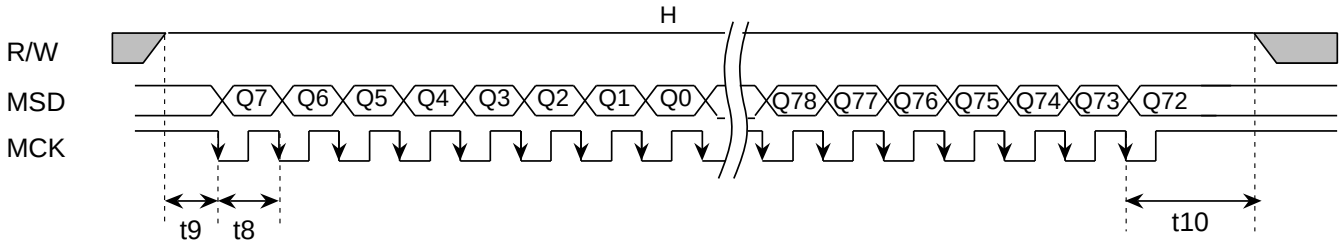
When R/W pin is L, MCU I/F is set in write mode. Address(1st byte) and data(2nd byte) are input with LSB first. Address and data are captured at the rising edge of MCK and are latched in internal register at the rising edge of MLA.



Symbol	Term	Min	Unit
t1	Shift clock pulse width	**200**	nsec
t2	Shift clock set up time	**100**	nsec
t3	Shift clock hold time	**100**	nsec
t4	Latch clock set up time	**200**	nsec
t5	Latch clock pulse width	**200**	nsec
t6	Write set up time	**250**	nsec
t7	Write hold time	**200**	nsec

(4)Read timing (Subcode Q register interface)

When R/W pin is H, MCU I/F is set in subcode Q register read mode. Subcode Q data output from MSD pin at the falling edge of MCK. Refer to (6) subcode Q I/F .



Symbol	Term	Min	Unit
t8	Shift clock pulse width	**200**	nsec
t9	Read set up time	**250**	nsec
t10	Read hold time	**400**	nsec

(5) Write mode

Address 00h CLV servo, Mute / ATT control

	Register name	0	1	Default
D0	Reserved	——	——	—
D1	S/S	CLV OFF (STOP)	CLV ON (START)	0
D2	BCON	Automatic brake mode	Manual brake mode	0
D3	BRAK	Manual brake OFF	Manual brake ON	1
D4	ATT	ATT OFF	ATT ON	0
D5	MUTE	MUTE ON	MUTE OFF	0
D6	TRST	Kick timer on	Kick timer off	1
D7	Reserved	——	——	—

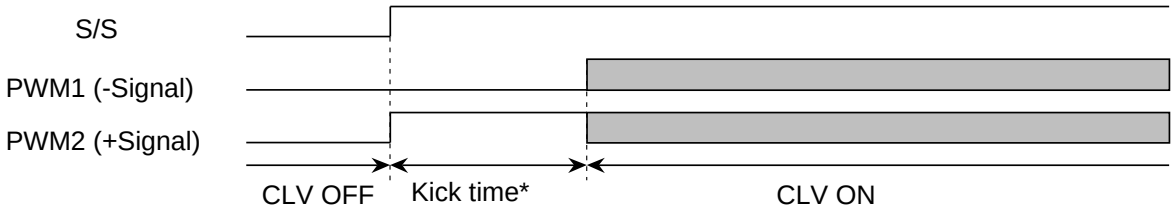
D0: Reserved

Don't care.

D1: S / S (Start / Stop)
D2: BCON (Automatic brake control)
D3: BRAK (Brake)

(1) Disc start

When S/S register changes from "0" to "1" , the kick pulse that is set by the kick control register at address 0Bh is output. After kick mode, disc rotation switched to CLV mode automatically.

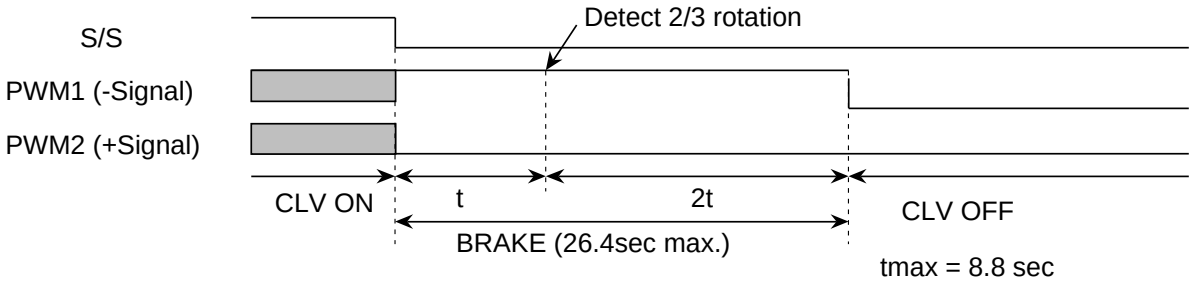


*Kick timer can be controlled by kick control register.

(2) Disc stop

(2-1) BCON=0 (Automatic brake mode)

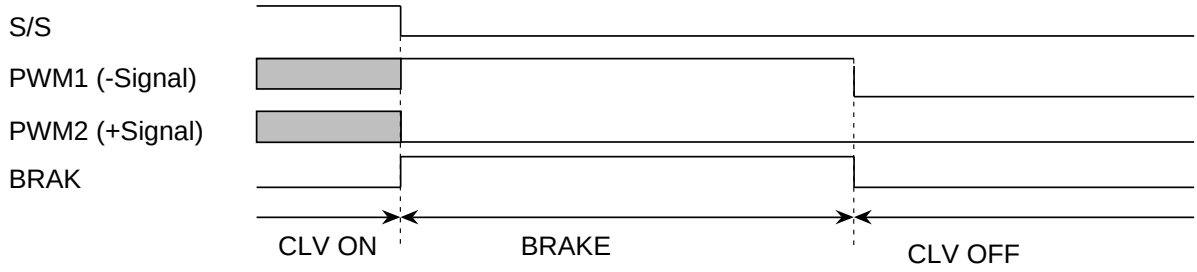
When S/S register changes from "1" to "0", the brake pulse that is calculated by the internal circuit output for the time 3t automatically. After brake mode, PWM switches to CLV off mode.
The time t is defined as the time that internal circuit detect the 2/3 rotation after S/S register changes 0. The time of detecting the 2/3 rotation can be monitored by DRD signal in LOCK/DRD pin.



tmax = 8.8 sec

(2-2) BCON=1 (Manual brake mode)

When S/S register change from "1" to "0", PWM output brake pulse while BRAK register is "1". This mode is used to stop the disc rotation by manual operation.



D4: ATT (Attenuate)

ATT=0: Attenuation OFF
ATT=1: The output data of DADT and ROMDT are attenuated by address 02h and 03h.

D5: MUTE

MUTE=0: Mute on for DADT and ROMDT.
MUTE=1: Mute off for DADT and ROMDT.

D6: TRST (kick timer reset)

TRST=0: Kick timer active
TRST=1: Kick timer stopped

D7: Reserved

Don't care

Address 01h Configuration

	Register name	0	1	Default
D0	NONAUDIO	Interpolation enable (Audio mode)	Interpolation disable (CD-ROM mode)	0
D1	ECCMOD	C1:2 errors correction C2:4 errors correction	C1:2 errors correction C2:2 errors correction	0
D2	FLPDIS	False-lock protection circuit On	Quasi-lock protection circuit Off	0
D3	PFHEN	VCO upper limiter OFF	VCO upper limiter ON	0
D4	HFDDIS	HFD enable	HFD disable	0
D5	GAINCNT	Normal CLV gain mode	CLV gain select mode	0
D6	GAINSEL	1/2 CLV gain mode	1/4 CLV gain mode	0
D7	Reserved		Inhibit	0

D0: NONAUDIO

NONAUDIO=0: Interpolation is enabled
C2 flag from EST pin output at 16 bit audioword unit.
NONAUDIO=1: Interpolation is disabled, prohibit interpolation.
C2 flag from EST pin output at 8 bit data byte unit.

D1: ECCMOD (Error correction mode)

ECCMOD=0: C1:2 error correction,C2:4 errors correction
ECCMOD=1: C1:2 error correction,C2:2 errors correction

D2: FLPDIS (False lock protection circuit disable)

FLPDIS=0: False lock protection circuit on
FLPDIS=1: False lock protection circuit off
(Refer to address 07h)

D3: PFHEN (VCO oscillation frequency upper limiter enable)

PFHEN=0: VCO oscillation frequency limiter is stopped
PFHEN=1: VCO oscillation frequency limiter is active

Limiter value = 8.6436MHz X 1.3 X S (S:Playback speed)

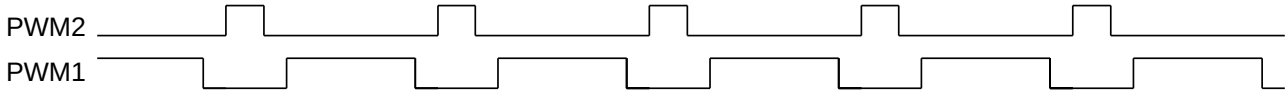
D4: HFDDIS (HFD disable)

HFDDIS=0: HFD input enable
HFDDIS=1: HFD input disable

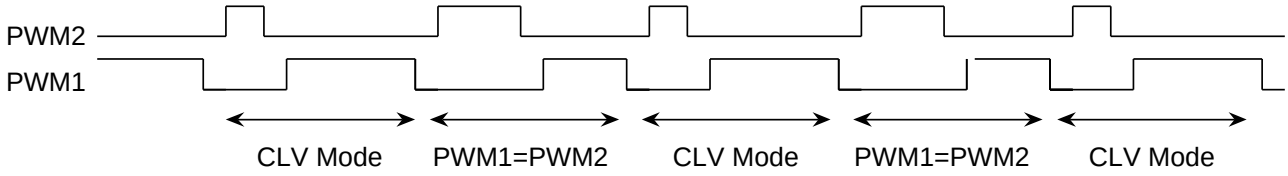
D5:GAINCNT(CLV gain control)
D6:GAINSEL(CLV gain select)

GAINCNT=0: Normal gain mode.
GAINCNT=1: CLV gain control mode.
CLV gain can be selected 1/2 and 1/4 of normal gain by GAINSEL register.

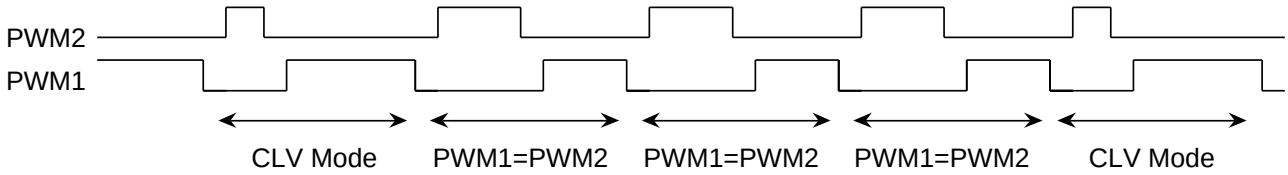
(a) Normal CLV gain mode (GAINCNT=0)



(b) 1/2 CLV gain mode (GAINCNT=1,GAINSEL=0)



(c) 1/4 CLV gain mode (GAINCNT=1,GAINSEL=1)



Address 02h / 03h Attenuation level control

MSB ⟷ LSB

Address	D7	D6	D5	D4	D3	D2	D1	D0
02h	L7	L6	L5	L4	L3	L2	L1	L0
03h	R7	R6	R5	R4	R3	R2	R1	R0
Default	0	1	0	0	0	0	0	0

Coefficience $L_{coe}= \sum_{n=0}^{7} L_n X2^{-(8-n)}$ $R_{coe}= \sum_{n=0}^{7} R_n X2^{-(8-n)}$

Attenuation $L_{ATT}=20 \times LOG(L_{coe})$ $R_{ATT}=20 \times LOG(R_{coe})$

Default value $L_{ATT}=R_{ATT}= -12dB$

When ATT register at address 00h is set to "1", the output data from DADT and ROMDT are attenuated by the attenuation level control register.

Address 04h Channel control

	Register name	0	1	Default
D0	CC1	Channel control register (Refer to Table 1)		1
D1	CC2			0
D2	CC3			0
D3	CC3			1
D4	DACIF	DAC interface mode 0	DAC interface mode 1	0
D5	DDEPASS	Automatic de-emphasis mode	De-emphasis pass mode	0
D6	SFLD	Software load on	Software load off	1
D7	AUTOLD	Automatic load off	Automatic load on	1

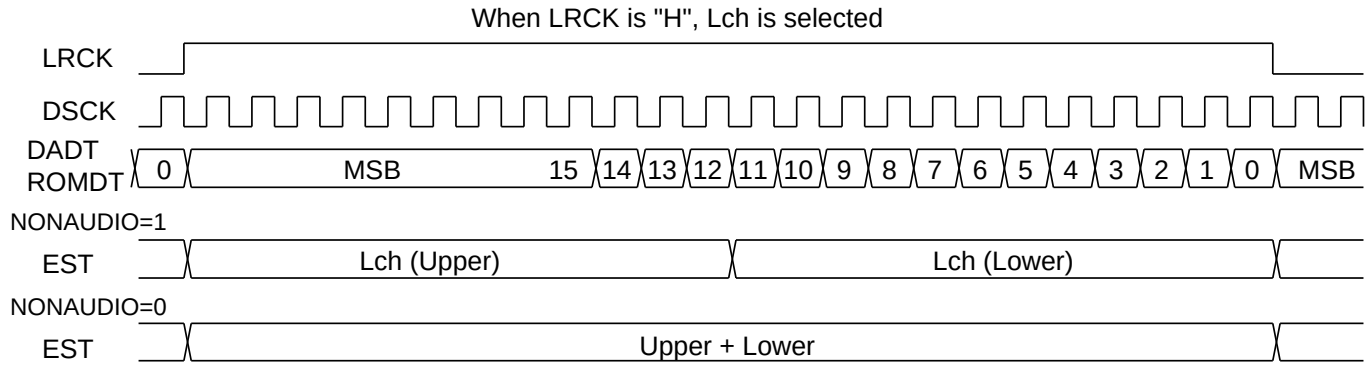
D0: CC0 (Channel control 0)
D1: CC1 (Channel control 1)
D2: CC2 (Channel control 2)
D3: CC3 (Channel control 3)

Table 1 : Channel control table

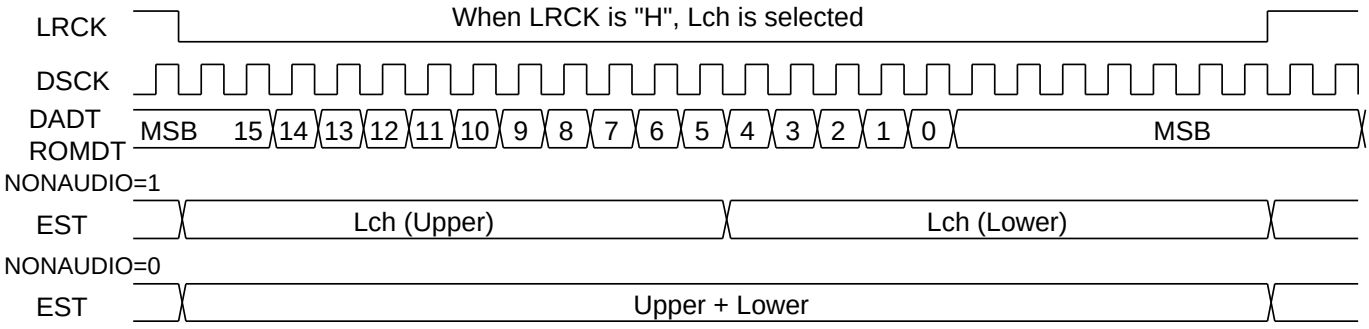
CC3	CC2	CC1	CC0	Lch output	Rch output	Note
L	L	L	L	MUTE	MUTE	MUTE
L	L	L	H	MUTE	R	
L	L	H	L	MUTE	L	
L	L	H	H	MUTE	(L+R)/2	
L	H	L	L	R	MUTE	
L	H	L	H	R	R	
L	H	H	L	R	L	SWAP
L	H	H	H	R	(L+R)/2	
H	L	L	L	L	MUTE	
H	L	L	H	L	R	STEREO
H	L	H	L	L	L	
H	L	H	H	L	(L+R)/2	
H	H	L	L	(L+R)/2	MUTE	
H	H	L	H	(L+R)/2	R	
H	H	H	L	(L+R)/2	L	
H	H	H	H	(L+R)/2	(L+R)/2	MONAURAL

D4: DACIF (DAC interface)

(1) DACIF=0 (DAC interface mode 0)



(2) DACIF=1 (DAC interface mode 1)



D5: DDEPASS (Digital de-emphasis pass)

DDEPASS = 0 : When emphasis flag is detected, internal digital de-emphasis circuit work automatically.
DDEPASS = 1 : Internal digital de-emphasis pass mode.

D6: SFLD (Software Load)

SFLD = 0 : When PLCKSEL register is 1, the EFM address counter is set the value that has ±8 frames jitter margin.
SFLD = 1 : EFM address counter is not influenced by this resister

D7: AUTOLD (Automatic Load)

AUTOLD = 0 : EFM address counter is not influenced by lock status.
AUTOLD = 1 :When PLCKSEL register is 1, the EFM address counter is set the value that has ±8 frames jitter margin at the LOCK point.

Address 05h Play back speed selector

	Register name	0	1	Default
D0	PLCKSEL	Xtal mode	PLL mode	0
D1	CKSEL0	Master clock selector (Refer to Table 2)		0
D2	CKSEL1			0
D3	CKSEL2			0
D4	PLSEL0	PLL clock selector (Refer to Table 3)		0
D5	PLSEL1			0
D6	DXSEL	Clock doubler not select	Clock doubler select	0
D7	DX24SEL	X 2	X 4	0

D0: PLCKSEL (PLCK select)

PLCKSEL=0: ECC circuit is worked by Xtal clock.
PLCKSEL=1: ECC circuit is worked by PLL clock.

D1: CKSEL0 (Clock select)
D2: CKSEL1 (Clock select)
D3: CKSEL2 (Clock select)

CKSEL2	CKSEL1	CKSEL0	Divide ratio
L	L	L	1
L	L	H	1/2
L	H	L	1/3
L	H	H	1/4
H	L	L	1/6
H	L	H	1/8
H	H	L	1/10
H	H	H	1/12

Table 2: Master clock selector

D4: PLSEL0 (PLL clock select)
D5: PLSEL1 (PLL clock select)

PLSEL1	PLSEL0	Divide ratio	Playback speed *
L	L	1	**Don't use**
L	H	1/2	**8X**
H	L	1/4	**2X,4X**
H	H	1/8	**1X**

Table 3: PLL clock selector

* Recommend value

D6: DXSEL (Clock doubler select)

DXSEL=0: Clock doubler does not select
DXSEL=1: Clock doubler select

D7: DX24SEL (Clock doubler 24 select)

DX24SEL=0: Double clock of Xtal is generated.
DX24SEL=1: Quad clock of Xtal is generated.

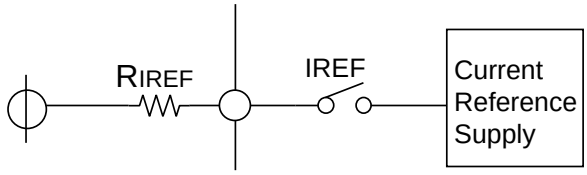
Address 06h Analog switch control

	Register name	0	1	Default
D0	IREF	OFF	ON	1
D1	Reserved			
D2	HPF1	OFF	ON	0
D3	HPF2	OFF	ON	0
D4	Reserved			
D5	Reserved			
D6	Reserved			
D7	Reserved			

D0: IREF (Current reference control resistance select)

Table 4: Current reference control

IREF	Function
L	Sleep
H	Current reference supply ON



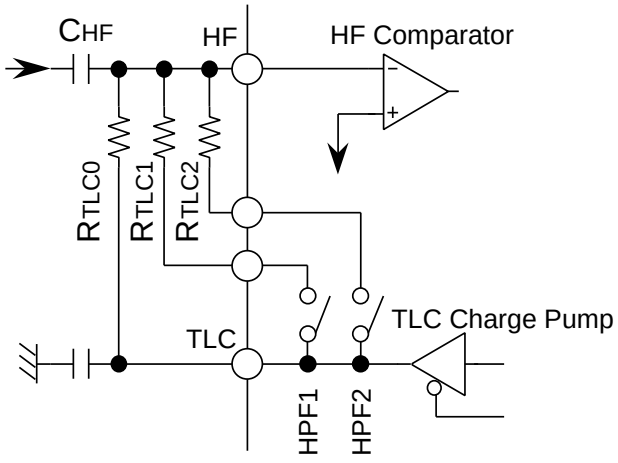
IREF=L: The analog block change to sleep mode by stopping the reference current to analog circuit.
Almost analog circuit stop the function, but the internal VCO does not stop the oscillation. Because the loop filter can not discharge. If VCO need to stop the oscillation in the sleep mode, please send the command (address:CEh, data:01h EFM-PLL charge pump output "L")
LSI change to low power supply mode by using the analog sleep mode and the digital sleep mode.

IREF=H: Set the reference current to analog circuit by the external resistor.

D2: HPF1 (HPF select 1)
D3: HPF2 (HPF select 2)

Table 5: High Pass Filter

HPF2	HPF1	External resistance value
L	L	R_{TLC0}
L	H	$R_{TLC0} \parallel R_{TLC1}$
H	L	$R_{TLC0} \parallel R_{TLC2}$
H	H	$R_{TLC0} \parallel R_{TLC1} \parallel R_{TLC2}$



These resisters are used to control the cut off frequency of the high pass filter that is composed by CHF and RTLC. This high pass filter is used to reject the defect (Example: Finger print)that can not be detected by the HF defect signal from SERVO IC.

PLAYBACK SPEED / ANALOG SWITCH CONTROL BLOCK DIAGRAM

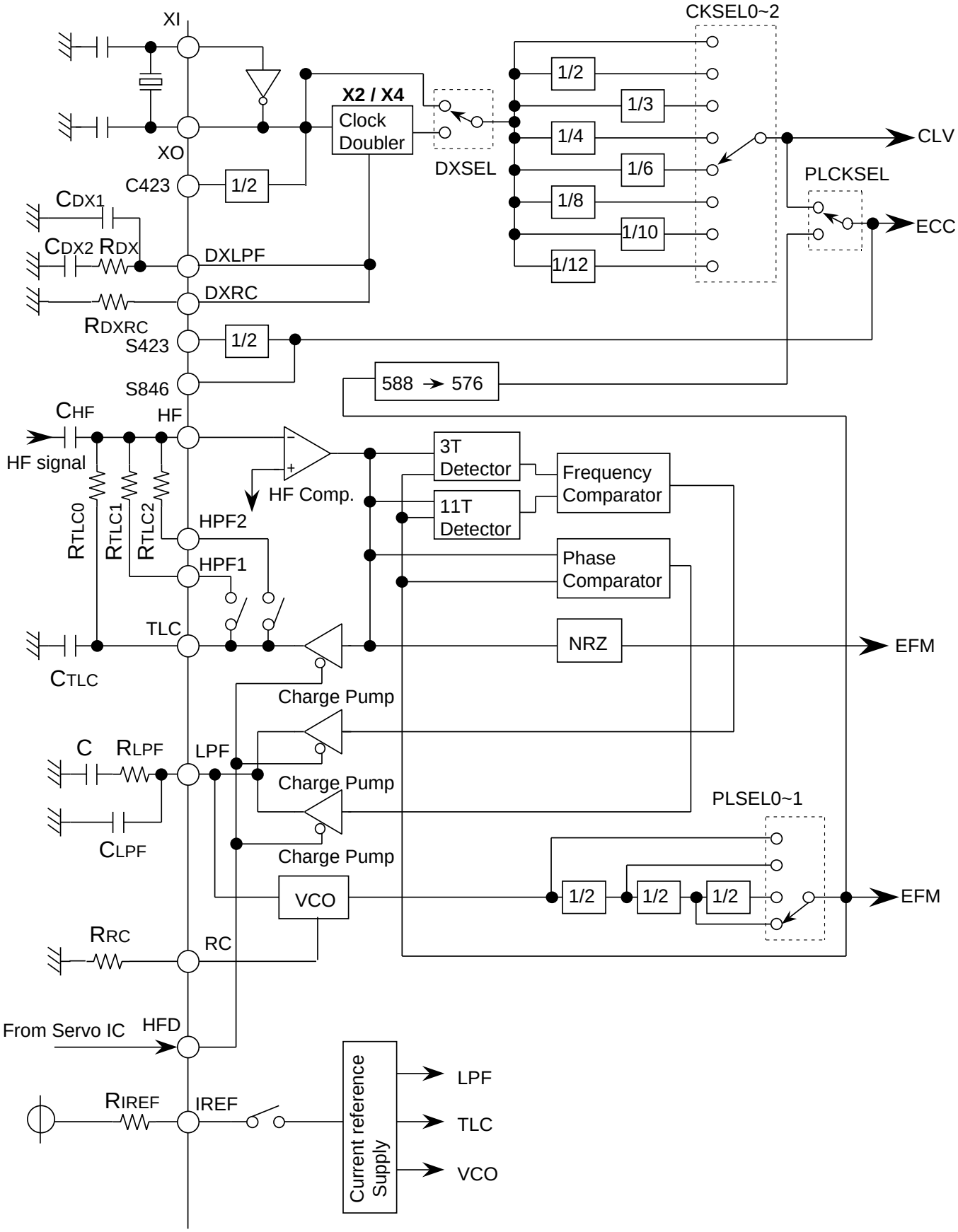


Fig. 2: Playback speed control / analog switch control block diagram

Address 07h Monitor control

	Register name	0	1	Default
D0	ERM0	Error monitor select (Refer to Table6)		0
D1	ERM1			0
D2	ERM2			0
D3	LOCKSEL0	Lock monitor select (Refer to Table7)		0
D4	LOCKSEL1			0
D5	LOCKMOD	Ignore disc rotation	Depend on disc rotation	0
D6	FLSEL0	False-lock protection clock duty select register (Refer to Table8)		0
D7	FLSEL1			0

D0: ERM0 (Error monitor select 0)
D1: ERM1 (Error monitor select 1)
D2: ERM2 (Error monitor select 2)

Table 6: Error monitor output

(a) 4 error correction mode

ERM2	ERM1	ERM0	EST output(error monitor)
L	L	L	C1,C2 decoder discorrectable
L	L	H	C2 decoder detects more than 4 errors
L	H	L	C2 decoder detects more than 3 errors
L	H	H	C2 decoder detects more than 2 errors
H	L	L	C2 decoder detects more than 1 errors
H	L	H	C1 decoder detects more than 3 errors
H	H	L	C1 decoder detects more than 2 errors
H	H	H	C1 decoder detects more than 1 errors

(b) 2 error correction mode

ERM2	ERM1	ERM0	EST output(error monitor)
L	L	L	C1,C2 decoder discorrectable
L	L	H	Disable
L	H	L	Disable
L	H	H	C2 decoder detects more than 2 errors
H	L	L	C2 decoder detects more than 1 errors
H	L	H	C1 decoder detects more than 3 errors
H	H	L	C1 decoder detects more than 2 errors
H	H	H	C1 decoder detects more than 1 errors

When ERM0, ERM1 and ERM0 are all "L", the error signal synchronize with the data from the DADT and ROMDT pins. The other mode can be used as an error monitor.

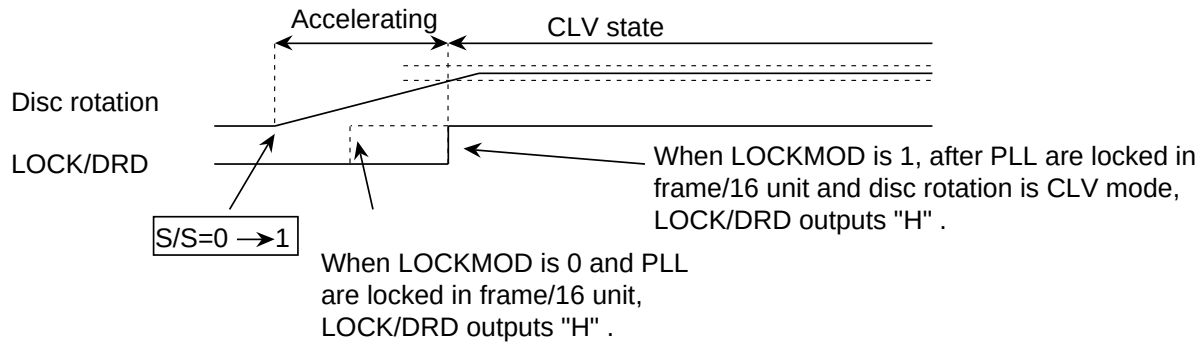
D3: LOCKSEL0 (Lock monitor select 1)
D4: LOCKSEL1 (Lock monitor select 0)

Table 7: LOCK/DRD output

LOCK SEL1	LOCK SEL0	LOCK/DRD output	Description
L	L	LOCK/DRD	BRAK register=0: LOCK monitor BRAK register=1: DRD output
L	H	SYCLK	Frame LOCK status output (H: Lock, L: Unlock)
H	L	LOCK	LOCK monitor output (H: Lock, L: Unlock)
H	H	DRD	Low disc rotation detect (H: Less than 2/3, L: More than 2/3)

D5: LOCKMOD (Lock mode)

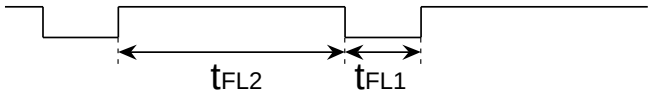
LOCKMOD=0: Independent of disc rotation, LOCK/DRD becomes "H" when PLL are locked in frame /16 unit.
LOCKMOD=1: LOCK/DRD becomes "H" when disc rotation gets close to target, perform CLV mode and PLL are locked in frame /16 unit.



D6: FLSEL0 (False-lock protection clock duty control register 0)
D7: FLSEL1 (False-lock protection clock duty control register 1)

Table 8: False-lock protection clock duty control register

FLSEL1	FLSEL0	Duty
L	L	**1/4**
L	H	**1/8**
H	L	**1/16**
H	H	**1/32**



$$\text{Duty} = \frac{t_{FL1}}{t_{FL1} + t_{FL2}} \qquad t_{FL1} + t_{FL2} = 557\text{msec} \times (1/S)$$

(S:Playback speed)

When mute data continue for a long time, PLL sometimes become hard to lock up. When the FLPDIS register at address 01h is "L", false-lock protection circuit adds stimulation to VCO control terminal which causes the PLL to lock up. False-lock protection circuit operates while false-lock protection clock is "L" (t_{FL1}) to increase VCO oscillation frequency.

This effect can be selected by the FLSEL1,0 register. This action can be stopped by the FLPDIS register at address 01h.

Address 08h / 09h Track counter control

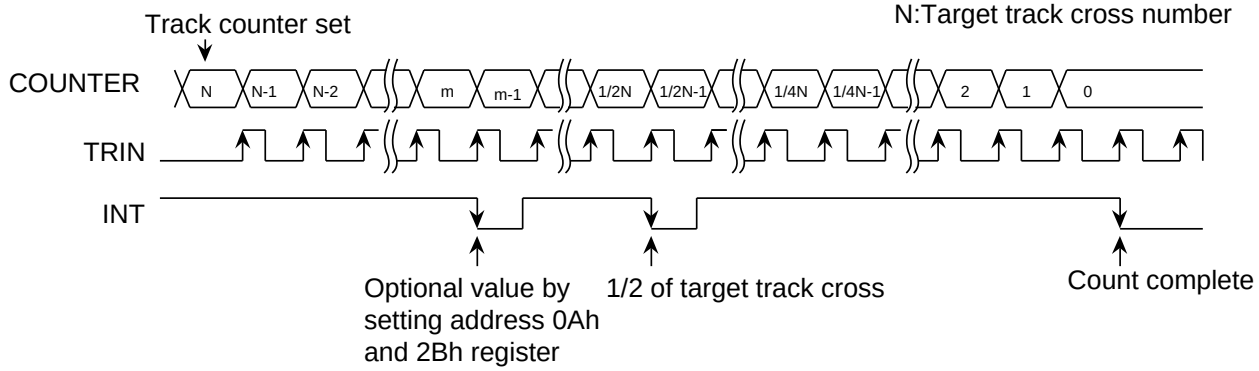
MSB ⟷ LSB

Address	D7	D6	D5	D4	D3	D2	D2	D1
08 h (LSB)	T7	T6	T5	T4	T3	T2	T1	T0
09 h (MSB)	T15	T14	T13	T12	T11	T10	T9	T8

Default = 0000h

Track counter value= $\sum_{n=0}^{15} T_n X2^n$

Up to 2^16 track cross signals can be counted by the internal track corss counter. After the target track cross number is set in the register by 2 byte data, the track cross counter is counted down at the rising edge of the track cross signal from servo LSI. Three kinds of the counter status can be output as the interrupt signal from INT pin by the interrupt mask register at address 0Ch.



Address 0Ah / 0Bh Track counter interrupt value control

MSB ⟷ LSB

Address	D7	D6	D5	D4	D3	D2	D2	D1
08 h (LSB)	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
09 h (MSB)	CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8

Default = 0000h

$$\text{Track counter interrupt value} = \sum_{n=0}^{15} CT_n \times 2^n$$

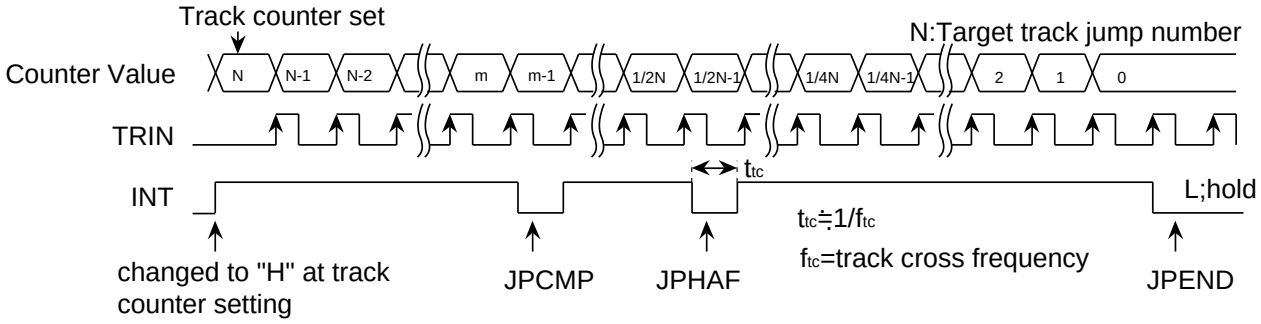
An optional interrupt value can be set by 2 byte in the track counter interrupt register. Interrupt signal outputs from INT pin. It can be prohibited by interrupt mask register at address 0Ch.

Address 0Ch Interrupt mask

	Register name	0	1	Default
D0	JPEND	No interrupt mode	Interrupt mode when track counter reches 0	0
D1	JPHAF	No interrupt mode	Interrupt mode when track counter reches 1/2 of set value	0
D2	JPCMP	No interrupt mode	Interrupt mode when track counter reches the optional set value at address 0Ah and 0Bh	0
D3	TRINO	Interrupt mode	Track cross signal output to INT pin directly	0
D4	MOVF	No interrupt mode	Interrupt mode when over ±8 frames jitter margin	0
D5	CLVDOWM	Rough servo off	Rough servo on (-)	0
D6	CLVUP	Rough servo off	Rough servo on (+)	0
D7	Reserved	0	Prohibit	0

D0: JPEND (Jump to end)
D1: JPHAF (Jump to half)
D2: JPCMP (Jump to comp)

When JPEND register is 1, the interrupt signal that output at counter reaches 0 is masked.
When JPHAF register is 1, the interrupt signal that output at counter reaches 1/2 of target track jump number is masked.
When JPCMP register is 1, the interrupt signal that output at counter reaches value of interrupt register at address 0Ah/0Bh is masked.

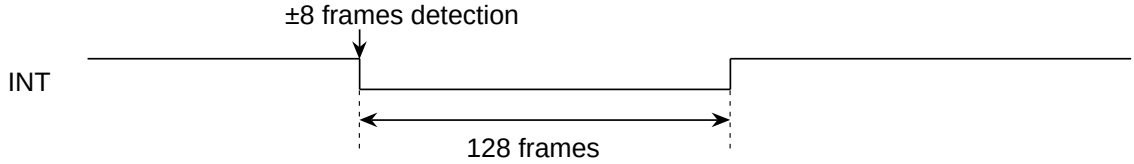


D3: TRINO (TRIN out)

TRINO=0: Interrupt signal which is set by D0~D2,D4 outputs to INT pin.
TRINO=1: Track cross signal input on the TRIN pin outputs to INT pin. At this time, the interrupt signal set by D0~D2,D4 is not be output.

D4: MOVF (Memory Over Flow)

MOVF=0: interrupt signal doesn't be generated.
MOVF=1: interrupt signal, which is generated when memory overflows exceeds ±8 frames of jitter margin, is masked. Interrupt signal becomes "L" when ±8 frames are detected and returns "H" after 128 frames pass.



1 frames = 136 / S µsec S:Playback speed (S times)

D5: SPMDOWN (Spindle motor down)
D6: SPMUP (Spindle motor up)

Rough servo mode can be realized by CLVDOWN and CLVUP register.

Table 9. Rough servo mode

SPMUP	SPMDOWN	PWM1(-)	PWM2(+)	Description
L	L	—	—	Normal mode
L	H	H	L	Rough servo (-) mode
H	L	L	H	Rough servo (+) mode
H	H	—	—	Prohibit

D7:Reserved

Set "0" in this register.

Command advantage about CLV servo is as follows.

Rough servo mode > Automatic CLV mode > CLV disable mode
(Address 0Ch) (Address 00h) (Address 0Ch)

Address 0Dh Kick timer control

MSB ← → LSB

Address	D7	D6	D5	D4	D3	D2	D2	D1
0Dh	S7	S6	S5	S4	S3	S2	S1	S0

Default = 20h

256 kinds of Kick pulse time can be set by 8 bit data.
Kick time is calculated as follows:

$$N = \sum_{n=0}^{7} T_n X 2^n$$ S : Playback speed

Kick Time T_{kick} =8.71 msec X N X (1/S)

Register of initial state are set to 20h (=32), kick time at single speed (S=1) is as follows:

T_{kick} =8.71 msec X 32 X (1/1) =278.72 msec.

Address 0Eh Digital audio interface C bit control

	Register name	0	1	Default
D0	ACCK0	Bit 28 of Cbit set to 0.	Bit 28 of Cbit set to 1.	0
D1	ACCK1	Bit 29 of Cbit set to 0.	Bit 29 of Cbit set to 1.	0
D2	SOURCE0	Bit 16 of Cbit set to 0.	Bit 16 of Cbit set to 1.	0
D3	SOURCE1	Bit 17 of Cbit set to 0.	Bit 17 of Cbit set to 1.	0
D4	SOURCE2	Bit 18 of Cbit set to 0.	Bit 18 of Cbit set to 1.	0
D5	SOURCE3	Bit 19 of Cbit set to 0.	Bit 19 of Cbit set to 1.	0
D6	DAOSEL	After channel control	Before channel control	0
D7	Reserved			

D0: ACCK0 (Crystal accuracy control 0)
D1: ACCK1 (Crystal accuracy control 1)

ACCK1	ACCK0	Description
0	0	Level ||
0	1	Level |||
1	0	Level |
1	1	Prohibited

Table 9 : Crystal accuracy control

D2: SOURCE0 (Source NO.0)
D3: SOURCE1 (Source NO.1)
D4: SOURCE2 (Source NO.2)
D5: SOURCE3 (Source NO.3)

SOURCE3	SOURCE2	SOURCE1	SOURCE0	Description
0	0	0	0	Default
0	0	0	1	Source NO.1
0	0	1	0	Source NO.2
0	0	1	1	Source NO.3
)	)	)	)	)
1	1	1	1	Source NO.16

Table 10: Source No. control

D6: DAOSEL (Digital audio interface select)

DAOSEL=0: Digital out is influenced by channel control and attenuation circuit.
DAOSEL=1: Digital out is not influenced by channel control and attenuation circuit.

Address 0Fh Soft reset / sleep / clock disable control

	Register name	0	1	Default
D0	SRST	Soft reset OFF	Soft reset ON	0
D1	HRST	Hard reset OFF	Hard reset ON	0
D2	SLP	Sleep OFF	Sleep ON	0
D3	TXDIS	Digital output ON	Digital output OFF	0
D4	C4DIS	C432 ON	S423 OFF	0
D5	S8DIS	S846 ON	S846 OFF	0
D6	S4DIS	S423 ON	C432 OFF	0
D7	APC EN	APC OFF (PLCKSEL=1)	APC ON (PLCKSEL=1)	0

D0: SRST (Soft reset)

SRST=0: Soft reset OFF
SRST=1: Default value are set in the write register by soft reset.
This register returns to "0" after soft reset.

D1: HRST (Hard reset)

HRST=0: Hard reset OFF
HRST=1: LSI resets are carried out. Reset state continued while HRST register is "1".
Reset is canceled by sending "0" to HRST register.

D2: SLP (Sleep)

SLP=0: Sleep OFF
SLP=1: Internal RAM and digital circuits can be put into sleep mode to reduce power consumption while the LSI is not in use. Sleep mode can be canceled by external reset or hard reset using the HRST register.
Using address 06h, the analog circuits can also be put into sleep mode

D3: TXDIS (Digital out disable)

TXDIS=0: Digital out data output from DOTX pin.
TXDIS=1: Digital out disabled and DOTX fixed to "L"

D4: C4DIS (C423 disable)

C4DIS=0: Crystal system clock output from C423 pin
C4DIS=1: C423 pin disabled and fixed to "L"

D5: S8DIS (S846 disable)

S8DIS=0: S846 pin output crystal or PLL master clock.
S8DIS=1: S846 pin disabled and fixed to "L"

D6: S4DIS (S423disable)

S4DIS=0: S423 pin output crystal or PLL system clock.
S4DIS=1: S423 pin disabled and fixed to "L"

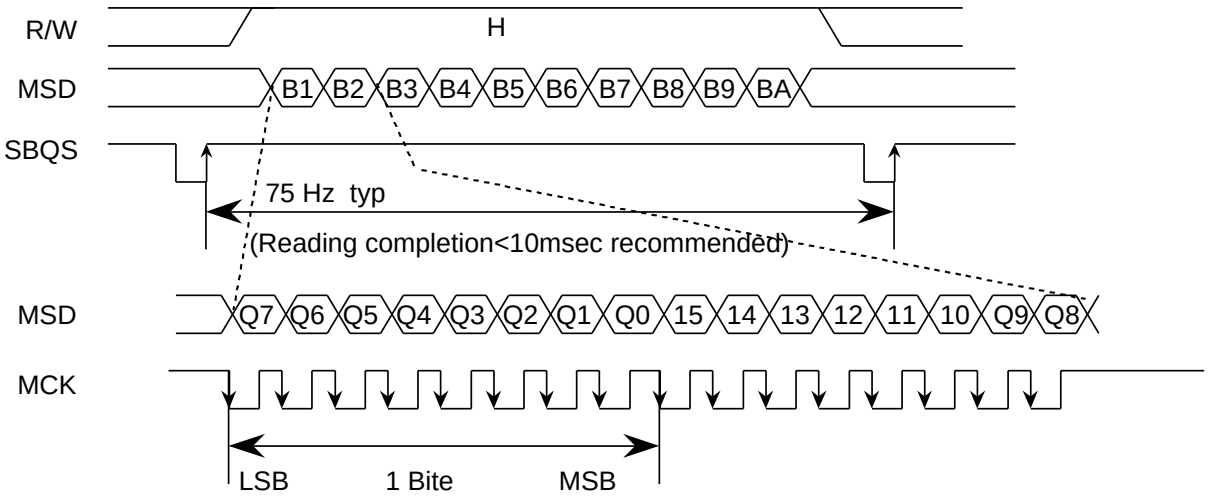
D7: APC EN (APC ENABLE)

APCEN=0: Automatic phase control circuit in CLV servo is disabled
APCEN=1: Automatic phase control circuit in CLV servo is enabled

When PLCKSEL register is "1", APCEN register influence APC function
When PLCKSEL register is "0", APCEN register is ignored.

(6) Read mode

Subcode Q I/F



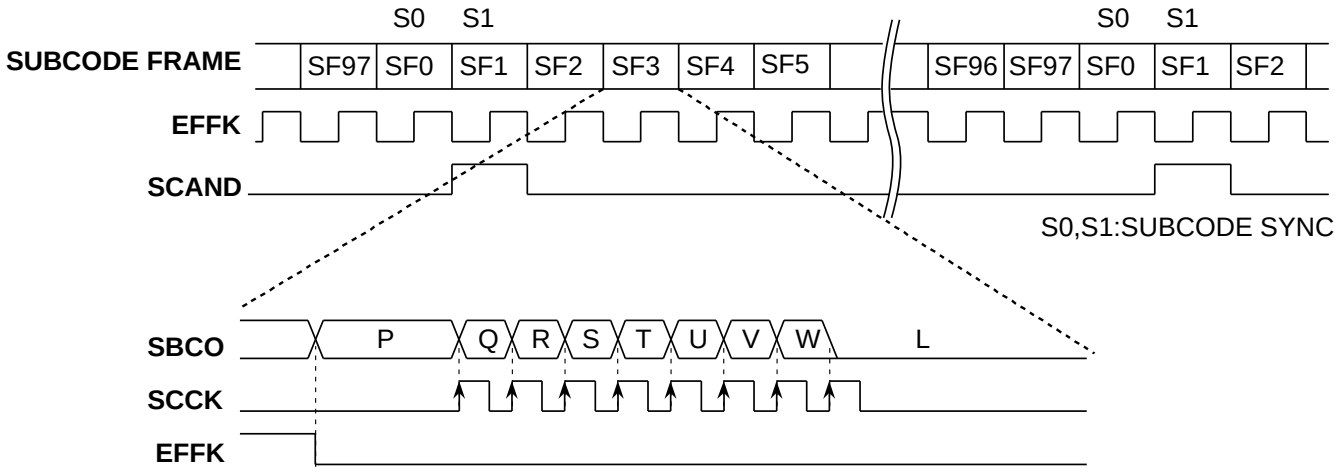
Subcode Q data which is stored in internal 80 bit register can be read in serial clock of MCU.
When R / W signal is "H", MSD are settled to output. By inputting 80 ck to MCK pin between two rising edges of SBQS pin, MSD pin output subcode Q data at the falling edge of MCK. Subcode Q data are output reversed MSB, LSB in 8 bit unit. SBQS pin output "L", when next condition are satisfied and internal register can be read.

<Condition that SBQS pin outputs "L">
a)CRC flag is OK.
b)Subcode synchronization signals S0,S1 are both detected at fixed position. (S0 AND S1)
When conditions a) and b) are both satisfied, SBQS pin outputs "L".

SBQS outputs 75Hz typ (=13.3msec) at single speed playback. In the case of S-times speed playback, it outputs S x 75Hz (13.3msec / S) so please notice when MCU design. Subcode Q register is valid from the rising edge of SQBS to the next rising edge. For actual design, please read subcode Q. (Normal speed playback: recommend less than 10msec readout completion)

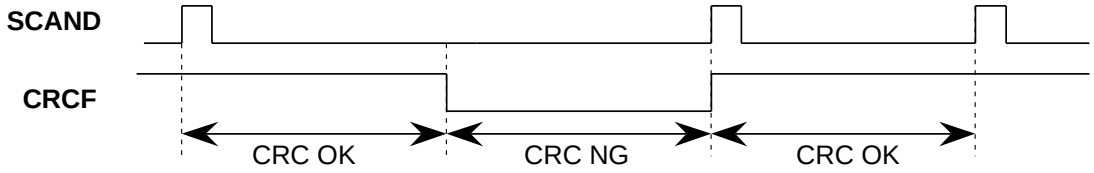
2.Subcode interface

Among the data which are converted from 14 bits EFM signals to 8 bits symbols, subcode P,Q,R,S,T,U,V and W are output from SBCO pin by inputting a shift clock to SCCK pin. If input frequency to SCCK is more than 8ck, SBCO becomes "L".



Subcode data synchronization status SCAND outputs "H" only when subcode synchronization patterns both S0 and S1 (S0 AND S1) are detected within a both fixed area of internal synchronization protection circuit.

Subcode Q CRC check outputs to CRCF pin. When CRC is OK, CRCF changes to "H", when CRC is NG, CRCF becomes "L".



Correspondence with EIAJ CP-2401 are as follows:

M65827FP	CP-2401	Signal variation
SCAND	SBSY	Subcode block synchronization
EFFK	SFSY	Subcode frame synchronization
SCCK	CLCK	Shift clock
SBCO	DATA	Output data

Table 11: Subcode serial interface corresponding table

3.EFM-PLL CIRCUIT

(1) Data slicing / PLL

The M65827FP has an analog front-end for incoming HF(EFM) signal. Using CMOS - Analog technology, the front - end is comprised of an automatic slice level control circuit and EFM-PLL circuit with internal adjust - free VCO. Under figure shows a block - diagram of the analog front - end. The HF signal is sliced by the HF comparator and a DC level is fed back from TLC to HF through some the external CR. If HFD becomes "H" because of defect in disc, then TLC becomes off state and holds the DC level. EFM - PLL is for extracting the EFM clock signal from the HF signal. The PLL circuit has a phase / frequency comparator so the M65827FP has a wide capture / lock range and there is no need to adjust the VCO. LPF is the charge-pump output and same-time control voltage input to the VCO.LPF becomes off state if HFD becomes "H".

M65827FP has an analog switch which it exchanges the analog external constants for playback speed (Refer to address 06h).

When VCO frequency is higher than 1.3 of target frequency, high frequency limiter suppress VCO frequency. High frequency limiter can be disabled by D3 bit of address 01h. Low frequency limiter is used for not stopping VCO oscillation; it can not be controlled this from the outside.

Sync loss counter becomes active when synchronization signal can't be detected, prevent from carrying out frequency comparator by instant synchronization pattern omission generated from disc defection.

IREF is the reference current input used to determine the current of the TLC and LPF charge pumps, the operating point of the HF comparator, and the VCO free run frequency. If IREF is connected to a noisy power supply through a resistor, VCO would be modulated and the error rate would increase. Therefore, power supply noise at IREF must be held to a minimum.

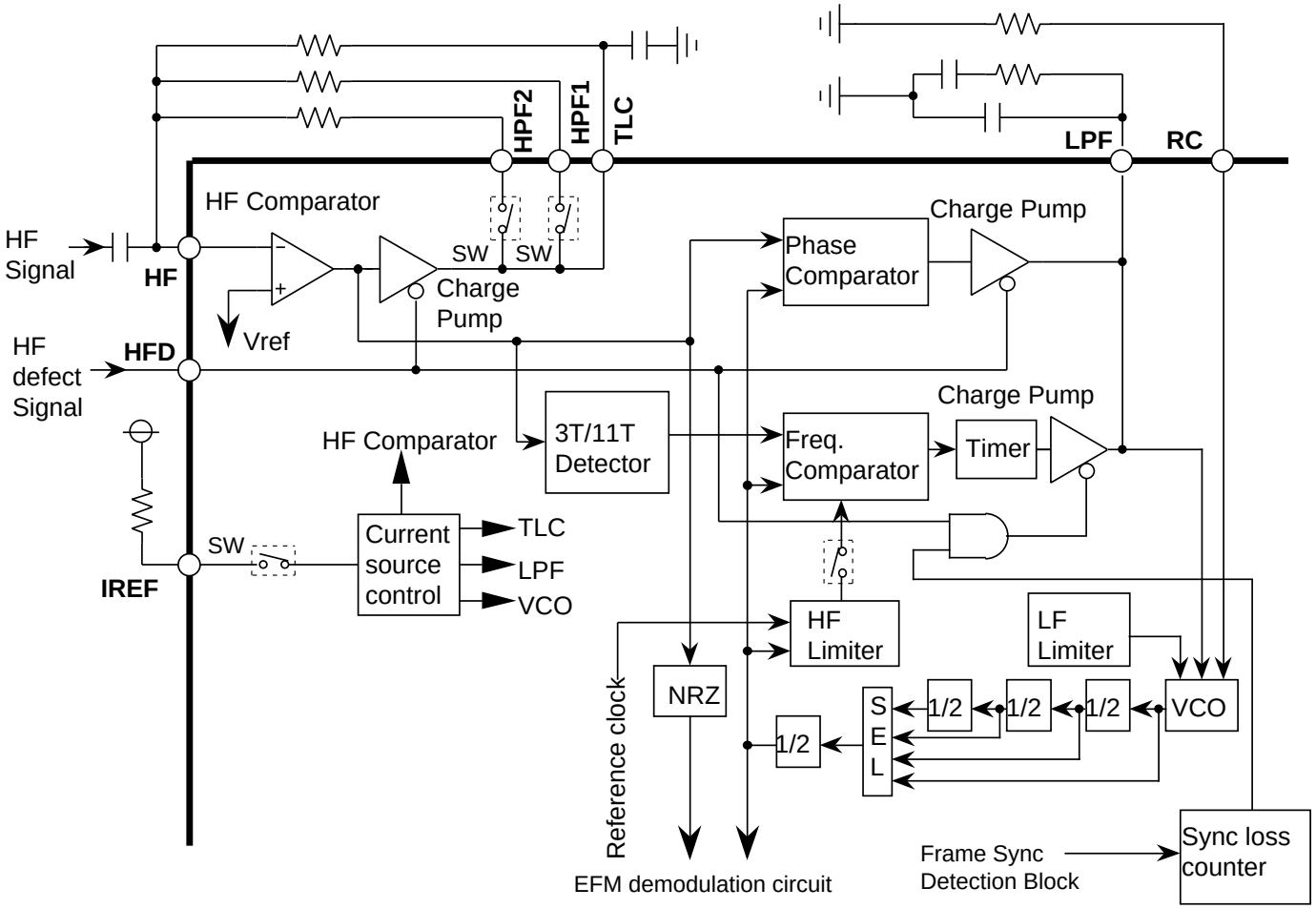
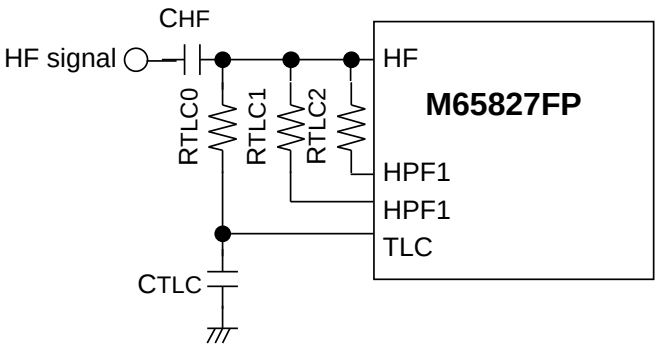


Fig. 3: EFM - PLL BLOCK DIAGRAM

(2) Slice level control

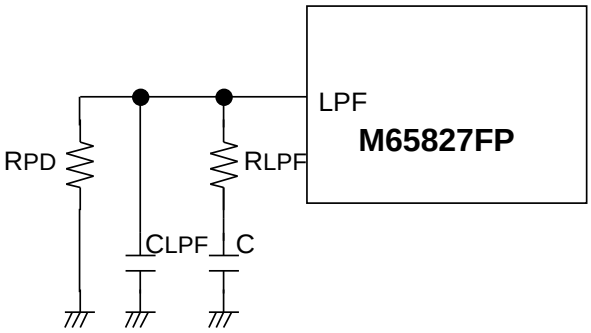


The slice level control circuit is formed by connecting resistors and capacitors to the HF(High - frequency signal input) and TLC (Slice level control output) pins.

(Recommend value)

CHF= 0.0022µF
CTLC= 0.022µF
RTLC0= 33KΩ
RTLC1= 33KΩ
RTLC2= 16KΩ
Vin= more than 0.5Vp-p

(3) PLL circuit

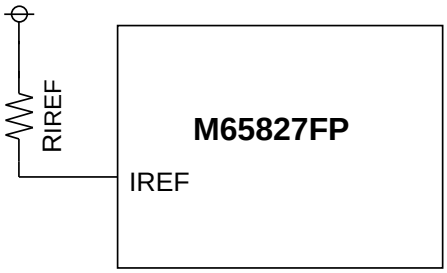


Since the adjustment - free VCO is built in, the adjustment - free PLL circuit can be formed by connecting a resistor and capacitors to the LPF(Low Pass Filter) pin.

(Recommend value)

CLPF= 470pF
C= 0.068µF
RLPF= 1.8KΩ
RPD= 560KΩ

(4) Reference current control

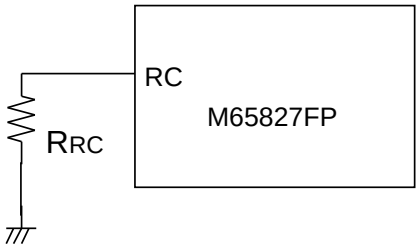


Resistors must be connected between the IREF pin and VDD in order to set the reference current used in determining the current values of the TLC pin and LPF pin, the comparator operating current of the slice level control circuit, and VCO free - run frequency.

(Recommend value)

RIREF= 75KΩ

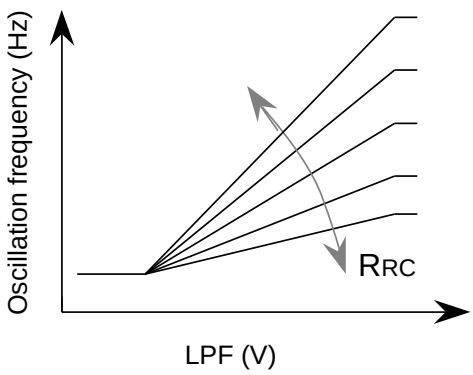
(5) VCO frequency gain control

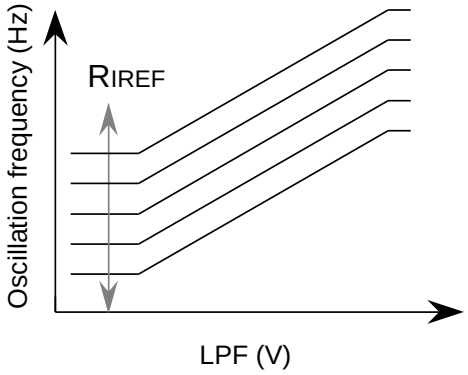


The frequency gain of the VCO of the EFM-PLL can be controlled by connecting the external resistor between RC pin and GND.

(Recommend value)

R_{RC}= 15KΩ





The gain of the oscillation frequency (Δf / ΔV) can be controlled by the external resistor R_{RC} and the minimum oscillation frequency can be controlled by the external resistor R_{IREF}. And the frequency divider ratio of the internal VCO of the EFM-PLL can be also controlled by the address 05h resister for each playback speed.

The external resistor R_{IREF} decide the characteristics of the free-run frequency of the internal VCO and the reference current for all analog circuit.

If the range of the free run is too wide, the error rate characteristics may be influenced. If the range of the free run is too narrow, the characteristics of the access time may be influenced. And if the minimum oscillation frequency is too high, the low disc rotation detector can not detect less than 2/3 of the normal rotation. So the minimum oscillation frequency need to set less than 1/2 of the play back frequency. The oscillation of the internal VCO of the EFM-PLL can be confirmed at EFFK pin.

The oscillation frequency of the VCO of the EFM-PLL = EFFK frequency X 1176

(8.6472MHztyp X S) (7.35KHztyp X S)

(S:Play back speed)

4.EFM demodulation

The EFM signal that has been converted to logic level, and the EFM clock that has been extracted from the EFM signal are input to the de-modulator and converted to an 8 bit symbol.

The EFM de-modulation depends on the EFM table in the RED book.

To demodulate, the demodulator must be synchronized to EFM signal for each frame. The frame synchronization protection circuit holds the synchronization in spire of some lack of synchronization pattern, and prevents false synchronization if demodulator bit-slipping or mis-synchronization occurs.

The frame synchronization control block diagram show fig.4.

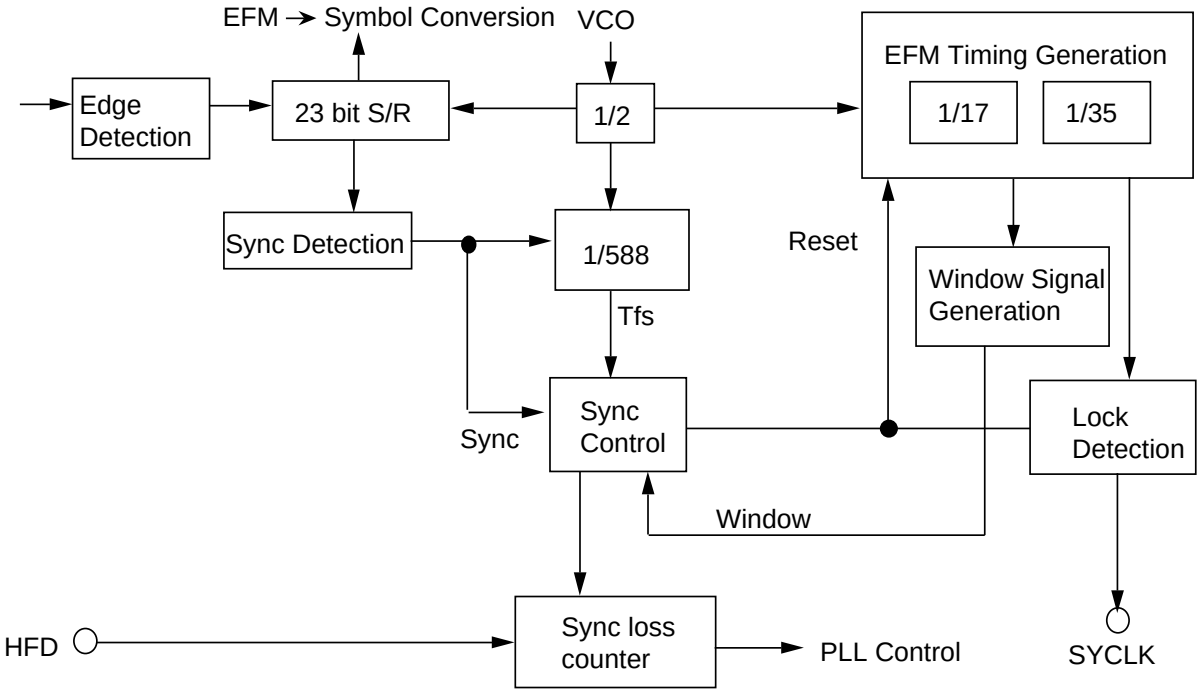


Fig. 4: Frame synchronize control part block diagram

In this figure, generation condition of counter reset signal in EFM timing generation block is as follows.

Reset = Sync X Tfs + Sync X Window (X: logical multiplication, +: logical addition)

where Sync, Tfs and Window mean synchronization signal, detection signal of synchronization signal blank, and window signal of ±7ck. In the synchronous state, Sync and Tfs generate simultaneously and Sync comes to the center of the window. At this time, "H" is output to the SYCLK pin, and EFM signal is synchronized by frame unit. Frame sync. status can be monitored in SYCLK mode at LOCK/DRD pin.

On the other hand, the SYCLK signal includes some bounce even during the sync. state when there is a lack of sync. pattern because of a defect in the disc. Hence there is a need for debouncing the sync. status signal, in order for it to be monitored by the MCU.

This debouncing is accomplished in the M65827FP by monitoring the frame sync. status at 1/16 EFM frame clock intervals (normal speed: 2.13msec) and then outputting the result to the LOCK/DRD pin. If monitored status is "locked" then output is "H", and after 8 continuous intervals of "unlocked" are observed, output becomes "L".

Also, when the disc rotation does not reach the target speed, lock monitor may become "LOCK" state because of its wide lock range. In such state, when an audio disc plays, noise may be generated by releasing mute state when LOCK signal become "H". The LOCK signal can output when the disc rotation in CLV mode in order to prevent noise generation. Output condition of the LOCK signal can be set by the D5 bit of address 07h.

5.CLV servo control

(1) PWM control

CLV servo control circuit operates using two signals. The first is the frequency difference between EFM clock and X'tal clock, and the second is the phase difference between write frame address and read frame address of the internal RAM. Motor control signals are output in PWM wave form to the PWM1 (-signal) PWM2 (+signal) pins. Because these signals are internally phase compensated, the CLV servo control circuit can be composed easily using current drivers on pins PWM1 and PWM2.

Kick pulse, Brake pulse, and Start/Stop are output to PWM1 and PWM2 under MCU control. When HDF becomes "H" (when HF signal is detected), PWM1 and PWM2 are automatically fixed duty pulse width to prevent disc from overrun. When the difference between the writing address and reading address of internal RAM exceeds ±8 frames because of PLL disc rotation jitter, the address of crystal is loaded to PLL address counter and reset so that the jitter margin become maximum. The result of memory overflow from disc rotation jitter can be monitored from the INT pin. The result is expanded to 128 frames.

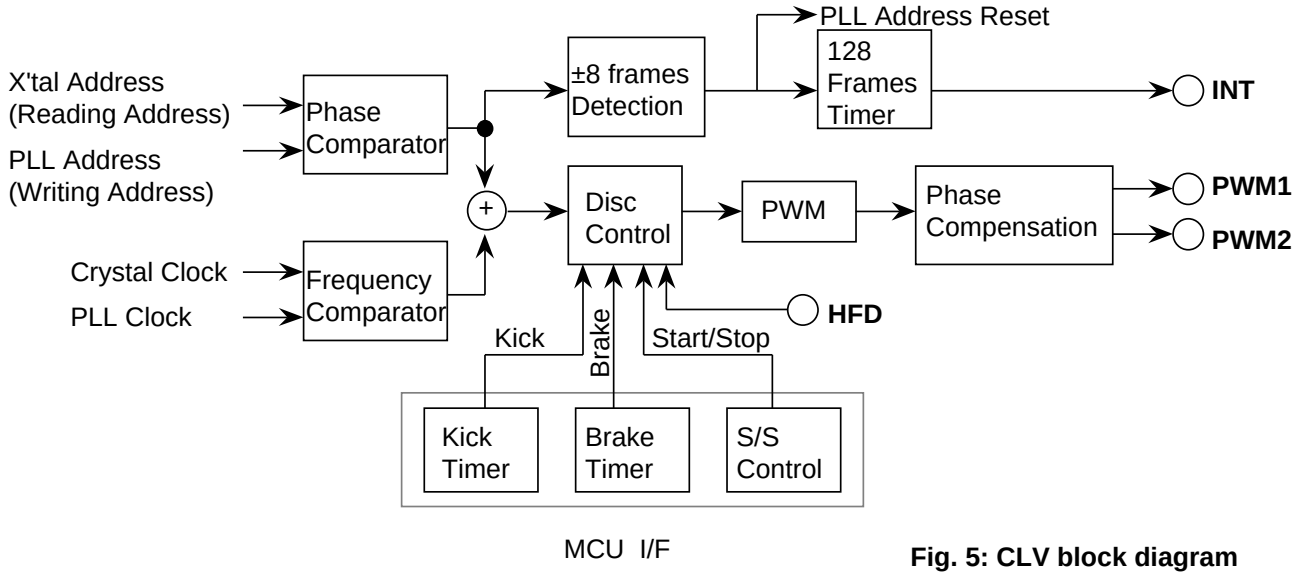


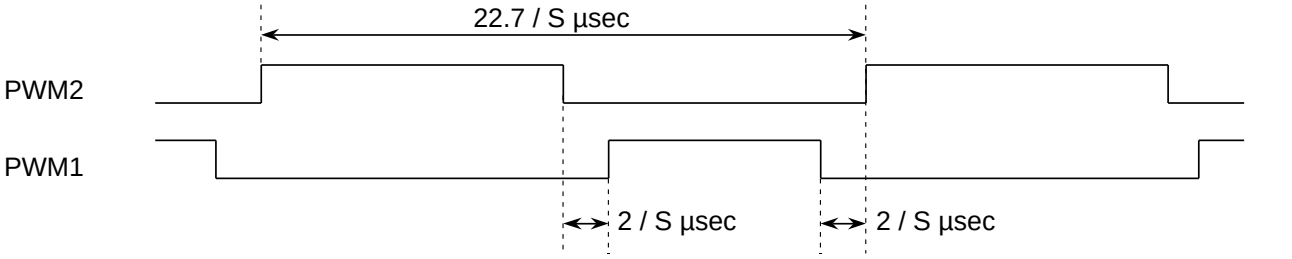
Fig. 5: CLV block diagram

Pin \ MODE	KICK	CLV	BRAKE	STOP
PWM2 (+signal)	H	*	L	L
PWM1 (- signal)	L	*	H	L

Table 3: PWM output state at each mode

Fig.6 shows CLV wave form and its duty.

Disc motor can be driven by PWM waveforms directly, or it can be driven by an analog signal that can be generated by integration of the PWM waveforms. By using an analog signal, it is possible to adjust the servo loop gain by varying direct external component values, but in the case of PWM waveforms, the servo loop gain is determined by motor torque, and the rotating moment of the disc, turntable, and disc clamper.



(S:PlayBack Speed)

$$\text{Duty} = \frac{\text{WPWM2-WPWM1}}{\text{WPWM2+WPWM1}} + 1$$

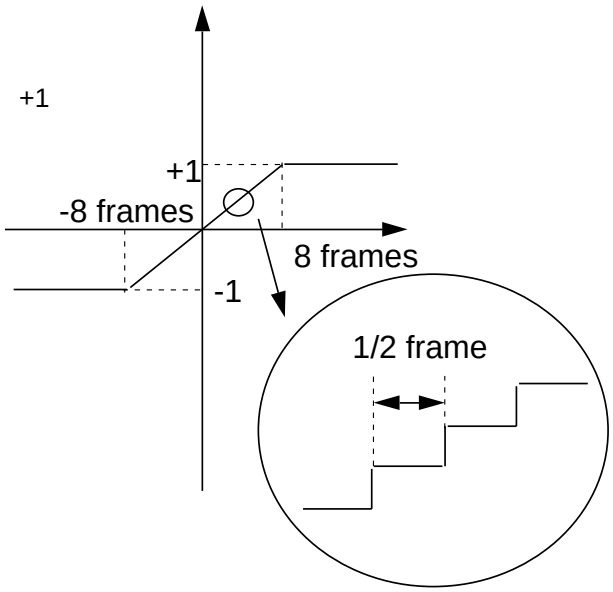


Fig. 6: CLV waveform

6. HFD (HF defect signal input)

Inputting "H" to the HFD pin when an HF signal defect is detected prevents the PLL and disc from incorrect behavior caused by scratches and dust and fastens PLL re-lock after HF signal recovery.

It enable by inputting "H" to HFD input pin when HF signal defect.

Internal function is as follows:

Internal action when HFD is "H"

(1) Charge pump both PLL phase comparator and frequency comparator is HiZ state, VCO control voltage is held
(2) Slice level of TLC pin is held
(3) CLV PWM output is fixed duty

Described function can be canceled by inputting "H" to HFDDIS register at address 01h.

7.Error correction

(1) Correctability

Max C1:2 error correction, C2:4 error correction.
C1:2 error correction, C2:2 error correction (no eraser correction mode) can be chose at address 01h.

(2) Error monitor output

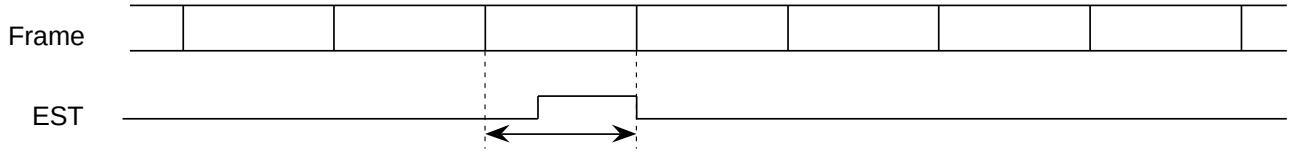
Error states which are detected during decoding are output to EST pin by setting ERM register at address D7h.

When ERM2, ERM1, and ERM0 are all "0", the error flag is output to the EST pin. On the other case, the unit error flag is output in current frame unit..

CD-ROM mode is selected by the NONAUDIO register at address 01h, output data is not interpolated, and error status of the C2 decoder are output in every data byte that can not be corrected.

When the NONAUDIO register at address01h selects audio mode, every interpolating word (2 byte) outputs the error status of the C2 decoder.

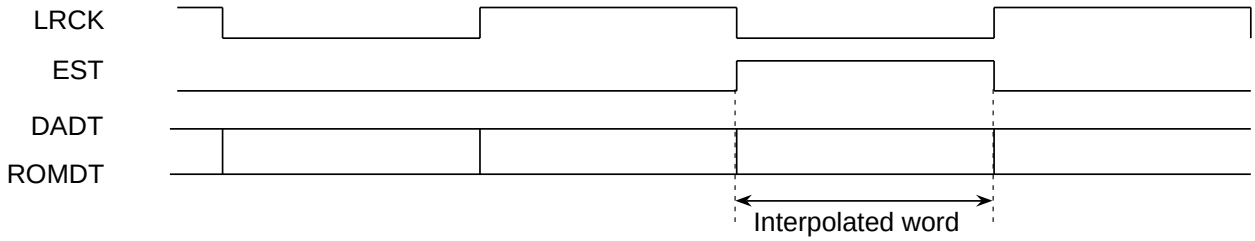
(a) Frame unit error monitor output (except ERM2=ERM1=ERM0=L)



Frame which error is detected

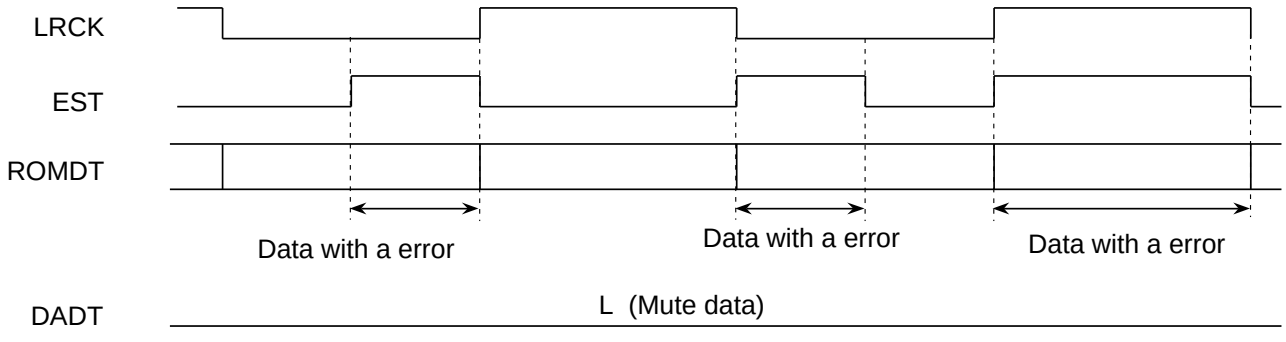
(b) Data unit error monitor output

(b-1) Audio mode (NONAUDIO register is "0")



Both DADT and ROMDT are same output.

(b-2) CD-ROM mode (NONAUDIO register is "1")



ROMDT pin output CD-ROM data.
DADT pin output mute data.

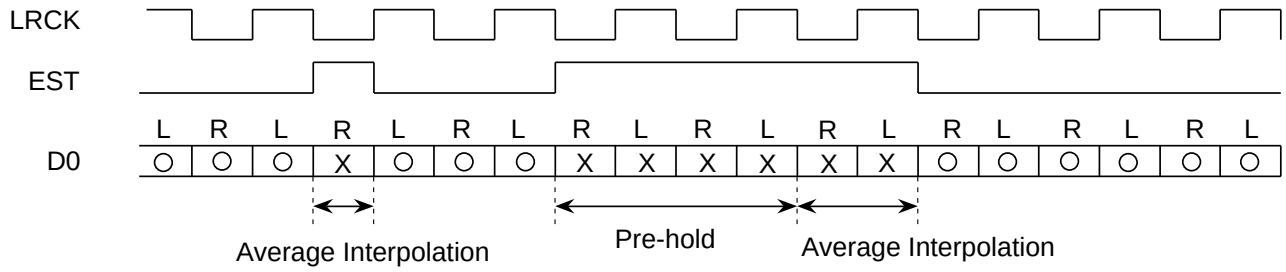
The frame unit error monitor is a mode to check decode condition. When an error flag is used for CD-ROM decoder, it needs to set ERM register at address 07h to ERM2=ERM1=ERM0=L.

(3) Interpolation

When an error word is judged uncorrectable by C2 decoding, average interpolation or pre-hold interpolation is performed and noise product prevented.

When an error is detected in a word, if the previous and subsequent words are error-free, average interpolation is attempted. If the previous or subsequent word is in error, pre-hold is tried.

When CD-ROM mode is selected by the NONAUDIO register at address 01h, interpolation management is not performed.



8.Digital audio interface output

The digital audio interface signal according to EIAJ regulation CP-1201 "digital audio interface" is output to the DOTX pin.

Validity flag is set automatically to "1" when the interpolated word is transmitted. The data that is read from the subcode interface block is transmitted to user data. Channel status clock accuracy and source number can be set using the MCU interface.

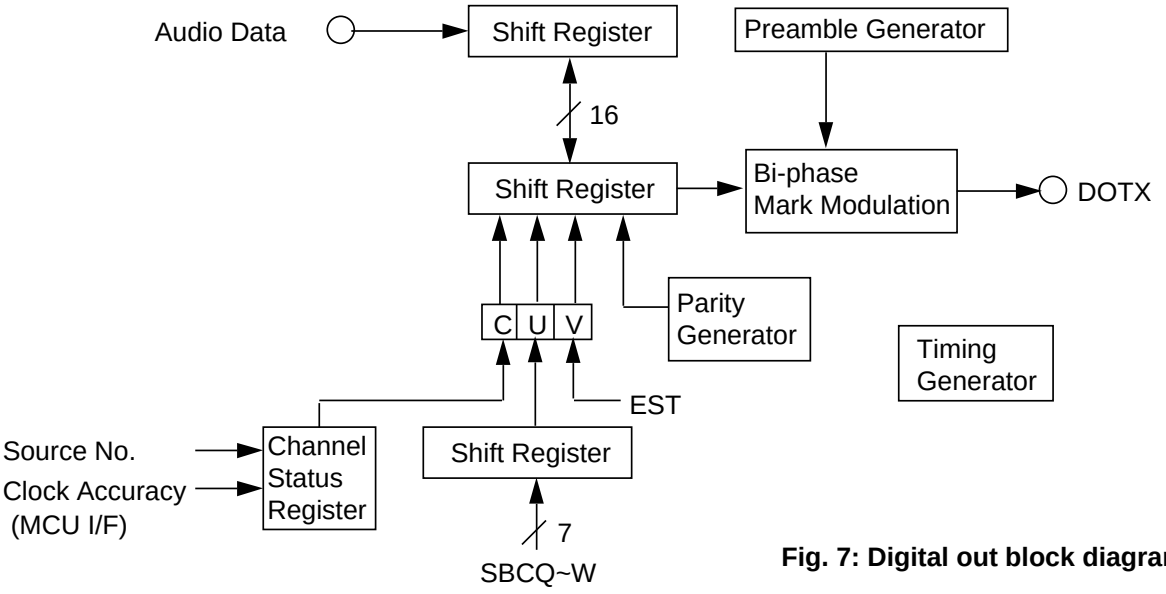
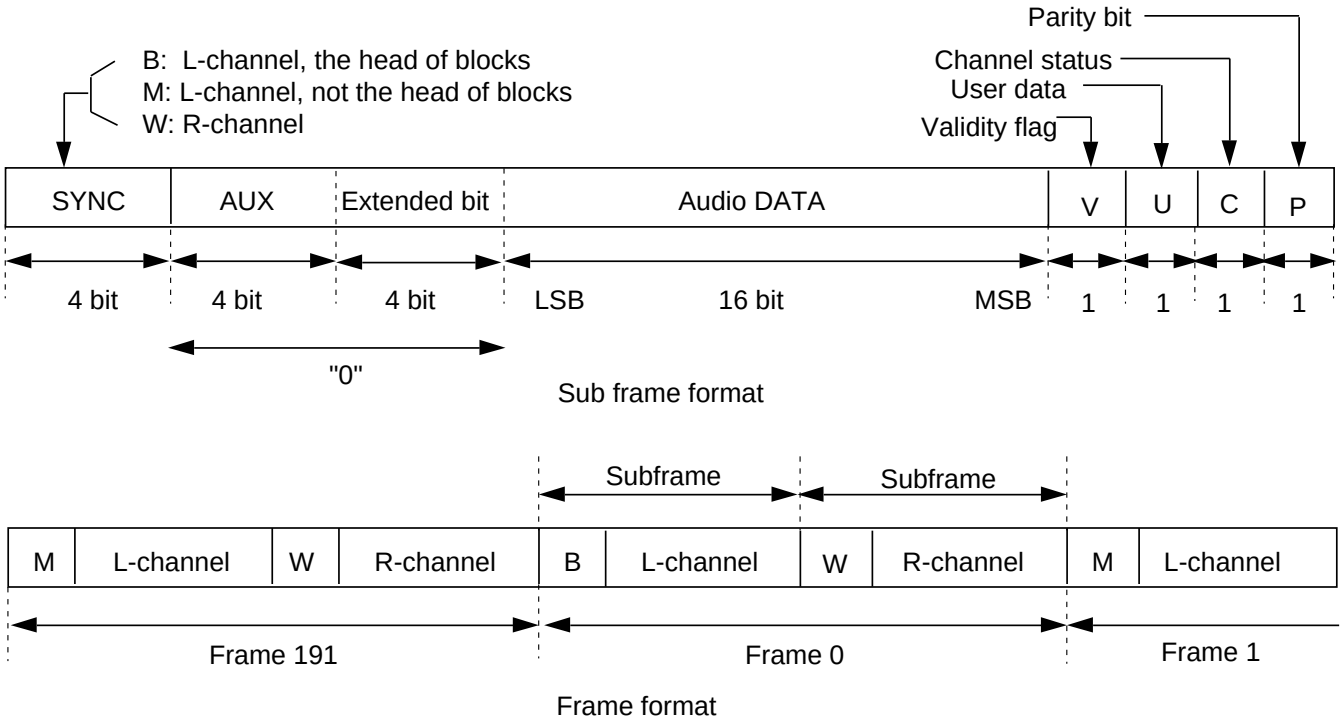
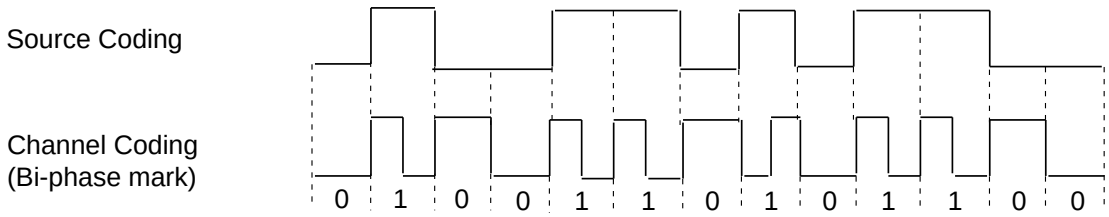


Fig. 7: Digital out block diagram





Channel coding (Bi-phase mark modulation)

In order to prevent radiation when digital output is not used, DOTX pin output can be fixed to "L" by setting at address 0Fh.

Channel status is set in IC as follows:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	from Subcode Q			0	0	0	0	1	0	0	0	0	0	0	0
		ID1	COPY	EMP												
16	SOURCE0	SOURCE1	SOURCE2	SOURCE3	0	0	0	0	0	0	0	0	ACCK0	ACCK1	0	0
32																
48																
64																
80																
96																
112																
128																
144																
160																
176																

Set by MCU

ALL 0

ID1,COPY,EMP are set when CRC flag is OK and subcode sync S0,S1 are detected at fixed position. In case any condition is NG, previous data is held.

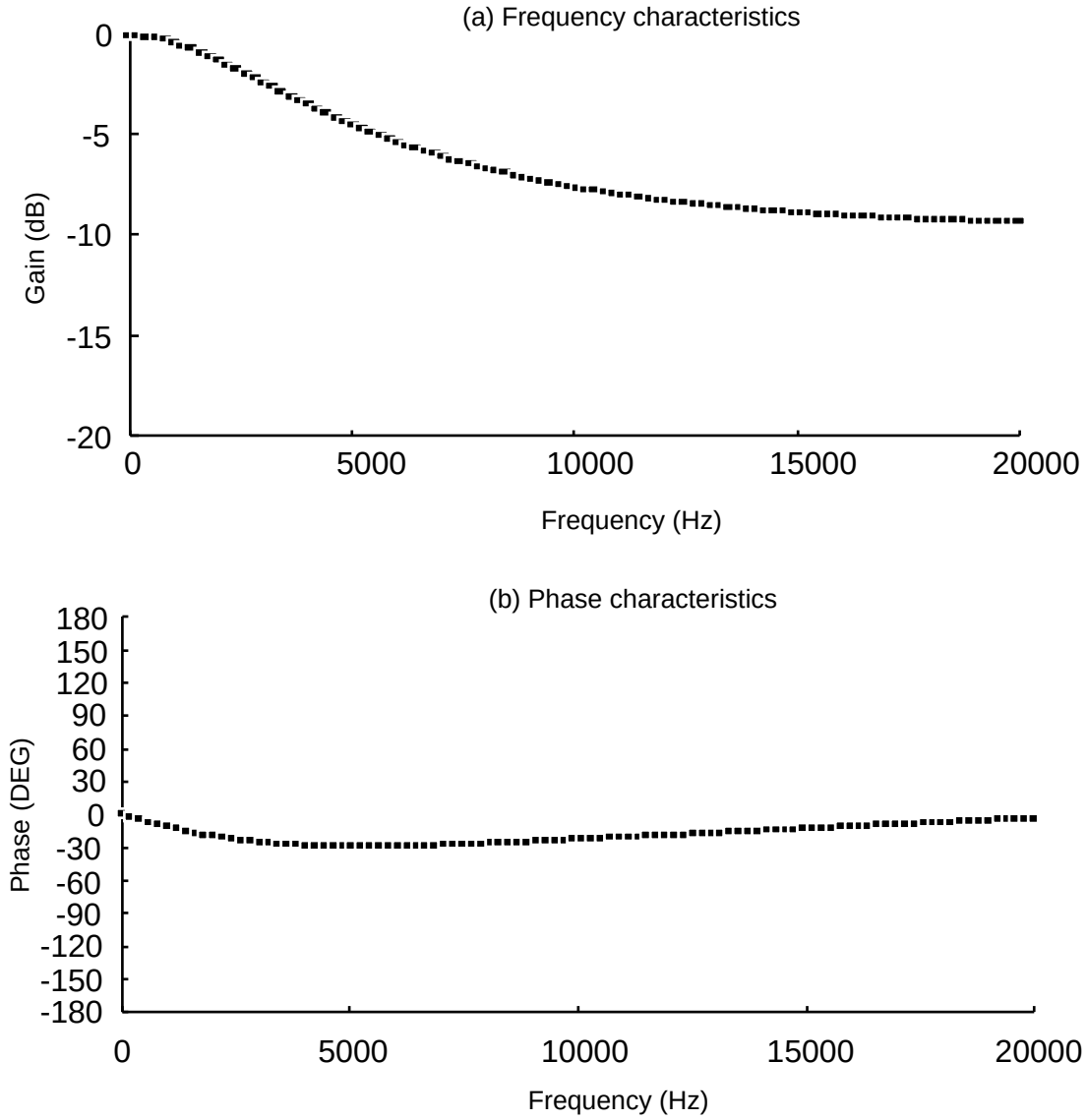
The validity flag is copied with the EST flag at audio mode.

9.Digital de-emphasis

M65827FP has a digital de-emphasis circuit composed of a first order IIR filter. When internal circuit defect emphasis state, a 50 /15 µ de-emphasis circuit automatically becomes active.

When DDEPASS register at address 04h is "1", de-emphasis pass mode is selected.

Figure 8 shows the characteristics of internal de-emphasis filter.



Frequency	Deviation*
0~18kHz	less than±0.2dB
18~20kHz	less than±0.5dB

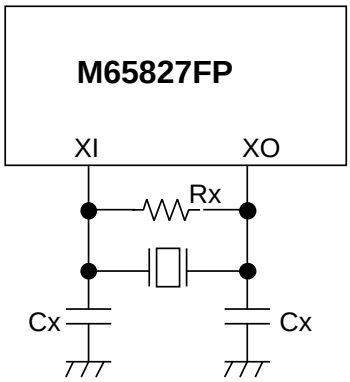
* Gain deviation from imaginary equation as follows:
(1+S•15µS)/(1+S•50µS)

Fig. 8: De-emphasis characteristics

10.DOscillation circuit and Timing generator

(1) Internal oscillation mode

The oscillation circuit can be formed by connecting a crystal oscillator, load resistance and load capacitors to pins XI and XO.

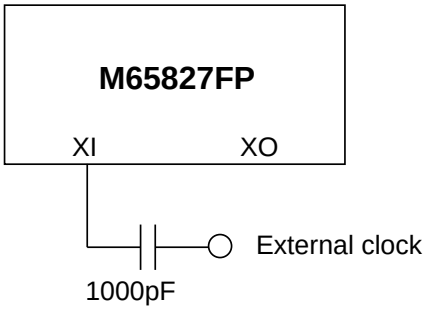


Oscillator	Cx (cf.)	Rx (cf.)
8.4672MHz	30pF	1MΩ
16.9344MHz	15pF	1MΩ
33.8688MHz	5pF	1MΩ

(Recommend value)

(2) External clock mode

When the system contains a clock, the clock can be input to pin XI via a capacitor without using the crystal oscillator. If the input signal is logic level, the capacitor is not necessary.

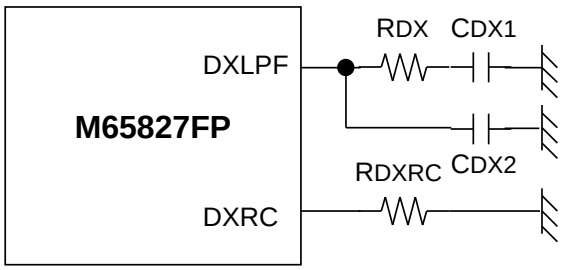


External clock	MIN	MAX
VIL	DVSS	——
VIH	——	DVDD3
AMPLITUDE	2VP-P	——

(3) Clock doubler circuit

M65827FP has a clock doubler, double and quad frequency master clock can be generated by composing loop filter at DXLPF pin. Clock doubler is selected at address 05h resister.

The gain of the internal VCO of the clock doubler can be controlled by connecting the external resistor R_{DXRC} between DXRC pin and GND. And the minimum frequency is determined by the reference current control resistor R_{IREF}.



(Recommend value)

R_{DX} = 1.8KΩ
C_{DX1} = 0.15μF
C_{DX2} = 470pF
R_{DXRC} = 15KΩ

(4) Clock output

M65827FP has various master clock dividers in order to realize many playback speeds. Of the clocks given by master clock divider, system clock and half clock are output from special pin. C423 output half clock of the crystal oscillator. C423 can be used for MCU master clock.

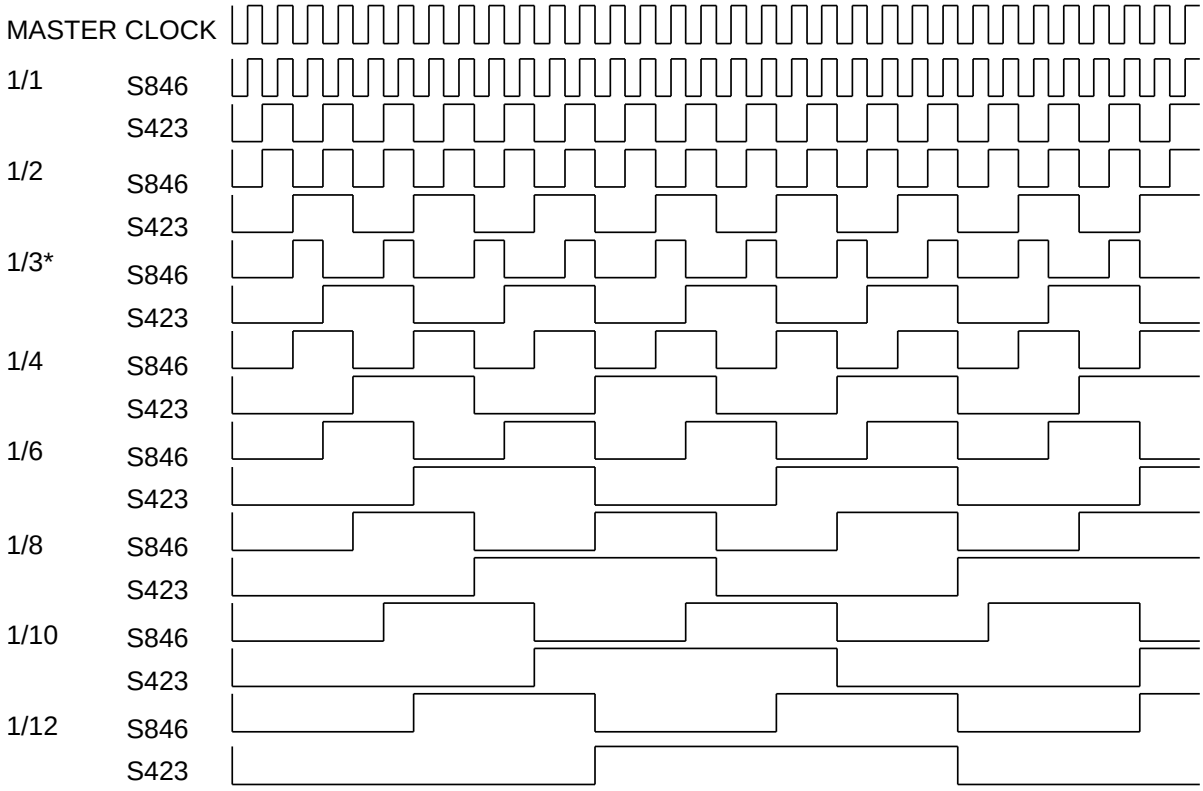
S846 and S423 output a clock which is synchronized with the M65827FP internal system clock. S846 and S423 can be used for external digital filter and CD-ROM decoder. When PLCKSEL is 1, system clock of M65827FP will be clock generated by PLL, and the clocks of S846 and S423 are synchronized with the PLL clock. When PLCKSEL is 0, system clock of M65827FP will be clock generated by X'tal, and the clocks of S846 and S423 are synchronized the X'tal clock.

(5) C423 (MCU system clock)

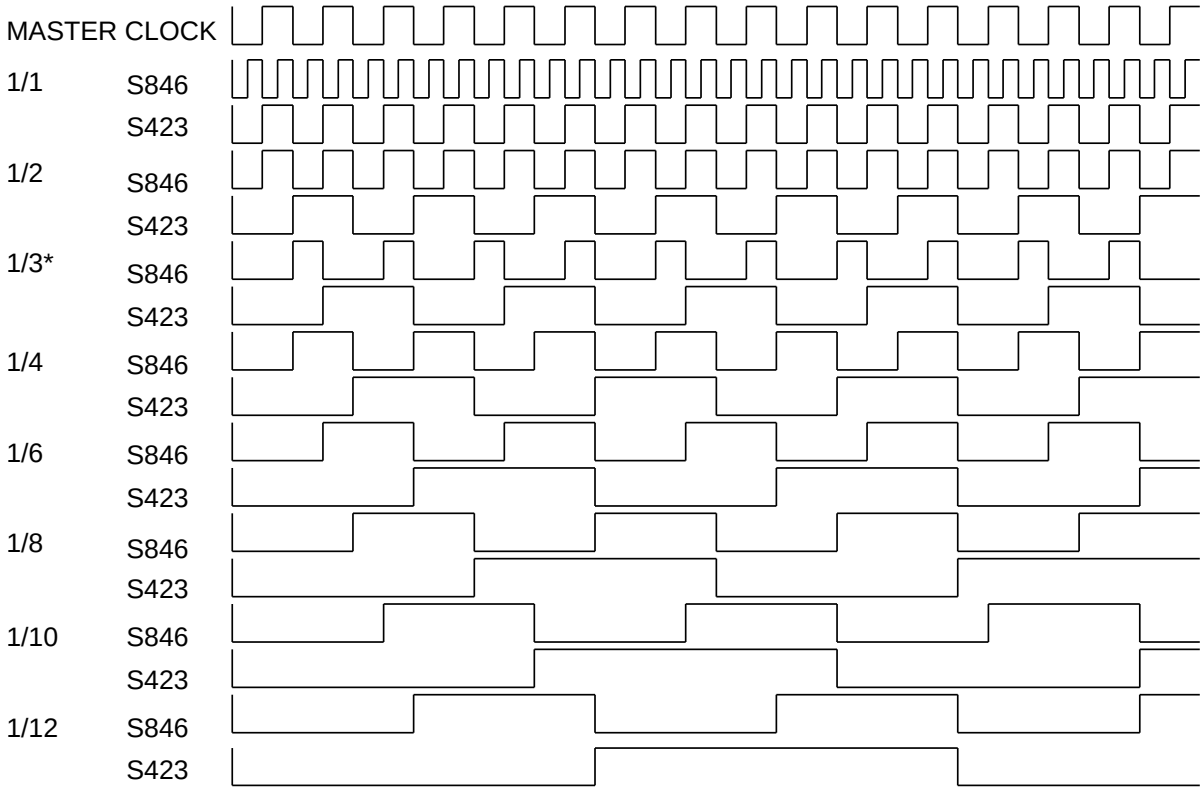
C423 pin outputs half clock of oscillator's clock. The clock is independent on playback speed selector and clock doubler. it is used for MCU system clock.

(6) Clock output timing

1.PLCKSEL = 0,EXSEL = 0,DXSEL = 0



2.PLCKSEL = 0,EXSEL = 0,DXSEL = 1

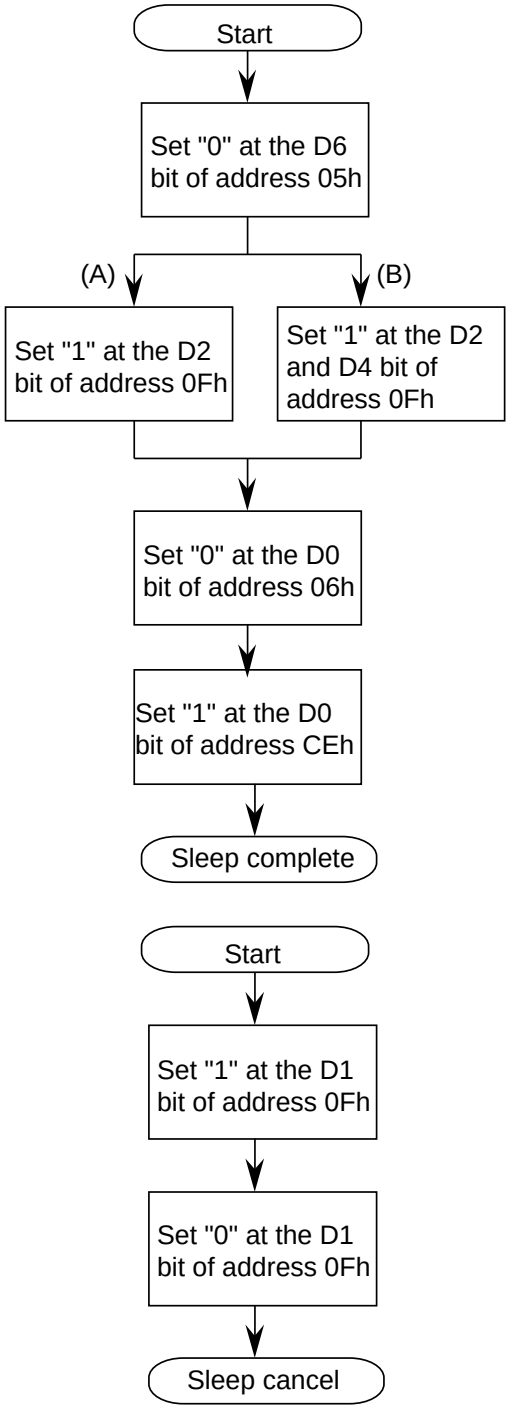


*When 1/3 is selected, output of C846 and S846 is 33% duty.

3.PLCKSEL = 1

When PLCKSEL register is 1, S846 has 24 intervals in a frame that do not output clock by 588/576 conversion. Other clock and data that is synchronized with S846 have same interval.

(7) Sleep mode



Clock doubler unselect.
If the clock doubler mode is not selected, this step is not needed.

Digital sleep mode.
The system clock stop to supply to the internal logic and the internal SRAM change to the disable mode.
If C423 output signal is used in the sleep condition, please set "1" at the only D2 resister of the address 0Fh. If C423 output signal is not needed, please set "1" at the D2 and D4 resister of the address 05h.

Analog sleep mode.
The reference current of all analog circuit is stopped.

Stop the oscillation of the VCO of the EFM-PLL.
The charge pump of the EFM-PLL output "L" and the internal VCO stop the oscillation.

DSP is initialized by the hard reset command and the sleep mode is canceled .
This command is same with inputting reset pulse to ALCR pin.

4. Playback speed control selector and each clock frequency

Master clock	CKSEL2	CKSEL1	CKSEL0	DXCK	PLCKSEL	C423	S846	S423	DSCK	LRCK
S x 192fs	L	L	L	L	L	S x 96fs	S x 192fs	S x 96fs	S x 48fs	S x fs
S x 192fs	L	L	H	L	L	S x 96fs	S x 96fs	S x 48fs	S x 24fs	S x (1/2)fs
S x 192fs	L	H	L	L	L	S x 96fs	S x 64fs	S x 32fs	S x 16fs	S x (1/3)fs
S x 192fs	L	H	H	L	L	S x 96fs	S x 48fs	S x 24fs	S x 12fs	S x (1/4)fs
S x 192fs	H	L	L	L	L	S x 96fs	S x 32fs	S x 16fs	S x 8fs	S x (1/6)fs
S x 192fs	H	L	H	L	L	S x 96fs	S x 24fs	S x 12fs	S x 6fs	S x (1/8)fs
S x 192fs	H	H	L	L	L	S x 96fs	S x 19.2fs	S x 9.6fs	S x 4.8fs	S x (1/10)fs
S x 192fs	H	H	H	L	L	S x 96fs	S x 16fs	S x 8fs	S x 4fs	S x (1/12)fs
S x 96fs	L	L	L	H	L	S x 48fs	S x 192fs	S x 96fs	S x 48fs	S x fs
S x 96fs	L	L	H	H	L	S x 48fs	S x 96fs	S x 48fs	S x 24fs	S x (1/2)fs
S x 96fs	L	H	L	H	L	S x 48fs	S x 64fs	S x 32fs	S x 16fs	S x (1/3)fs
S x 96fs	L	H	H	H	L	S x 48fs	S x 48fs	S x 24fs	S x 12fs	S x (1/4)fs
S x 96fs	H	L	L	H	L	S x 48fs	S x 32fs	S x 16fs	S x 8fs	S x (1/6)fs
S x 96fs	H	L	H	H	L	S x 48fs	S x 24fs	S x 12fs	S x 6fs	S x (1/8)fs
S x 96fs	H	H	L	H	L	S x 48fs	S x 19.2fs	S x 9.6fs	S x 4.8fs	S x (1/10)fs
S x 96fs	H	H	H	H	L	S x 48fs	S x 16fs	S x 8fs	S x 4fs	S x (1/12)fs

fs = 44.1kHz,S:Playback speed (S-times)

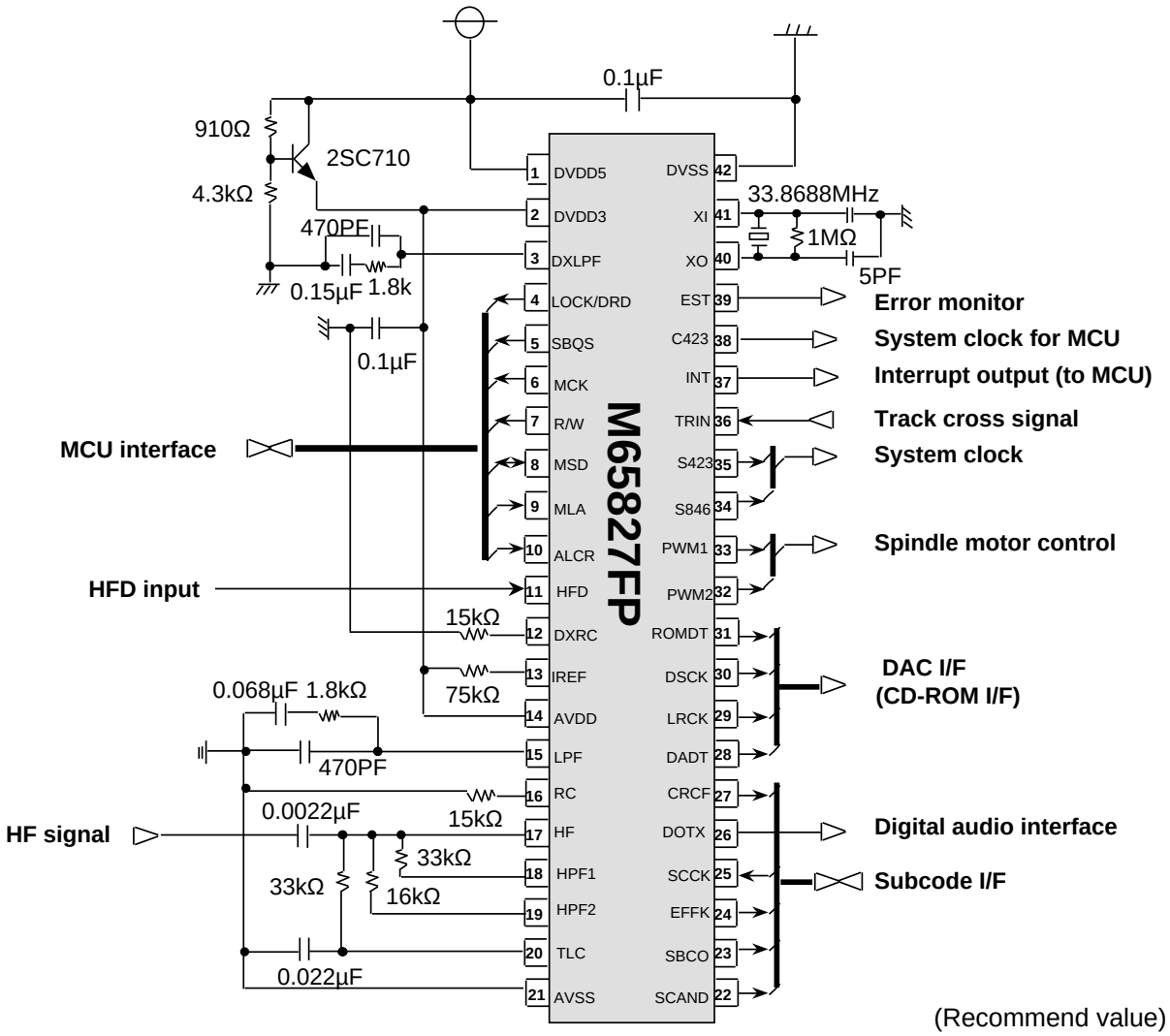
Master clock	CKSEL2	CKSEL1	CKSEL0	DXCK	PLCKSEL	C423	S846	S423	DSCK	LRCK
S x 192fs	L	L	L	L	H	S x 96fs	S x 192fs typ	S x 96fs typ	S x 48fs typ	S x fs typ
S x 192fs	L	L	H	L	H	S x 96fs	S x 96fs typ	S x 48fs typ	S x 24fs typ	S x (1/2)fs typ
S x 192fs	L	H	L	L	H	S x 96fs	S x 64fs typ	S x 32fs typ	S x 16fs typ	S x (1/3)fs typ
S x 192fs	L	H	H	L	H	S x 96fs	S x 48fs typ	S x 24fs typ	S x 12fs typ	S x (1/4)fs typ
S x 192fs	H	L	L	L	H	S x 96fs	S x 32fs typ	S x 16fs typ	S x 8fs typ	S x (1/6)fs typ
S x 192fs	H	L	H	L	H	S x 96fs	S x 24fs typ	S x 12fs typ	S x 6fs typ	S x (1/8)fs typ
S x 192fs	H	H	L	L	H	S x 96fs	S x 19.2fs typ	S x 9.6fs typ	S x 4.8fs typ	S x (1/10)fs typ
S x 192fs	H	H	H	L	H	S x 96fs	S x 16fs typ	S x 8fs typ	S x 4fs typ	S x (1/12)fs typ
S x 96fs	L	L	L	H	H	S x 48fs	S x 192fs typ	S x 96fs typ	S x 48fs typ	S x fs typ
S x 96fs	L	L	H	H	H	S x 48fs	S x 96fs typ	S x 48fs typ	S x 24fs typ	S x (1/2)fs typ
S x 96fs	L	H	L	H	H	S x 48fs	S x 64fs typ	S x 32fs typ	S x 16fs typ	S x (1/3)fs typ
S x 96fs	L	H	H	H	H	S x 48fs	S x 48fs typ	S x 24fs typ	S x 12fs typ	S x (1/4)fs typ
S x 96fs	H	L	L	H	H	S x 48fs	S x 32fs typ	S x 16fs typ	S x 8fs typ	S x (1/6)fs typ
S x 96fs	H	L	H	H	H	S x 48fs	S x 24fs	S x 12fs typ	S x 6fs typ	S x (1/8)fs typ
S x 96fs	H	H	L	H	H	S x 48fs	S x 19.2fs typ	S x 9.6fs typ	S x 4.8fs typ	S x (1/10)fs typ
S x 96fs	H	H	H	H	H	S x 48fs	S x 16fs typ	S x 8fs typ	S x 4fs typ	S x (1/12)fs typ

fs = 44.1kHz,S:Playback speed (S-times)

At PLCKSEL=1, C846 and C423 are synchronized to master clock, S846, S423, DSCK, and LRCK are synchronized to PLL.

S846, S423, DSCK, and LRCK represent typical state frequency which disc rotation reaches at target playback speed.

APPLICATION CIRCUIT



(Recommend value)