

MITSUBISHI LSTTLs M74LS96P

5-BIT SHIFT REGISTER

DESCRIPTION

The M74LS96P is a semiconductor integrated circuit containing a 5-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

- Positive edge-triggering
- Right shift function
- Asynchronous parallel input provided
- Direct reset input provided
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

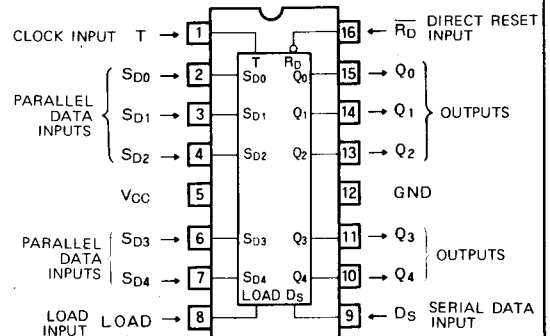
This 5-bit shift register is composed with 4 R-S-T flip-flops and it functions as a serial/parallel input-serial/parallel output shift register.

For use as a serial input-serial/parallel output shift register, the load input LOAD or parallel data inputs $S_{D0} \sim S_{D4}$ are kept in high and the data are applied to the serial data input D_S . When a clock pulse is applied to clock input T with D_S in high, the high signal is shifted sequentially to $Q_0, Q_1 \dots Q_4$. Shifting is performed when T changes from low to high. When the serial data are applied to $D_{S0} \sim D_{S4}$ and LOAD is set high, the $S_{D0} \sim S_{D4}$ signals appear in $Q_0 \sim Q_4$ respectively irrespective of T.

When direct reset input R_D is set low, $Q_0 \sim Q_4$ are set low if LOAD is low irrespective of the other input signals.

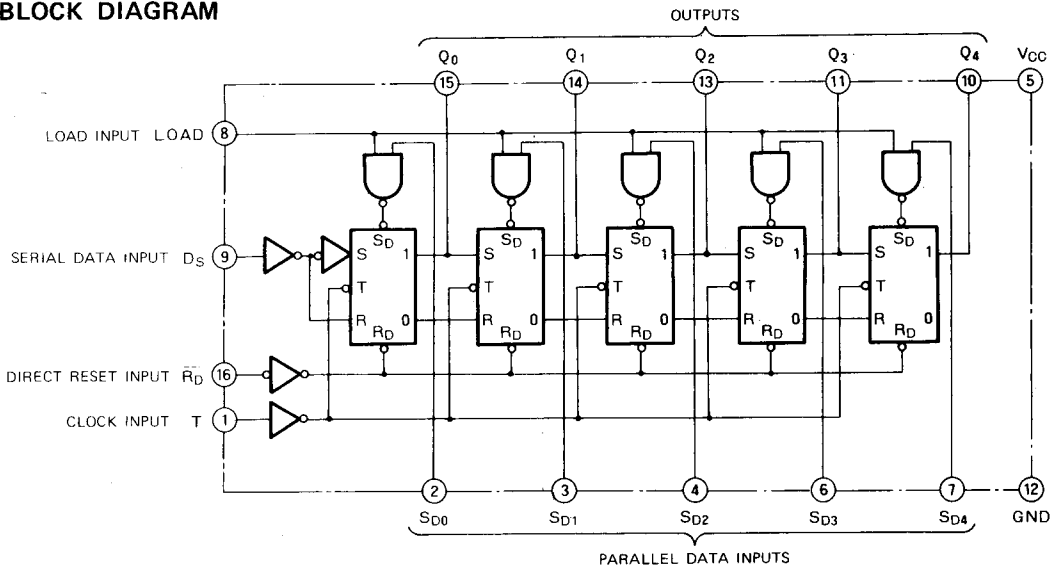
When LOAD is high, parallel reading takes precedence, and the $S_{D0} \sim S_{D4}$ signals appear in $Q_0 \sim Q_4$.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



5-BIT SHIFT REGISTER

FUNCTION TABLE (Note 1)

SERIAL INPUT-PARALLEL OUTPUT

	t_n	t_{n+1}	t_{n+2}	t_{n+3}	t_{n+4}	t_{n+5}	t_{n+6}
D_S	L	H	L	H	L	H	L
Q_0	*	L	H	L	H	L	H
Q_1	*	*	L	H	L	H	L
Q_2	*	*	*	L	H	L	H
Q_3	*	*	*	*	L	H	L
Q_4	*	*	*	*	*	L	H

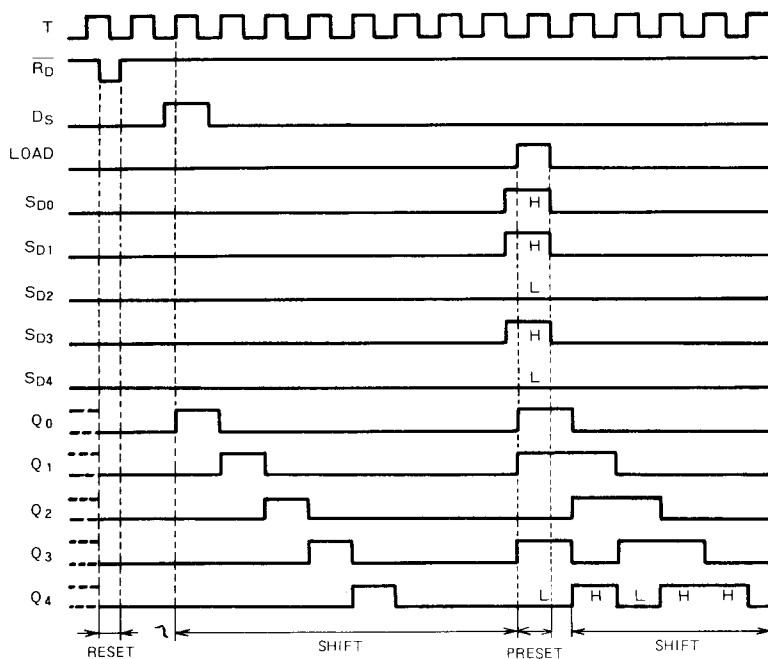
Note 1: For use as a serial input-parallel output, LOAD, S_{D0} , S_{D1} , S_{D2} , S_{D3} and S_{D4} are all kept at low and R_D is kept at high.
 t_n : Bit time prior to clock
 t_{n+1} : Bit time after application of 1 clock pulse
 t_{n+6} : Bit time after application of 6 clock pulses
 * : Cannot be predicted

PARALLEL INPUT-PARALLEL OUTPUT

LOAD	$S_{D(N)}$	R_D	$Q(N)$
L	L	L	L
L	L	H	Q^0
L	H	L	L
L	H	H	Q^0
H	L	L	L
H	L	H	Q^0
H	H	L	H
H	H	H	H

Note 2: For use as a parallel input-parallel output, R_D is first set low and kept at high. The parallel input data are input into $S_{D0} \sim S_{D4}$. The data are read when LOAD is high and they simultaneously appear in the outputs. R_D is usually kept at high and LOAD at low. The "N" in $S_{D(N)}$ refers to 0, 1, 2, 3, 4. Q^0 is the level of Q before the indicated steady-state input conditions were established.

OPERATION TIMING DIAGRAM



5-BIT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage		-0.5 ~ +15	V
V _O	Output voltage	High-level output	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V _{CC}	Supply voltage		4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≥ 2.7V	0		-400	μA
I _{OL}	Low-level output current	V _{OL} ≤ 0.4V	0		4	mA
		V _{OL} ≤ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ *	Max	
V _{IH}	High-level input voltage			2			V
V _{IL}	Low-level input voltage					0.8	V
V _{IC}	Input clamp voltage		V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage		V _{CC} = 4.75V, V _I = 0.8V V _I = 2V, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Low-level output voltage		V _{CC} = 4.75V V _I = 0.8V, V _I = 2V	I _{OL} = 4mA	0.25	0.4	V
				I _{OL} = 8mA	0.35	0.5	V
I _{IH}	High-level input current	LOAD	V _{CC} = 5.25V			100	μA
		Other inputs	V _I = 2.7V			20	
		LOAD	V _{CC} = 5.25V			0.5	mA
		Other inputs	V _I = 10V			0.1	
I _{IL}	Low-level input current	LOAD	V _{CC} = 5.25V			-2.0	mA
		Other inputs	V _I = 0.4V			-0.4	
I _{OS}	Short-circuit output current (Note 3)		V _{CC} = 5.25V, V _O = 0V	-20		-100	mA
I _{CC}	Supply current		V _{CC} = 5.25V (Note 4)		12	20	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

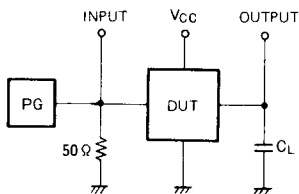
Note 4: I_{CC} is measured with R_D at 0V and all the other inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
f _{max}	Maximum clock frequency		C _L = 15pF (Note 5)	25	45		MHz
t _{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q ₀ ~ Q ₄				12	40	ns
t _{PHL}					12	40	ns
t _{PLH}	Low-to-high-level output propagation time, from input S _D , LOAD to outputs Q ₀ ~ Q ₄				11	35	ns
t _{PHL}	High-to-low-level output propagation time, from input R _D to outputs Q ₀ ~ Q ₄				11	35	ns

5-BIT SHIFT REGISTER

Note 5: Measurement circuit

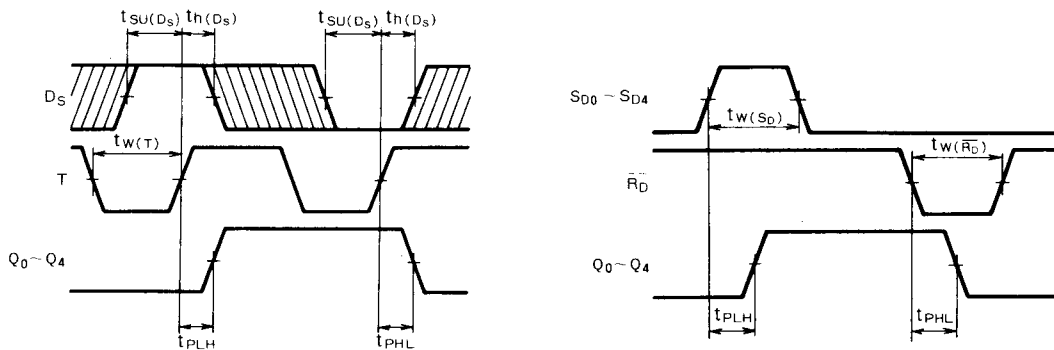


- (1) The pulse generator (PG) has the following characteristics.
 PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$,
 $V_P = 3V_{P-P}$, $Z_0 = 50\Omega$.
- (2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a = 25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_w(T)$	Clock input T pulse width		20	5		ns
$t_w(S_D)$	Parallel data input pulse width		30	5		ns
$t_w(\overline{RD})$	Direct reset pulse width		30	5		ns
$t_{su}(D_S)$	Setup time D_S to T		30	3		ns
$t_h(D_S)$	Hold time D_S to T		5	-1		ns

TIMING DIAGRAM (Reference level = 1.3V)

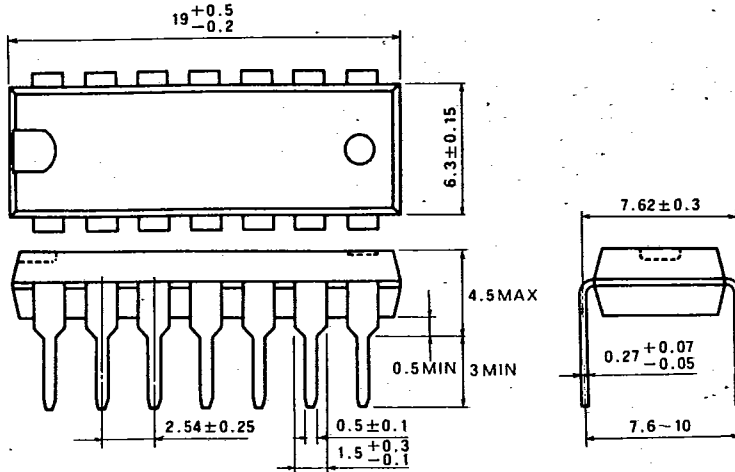


Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

T-90-20

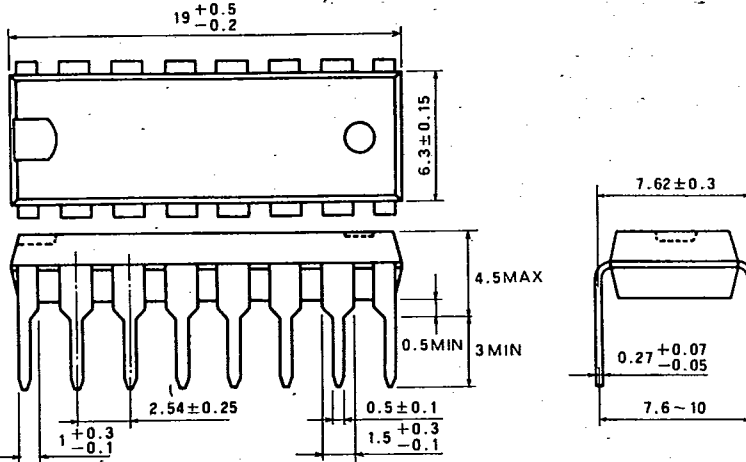
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

